2.45 GHz Power and Data Transmission for a Low-Power Autonomous Sensors Platform

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ABSTRACT

This paper describes a power conversion and data recovery system for a microwave powered sensor platform. A patch microwave antenna, a matching filter and a rectifier make the system front-end and implement the RF-to-DC conversion of power carrier. The efficiency of the power conversion is as high as 47% with an input power level 250 μW at 2.45 GHz. Then, a 0.18 μm CMOS integrated circuit extracts the clock and the digital data. A modified pulse amplitude modulation scheme is used to modulate the data on the 2.45 GHz carrier frequency for combined data and power transmission; this scheme allows very low power consumption of the entire IC to be less than 10 μW and making the system suitable for an autonomous wireless connected sensor module.

Categories and Subject Descriptors

B.7.1 [**Integrated Circuits**]: Types and Design Styles – *VLSI (very large scale integration).*

General Terms

Design.

Keywords

Wireless sensor, RF to DC power conversion, microwave power transmission, low power clock and data recovery.

1. INTRODUCTION

Sensor systems will evolve toward a fully nomadic yet fully interconnected approach. Each electro-mechanical apparatus and physical system will be supported by a number of full set of electronic devices, all of them behaving as a micro-system connected to a hierarchy of organized networks, aimed at improving efficiency, increasing security and reducing risk of malfunction. The basic components of networked sensor-systems will integrate on the same micro-substrate sensing (and when necessary, actuating) devices with local processing capability and modular interconnection techniques, thus providing as much distributed intelligence as possible [1].

The sensing modules will ensure mobility when they do not demand huge communication and processing bandwidths. In the sensor module that we envision the power is wireless received in microwave form, transformed, stored onto a capacitor and carefully managed to ensure the best quality service. In addition to power, the microwaves transmit synchronization and low data rate signals thanks to a simple amplitude modulation scheme of the microwave carrier.

Microwave power transmission is well studied for high power applications [2]. A typical system uses a rectifying antenna (rectenna), to convert RF or microwave energy to DC power. The rectenna combines a dipole or patch antenna, a front-end low-pass filter, a rectifying circuit based on Schottky barrier diodes, and an output low-pass filter. Several units are connected together to form an array covering a large surface. The power conversion efficiency can be as high as 80% [3, 4], but for low power density applications rectenna techniques are not so effective [5], with efficiencies below 50%. As a result, low-power applications like short-range wireless sensors or Radio Frequency Identification (RFID) [6, 7, 8] are able to achieve an operating range limited to 10 m or less.

This paper describes the power and data receiver block for the maximum distance of 30 m from the base station. The expected incoming power is 250 μW, therefore, effective RF-to-DC power conversion and low-power data receiver module are essential. A modified pulse amplitude modulation scheme makes possible a 10 μW power budget for the data recovery circuit, that is equivalent to 4% of the received power in the worst case.

In addition to the circuit described in this paper other basic blocks are being designed and integrated on the same 0.18 μm digital CMOS process. The prototype is based on a multi-chip approach with commercial components for DSP and memory. The blocks library will enable building-up micro-systems with different sensing elements (humidity, temperature, and optical sensor), A/D conversion, RF transmitter and an interface toward low-power DSP and memory units. Section II of this paper describes the sensor platform, section III describes the power conversion and the data recovery circuits, section IV shows the simulation results and section V presents the measured results for the RF front-end.

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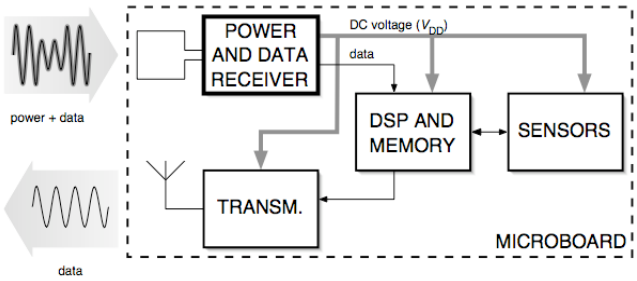

Figure 1. Block diagram of a possible sensor module.

2. SYSTEM DESCRIPTION

Figure 1 shows the block diagram of a possible micro-board sensing module. A patch antenna receives the modulated MW from the base station. The Power and Data Receiver section extracts the power for charging the power capacitor and provides signals for the DSP and Memory block. The Transmitter block includes the up-conversion from base-band to RF, the modulation, the frequency synthesis, and the power amplifier. The DSP and memory perform packet formatting, error control, hop selection, internal clock generation, and power saving algorithms. The block includes an embedded memory array for program and data storage. The Sensors Block includes sensors elements, read-out channels, multifunction interface, and A/D converter.

We assume to use a single patch antenna 10 by 10 cm and we estimate that the minimum power level received by the sensor to provide proper service is 250 μW. In these conditions, in order to comply with the maximum allowable transmitted power output from the base station, as specified by governing agency regulations, the operating range is 30 m from the base station. This range can be extended by considering a number of transmitting base stations and smart antennae. The received power is used to charge an electrolytic capacitor, whose capacitance (5 mF) contains 6 mJ of available energy. The value of the capacitance can be scaled accordingly to the application and higher energy-density capacitors, such as ultracapacitors [9], can be used in case extended range or long-time operation are required. The most power hungry block is the Transmitter, which dissipates 900 μW during transmission, while the overall power dissipation of the other blocks is less than 100 μW. By properly managing the power dissipation of each block, a 0.5% transmission duty-cycle (i.e. the ratio between the average time the Transmitter can be on and the time needed for recharging) is feasible. Similar transmission duty-cycles are achieved in systems where sensors scavenge energy from the environment [1] without this being a limitation when burst transmission is required. In our system we chose the value of the capacitance so that the available energy if enough to transmit the required information (in our design we considered a frame of an image sensor) without waiting for additional recharge.

3. CIRCUIT DESIGN

3.1 Power conversion

Within the present design the wirelesses transmit power must be in a medium-range (30 m). Therefore, it is necessary to optimize the design under low power conditions. Moreover, since the received power is not enough for a continuous operation, the system stores energy in a capacitor instead of delivering it directly to a resistive load as in most of applications. The energy stored onto the power capacitor is used by the sensor platform for data acquisition and transmission to the base station.

Extensive studies and simulations at component level lead to the power extraction and data rectification circuit shown in Figure 2. It consists of an input low-pass filter made by the interconnection of four microstrip lines TL1-TL4, followed by microstrip impedance matching elements TL5 and TL6, Schottky rectifiers D1 and D2, data pass filter R_1 and C_1, and power capacitor C_2. The circuit is realized onto a 31 mil thickness FR-4 substrate with $\varepsilon_r = 4.8$. D1 and D2 are HSMS-2850 type from Agilent Technologies. The schematic does not show the package parasitics, accounted for in the simulations.

TL1-TL4 is a low pass filter with stop band above 5 GHz. TL5 and TL6 match the input impedance of D1 and the one of the low-pass filter stage for maximizing the power delivered to capacitor C_2. V_{SIG} is the extracted data waveform, which is separated from power supply output V_{DD} by D2. R_1 and C_1 implement a low-pass filter for data recovery, and their values are selected to pass 100 kbit/s data while filtering out the 2.45 GHz carrier. Since resistor R_1 dissipates power, its DC current is suitable for a cell of the system capable to perform the same function. For example, a monitor of the received power level necessary for refining the smart antenna directionality can replace R_1. A 5 mF power capacitor C_2 is the value used in the design. However, a larger value can be used with no impact to this RF front circuit design.

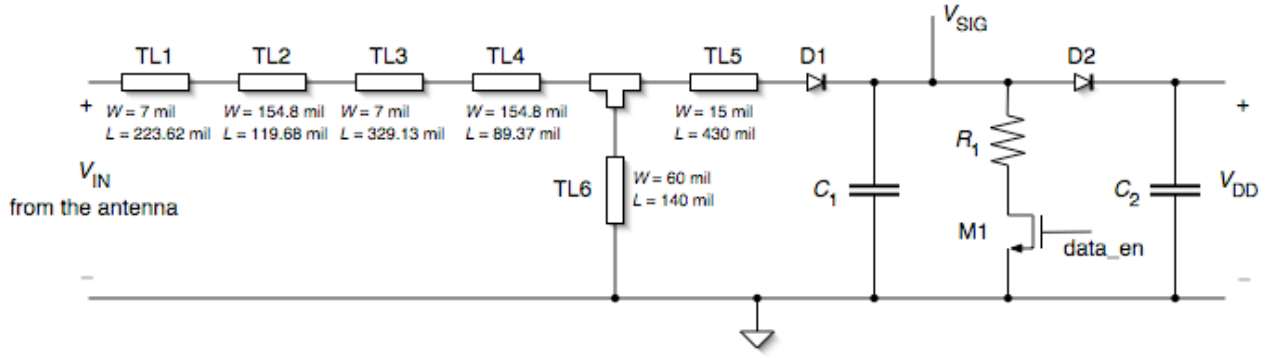

Figure 2. Schematic of the power extraction and data rectification circuit.

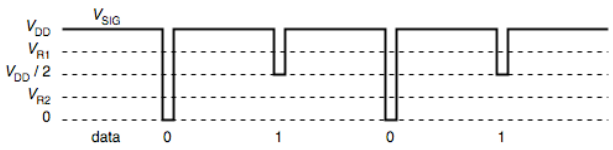

Figure 3. Extracted signal waveform (V_{SIG}).

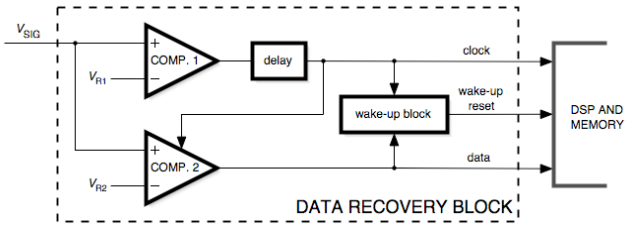

Figure 4. Block diagram of the data recovery module.

3.2 Data recovery

The signal is transmitted using a binary pulse amplitude modulation of the 2.45 GHz carrier. The waveform duty-cycle is 90% to maximize the recharging effect. The high level is about V_{DD}, while the pulse amplitude is $V_{DD}/2$ (corresponding to a logical 1) and 0 (corresponding to 0). The reference voltage V_{R1} is used to generate the clock signal; V_{R2} is used to distinguish the two data voltage levels (0 and $V_{DD}/2$). A possible extracted waveform after full wave rectification is shown in Figure 3 and corresponds to 0101 sequence.

Figure 4 shows the block diagram of the data recovery section. The continuous-time comparator 1 generates the clock signal controlling comparator 2, that extracts data, and the following digital circuit. Since the input signal does not have fast rising and falling times, clock is properly delayed to ensure a right timing.

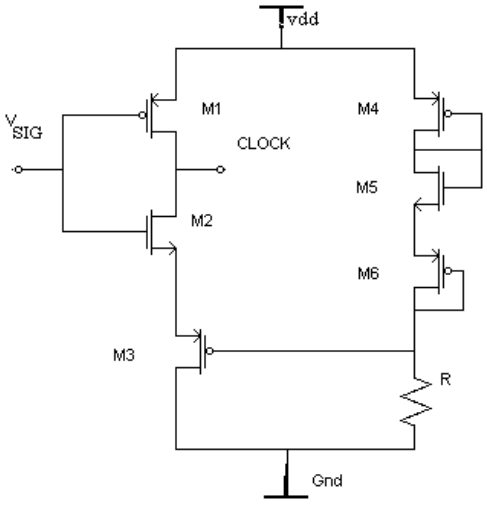

Figure 5. Schematic of comparator 1.

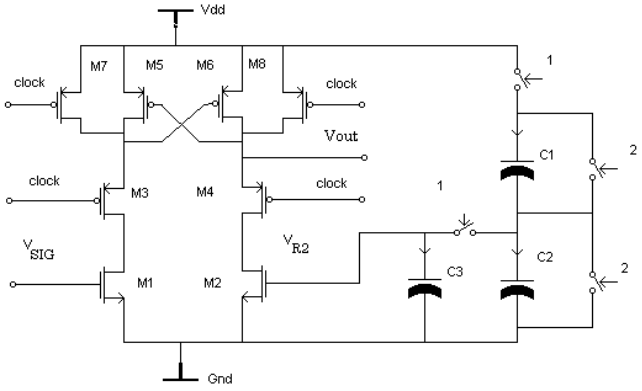

Figure 6. Schematic of comparator 2.

Each sensor has a unique identification number. When the base station start transmitting, it sends a synchronization sequence and a code, which is the identification code of a single sensor (to communicate with a single sensor), or a master-key code (to broadcast to all sensors). When the wake up block receives the sensor identification code (or the master-key code), the DSP wakes up and begins processing the incoming data.

Figure 5 shows the schematic of comparator 1. It is an inverter with controlled threshold voltage (V_{R1}). The threshold is defined by the stacked transistor M3. If V_{DD} is small, the gate of M3 is grounded. When V_{DD} exceeds the limit established by the diode connected transistors M4, M5, M6, the gate of M3 rises, thus increasing the threshold. The value of the resistance R is in the mega-ohm range. Therefore, the DC current in M1-M2 is zero or limited to the current flowing in the bias branch. For low supply voltage the threshold of the comparator is one p-channel plus one n-channel threshold.

Fig 6 shows the schematic of the comparator 2. Since the input signal is larger than 0.1 V, a single latch is enough to achieve the digital result. A switched capacitors divider generates the reference voltage with minimum power dissipation. The reference is $V_{R2} = 0.25\ V_{DD}$. Therefore, a logic 1 corresponding to $0.5\ V_{DD}$ determines a $0.25\ V_{DD}$ input difference. Since V_{DD} ranges from 0.9 to 1.4 V, the latch control is at least 225 mV.

4. SIMULATION RESULTS

4.1 Power conversion

The main features of the power conversion circuit are RF to DC power conversion efficiency and output DC voltage. The goal is maximizing efficiency and achieving an output voltage higher than 1.2 V. Based on the output voltage requirement, the input RF power was selected to be 250 µW (–6 dBm). It has been proved in rectenna design that the RF front end low pass filter following the input antenna serves as a buffer for better impedance matching between the rectifier circuit and antenna and blocks the flow of harmonic energy from the rectifier back to antenna [4]; both effects are crucial for the best efficiency. Figure 7 shows the simulated transient response of output DC voltage levels with the top curve with filter and bottom curve without filter at the specified input RF power, respectively. The case without filter barely meets the voltage requirement, while with the addition of the filter the circuit reaches 1.6 V, clearly demonstrating the effect of the low pass filter.

In the simulation, a smaller capacitor of 100 pF is used, instead of the desired 5 mF value for the final design. The latter capacitance value was designed so that about 50 s is to be used to charge the capacitance to 1.5 V level. However, to simulate the charging process of 5 mF capacitor will take prohibitive simulation time and storage, due to the fact that the charging signal has a frequency of 2.45 GHz, which limits the simulation steps to ns scale. Since the time constant of the charging process is proportional to the capacitor value; a smaller capacitor is used here to demonstrate the final output DC voltage level difference for the two methods.

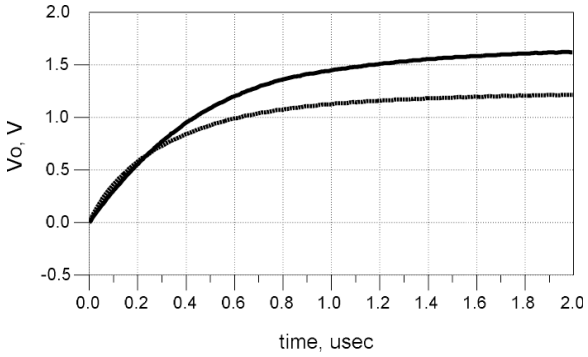

Figure 7. DC voltage and efficiency improvement using the LP filter.

In most rectenna design environment, RF or Microwave power conversion is studied for a resistive load case, and the efficiency is maximized under certain resistive load conditions. However, in our case, the RF energy conversion is a transient process in which the output power capacitor C_2 is charged by the rectified RF energy. Therefore, we have defined the average power conversion efficiency as:

$$\eta = \frac{\text{converted } DC \text{ power}}{\text{available input power}} = \frac{\frac{1}{2}C_2\Delta V^2}{\Delta T} \Big/ P_{IN} \qquad (1)$$

In the above definition, C_2 is the output capacitance, ΔV is the finally charged output DC voltage, ΔT is the rising time when DC voltage goes from 20% to 80% of the final voltage, and P_{IN} is the available RF input power assuming 50 Ω antenna output impedance. Using this definition, the power conversion was simulated against the input power and the result is shown in Figure 8. The efficiency reaches 52% at an input power of 250 μW and peaks at around 500 μW. The DC output voltage is also sweeped against the available RF input power, and the result is shown in Figure 9. The voltage rises with the input power level and flattens out around 500 μW power, corresponding to the peak efficiency at that power level.

Data rectification is another important function this RF front-end circuit needs to implement. Since impedance matching is implemented as microstrip lines, a separate signal and power path design would make the impedance matching difficult, sacrificing the power conversion efficiency. Instead, the two paths are merged so that RF power input is maximized to the rectifier D1 where signal is extracted first and further rectified by D2 to convert energy to DC at the output power capacitor C_2. D1 and D2 are low barrier Schottky diodes with low turn on voltage around 0.2 V, this extra power loss is not significant and has to be tolerated. The transient response of V_{SIG} signal is shown in Figure 10. The top curve (a) shows a 100% modulated input RF wave and the bottom curve shows the rectified data signal.

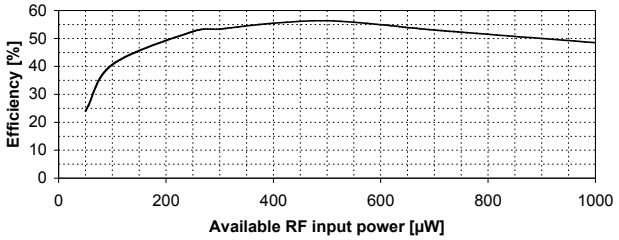

Figure 8. Power conversion efficiency (η) vs. input available RF power.

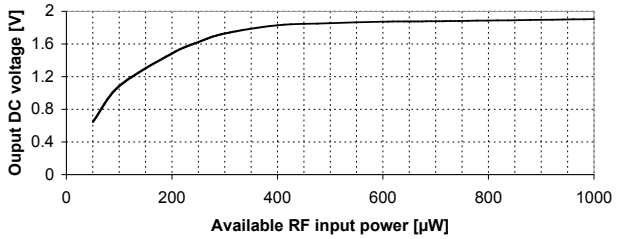

Figure 9. Output DC voltage (V_{DD}) vs. input available RF power.

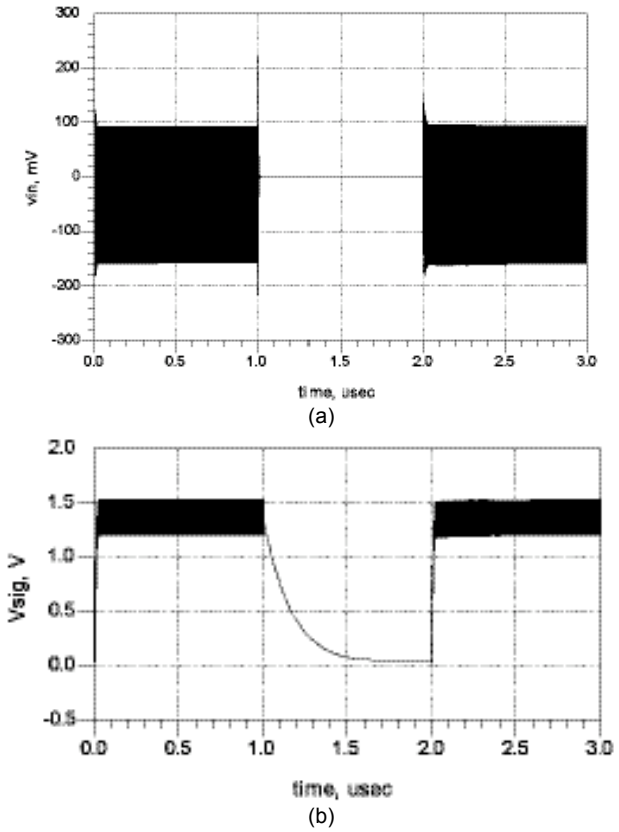

Figure 10. (a) The antenna input waveform (V_{IN}), and (b) the signal waveform (V_{SIG}).

4.2 Data recovery

The circuit has been designed and simulated using a standard CMOS 0.18 µm technology. Figure 11 shows the transient output of the circuit.

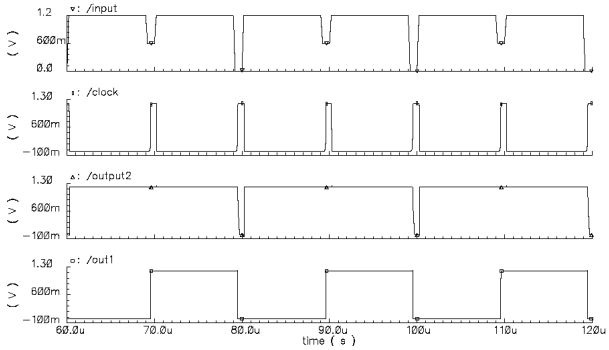

Figure 11. Data recovery module output.

The first waveform is the input signal with 10101 data modulated; the second waveform is the clock signal that is synchronized with the input; the third waveform is the output from the comparator 2 (latch); the last waveform is the final output from the flip-flop, we can see clearly the demodulated data 10101.

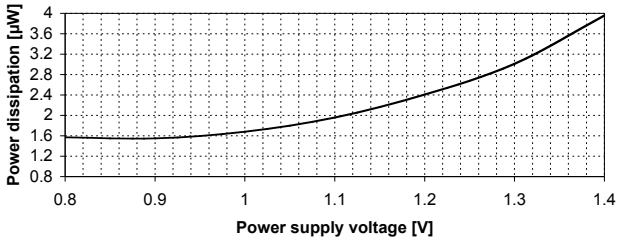

Figure 12. Supply voltage (V_{DD}) vs power dissipation of the data recovery circuit.

The frequency of the input signal is 100 kHz with the delay of 0.2 µs at the edge. As the supply voltage increase, power consumption increase accordingly. The maximum power consumption is around 4 µW. If we include the digital part (register and decoding network), the overall power dissipation is estimated to under 10 µW.

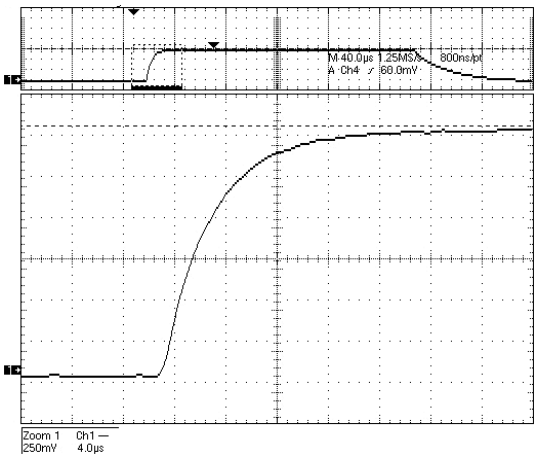

Figure 13. Measurement of the turn-on transient of V_{DD}.

5. EXPERIMENTAL RESULTS

The power extraction and data rectification circuit has been fabricated and tested. The measured DC output voltage at –6 dBm input power is 1.5 V as shown in Figure 13. The picture shows the charging transient for a 1.2 nF capacitor. The maximum voltage is slightly lower with respect to the simulation results due to losses and material dielectric constant variation. The power conversion efficiency calculated using equation (1) is 47%.

6. CONCLUSION

A 2.45 GHz power conversion and data extraction circuit is designed for a wireless autonomous sensor platform. The power conversion converts the RF power to DC power onto a capacitor with a power conversion efficiency of 47% with an input power level of 250 µW. The low power data recovery circuit interfaces with the RF front end to extracts clock and data with a maximum power consumption of 10 µW.

7. ACKNOWLEDGMENTS

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