Advanced Timing Analysis Based on Post-OPC Extraction of Critical Dimensions

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ABSTRACT

While performance specifications are verified before sign-off for a modern nanometer scale design, extensive application of optical proximity correction substantially alters the layout introducing systematic variations to the simulated and verified performance. As a result, actual on-silicon chip performance is quite different from sign-off expectations. This paper presents a new methodology to provide better estimates of on-silicon performance. The technique relies on the extraction of residual OPC errors from placed and routed full chip layouts to derive actual (i.e., calibrated to silicon) CD values that are then used in timing analysis and speed path characterization. This approach is applied to a state-of-the-art microprocessor and contrasted with traditional design flow practices where ideal (i.e., drawn) L_{gate} values are employed, leading to a subsequent lack of predictive power. We present a platform for diagnosing and improving OPC quality on gates with specific functionality such as critical gates or matching transistors. Furthermore, with more accurate timing analysis we highlight the necessity of a *post-OPC verification* embedded design flow, by showing substantial differences in the Si-based timing simulations in terms of significant reordering of speed path criticality and a 36.4% increase in worst-case slack. Extensions of this methodology to multi-layer extraction and timing characterization are also proposed.

Categories and Subject Descriptors

B.7.2 [**Integrated Circuits**]: Design Aids—*layout, verification*; B.8 [**Hardware**]: Performance and reliability—*Performance, analysis and design aids*

General Terms

Design, Algorithms, Performance

Keywords

OPC, layout, process CD, design flow

1. INTRODUCTION AND MOTIVATION

For current and upcoming technology nodes (90, 65, 45 nm and beyond) a fundamental enabler of Moore's Law is the use of resolution enhancement techniques (RET) in optical lithography. While RETs such as phase shift masks and off-axis illumination allow for continuing reduction in integrated circuit critical dimensions (CD), layout distortions are introduced as an undesired consequence due to proximity effects. Complex and costly optical proximity correction (OPC) is deployed to compensate for L_{gate} variations and the loss of pattern fidelity (Figure 1). With these modifications, chip manufacturability and yield are improved but performance is adversely affected. There have been efforts to consider process variations such as gate CD, oxide thickness, metal width and thickness, temperature, voltage, etc., during circuit performance analysis at the design stage but this requires proper modeling of the variabilities [1, 2, 3]. The most common approach to modeling variability, typically aimed at speed/frequency prediction, is based on "worst case scenarios" (corner cases). This approach assumes all transistors are independent and hence yields overly pessimistic simulations, making the design unnecessarily difficult [4, 5]. Other approaches seek to provide more accurate variability modeling by considering its sources. Treated as purely random components, process variations are modeled using a probabilistic framework with effort to accurately model correlations [5, 6].

More than 50% of L_{gate} variation is due to systematic sources [7], which can be modeled accurately once the physical layout is completed. In fact, assumptions about the L_{gate} distribution in Monte Carlo simulations and statistical timing analysis in general, could be made more rigorous by considering realistic systematic contributions (the majority of which arises due to proximity effects) to the overall process variation [8, 9, 10]. With measured data, [8] show a significant systematic intra-chip variability of L_{gate} which leads to large circuit path delay variation. That work estimates the location-dependent L_{gate} variation by classifying the layout patterns within 5 categories; in actuality there are many more relevant scenarios, complicating the approach. References [9, 10] use aerial image process simulations to account for systematic L_{gate} variations, however these simulations are limited to fixed layout patterns and cannot be expanded to full-chip timing analysis. In [11] the authors propose a systematic variation-aware static timing methodology using library-based OPC. However, at the full-chip level OPC features applied to a given library cell will not be identical across all instances and depend largely on neighboring geometries. This approach therefore loses the advantage of model-based OPC, particularly considering those cells with small sizes (in which OPC applied throughout the cell can easily be impacted by neighboring patterns) and high frequency of occurrence on critical paths (e.g., invert-

DAC 2005, June 13–17, 2005, Anaheim, California, USA.

ers, NANDs) sacrificing the accuracy claimed in their static timing analysis.

In this paper we present a methodology for post-OPC embedded static timing analysis by extracting residual OPC errors from a state-of-the-art placed and routed full-chip microprocessor layout and for deriving actual (calibrated to silicon) L_{gate} values. The implementation of this automated flow is achieved through a combination of post-OPC layout back-annotation and selective extraction from the global circuit netlist. This approach improves upon the traditional design flow practices where ideal (drawn) L_{gate} values are employed, which leads to poor performance predictability of the as-fabricated design. When post-OPC L_{gate} values are used, timing analysis results indicate substantial differences in the order of speed path criticality, with the worst-case slack increasing by 36.4%. Pin slacks of critical instances are worsened on average and a larger number of critical cells are reported in terms of both total cell count as well as the number of cell types involved on critical paths.

These results point to the need for adoption of process-based simulation results within the traditional design flow so that design optimization is better targeted and effort is not wasted optimizing paths that are not actually critical in the fabricated part. In addition, this flow can be used by OPC engineers to locate critical layout patterns across the full-chip layout where OPC could not achieve the desired L_{gate} control. Once identified, a calibrated OPC algorithm could then be applied locally to attain large savings on full-chip OPC run time. This is particularly essential in designs with matching transistors (e.g., mixed signal designs, clock generation in microprocessors). Furthermore, this flow can easily identify cells either with high frequency of occurrence in critical paths or with large pin slacks, so that various optimizations such as well-calibrated localized OPC algorithms, multi-threshold voltage assignments, gate sizing, etc., can be applied directly to the full-chip layout to improve overall chip performance. While these optimizations are already applied prior to sign-off, a post-OPC timing analysis will provide more accurate CD data and allow for further improvement.

The organization of the paper is as follows. In the next section, we describe the overall methodology developed to enable post-OPC timing analysis. Section 3 describes our experiments and results based on a leading-edge 90nm microprocessor. Section 4 summarizes our findings and discusses future improvements on the post-OPC layout verifications for a systematic variation-aware timing methodology.

2. OVERVIEW OF METHODOLOGY

CD distortions introduced by proximity effects have a significant impact on circuit performance. OPC is used to compensate for these CD distortions yet it becomes a major source of systematic variability itself. Analysis in [8] demonstrated that systematic intra-chip L_{gate} variability is the main cause of speed degradation for large circuits, especially those with a large number of critical paths and short logic depths. In addition, designers place significant emphasis on fixing worst-case speed paths that are identified in timing simulations based on ***ideal*** L_{gate} values (potentially corner-based) which may be quite misleading in the sub-wavelength lithography regime. Process simulations showing aerial images of printed features are used to check the effectiveness of OPC and can provide accurate L_{gate} predictions after a layout is complete, pointing to the possibility of post-OPC timing verification and OPC re-calibration. This section describes a newly developed methodology as illustrated in Figure 2.

- *Process CD Simulation for Critical Gates.* The starting point of the flow is a post-OPC layout on which process CD simulations can theoretically be performed across the entire chip although this would be very time consuming. The OPC layers used for mask creation are generated based on carefully calibrated optical and resist models for the particular lithographic conditions. In our analysis we focus on the systematic poly gate variation introduced by RETs/OPC; the presented flow could easily be extended to include variation of metal layers as well. We perform a selective process CD simulation only for gates on critical paths as predicted in the full-chip timing analysis, tagging them with a *critical layer*. These tagged critical gates are then extracted along with the peripheral geometries within a certain distance (i.e., the optical diameter, beyond which geometries have no impact for the given optical lithography system) to account for optical interactions from adjacent cells. We do this on a path-by-path basis to facilitate future analysis and diagnosis. We perform aerial image simulations with Mentor Graphics Calibre RET tools for each of the critical paths, and for simplicity, the Si-based CDs are extracted and defined as the dimension at the center point for each transistor. Each process CD value is identified with the GDS coordinates of the corresponding transistor which are used to map process CDs back to the circuit netlist.
- *Library Re-characterization.* This step updates the cell timing library with Si-based process CDs by creating a *location-aware* SPICE netlist for each cell. After the process CDs for critical gates are found and back-annotated, the original library is expanded with re-characterized cells. Each transistor is identified by its lower-left coordinates relative to the origin point of the cell. The origin point is determined by the cell's placement orientation and the relative coordinates are calculated with additional info on gate geometry. A special LVS is performed to extract the location of each transistor within a cell in the library. After that, the L_{gate} values in the SPICE netlists are modified with the extracted Si-based process CDs. Finally, SPICE simulations are performed for timing re-characterizations to account for the impact of systematic L_{gate} variations. During the cell library characterization, input capacitance changes due to gate CD variations are also considered. These re-characterized cells, corresponding to their locations and distinguished by cell names, are combined with a typical cell library for timing analysis.
- *Static Timing Analysis with Process CDs.* The global chip netlist is modified to map to the expanded cell library. Then a full-chip timing analysis is performed using commercial tools and the top critical paths are reported. These critical paths may include cells that were not re-characterized in the previous step (i.e., they are on paths that the original pre-OPC timing analysis did not flag as critical) in which case re-characterization of newly critical cells will be necessary.
- *Results Comparison with Traditional Timing Analysis.* Timing analysis results based on process-simulated CDs

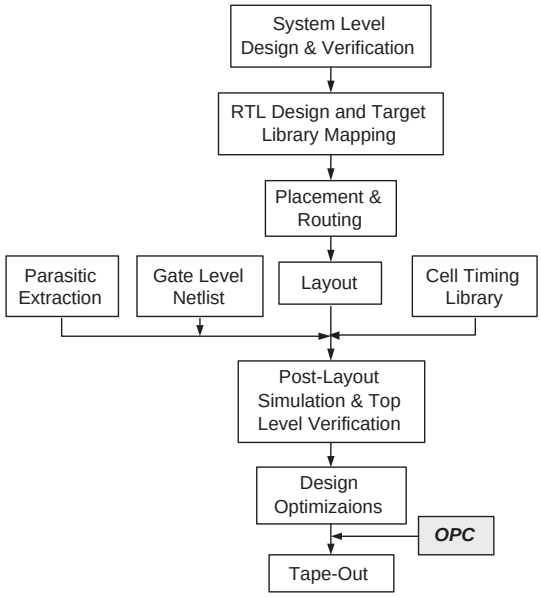


Figure 1: Typical design flow in sub-micron VLSI design.

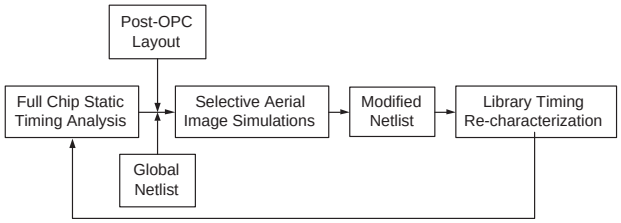


Figure 2: Methodology overview.

are compared with those simulated in the traditional flow with *ideal* gate CDs at typical operating conditions. We choose to make comparisons at the typical process corner rather than the worst process corner to avoid the overly pessimistic worst-case process corner and also since post-OPC CD extractions are performed at best focus conditions, corresponding to a typical process. Therefore, our goal is to determine whether the systematic L_{gate} variations introduced by RET/OPC have a significant impact on typical corner performance.

3. EXPERIMENTS AND RESULTS

We focus on a state-of-the-art microprocessor design in 90 nm technology, using a 193nm optical lithography system. The optical diameter outside of which neighboring geometries have no impact, is set as 4 μm based on experimental results. Due to newly discovered critical cells in each timing analysis with Si-based process CDs, three iterations of cell timing re-characterizations are performed with runtime of approximately three hours per iteration. In the final speed path report, under 2% of total critical cells have not been re-characterized using their extracted CDs; these cells appear only in paths with lower critical ordering. The total runtime for this flow is kept low due to the following: (1) only a small subset of all instances ($\sim$0.5%) are selected for post-OPC process CD simulations; (2) process

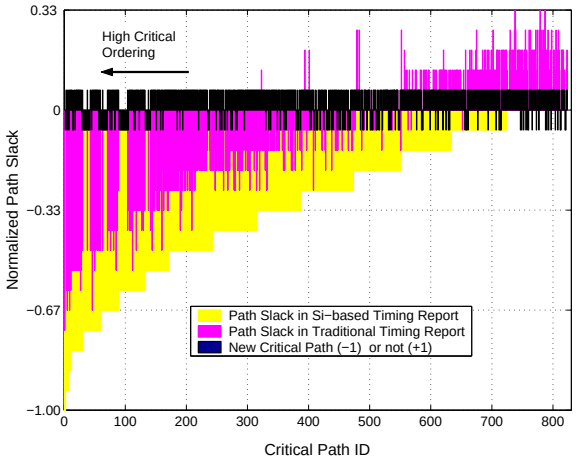


Figure 3: Critical path reordering.

CD simulations for each of the critical paths, as well as timing re-characterization for critical cells, is done in parallel; and (3) most cells on critical paths are simple, such as inverters and MUXes, so that little runtime for cell timing re-characterizations is required. In the experimental results below we outline the need for a post-OPC timing verification design flow with the potential for re-optimization or further OPC assignment. This flow can be supported with a fast and localized OPC assignment algorithm; for each design optimization requiring layout modification, the OPC layer will be changed although only slightly. With the majority of the layout geometries remaining the same, there is no need to regenerate OPC patterns for the bulk of features and thus incremental OPC capabilities are desirable.

3.1 Critical Paths Reordering

We define *critical paths* as paths with *slack* ≤ 0. These paths are rank ordered with the most critical ones first and we assign path IDs according to this ordering (e.g., the most critical path is path ID 1). The experimental results show that in general the Si-based timing report lists more paths (2.7X) as critical than the ideal L_{gate} based timing report, with average path slacks worsened by 24.4%. Figure 3 shows the slack distributions for critical paths from the Si-based timing report and the traditional timing report, and also provides a binary indicator with value +1 meaning that the path appears in both of timing reports while a value of −1 indicates that the specified path only appears in the Si-based timing report. The y-axis relates normalized path slack where the slack of the most critical path in the Si-based timing report is the reference value. In general, we observe more negative slack paths in the Si-based timing report. A considerable number of paths with high critical ordering are not reported in the traditional timing analysis (indicated as −1). We now discuss these paths separately based on whether they appear in both reports (old paths) or only in the Si-based timing report (new paths).

- *Old Paths.* For paths existing in both timing reports, we examine the critical ordering difference. The sign (negative/positive) of the critical ordering difference indicates the shifting direction (more/less critical, respectively) of that critical path in the Si-based timing report compared to the traditional timing report, while the absolute value indicates how many paths it

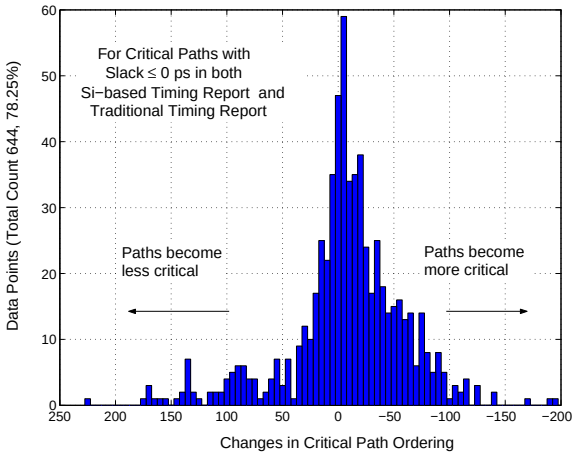


Figure 4: Reordering of critical paths.

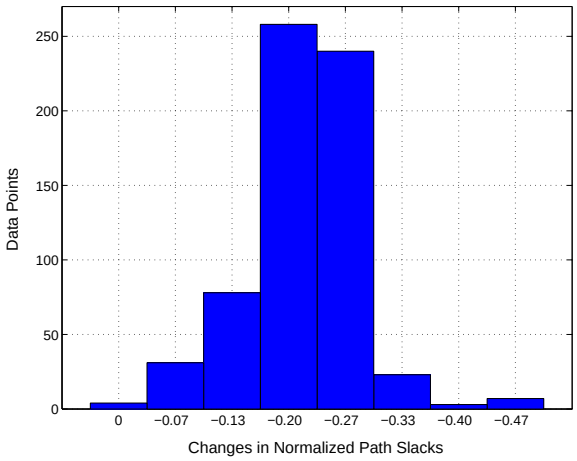


Figure 5: Worsened slacks for *old* critical paths.

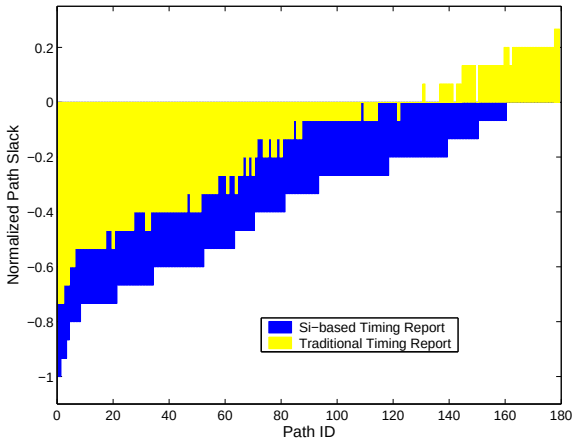


Figure 6: Slacks for *new* critical paths.

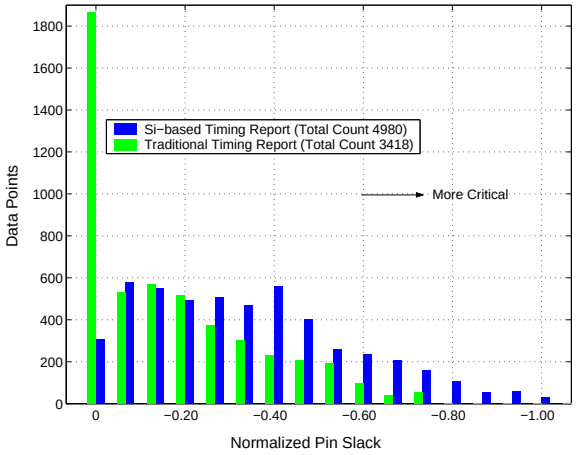


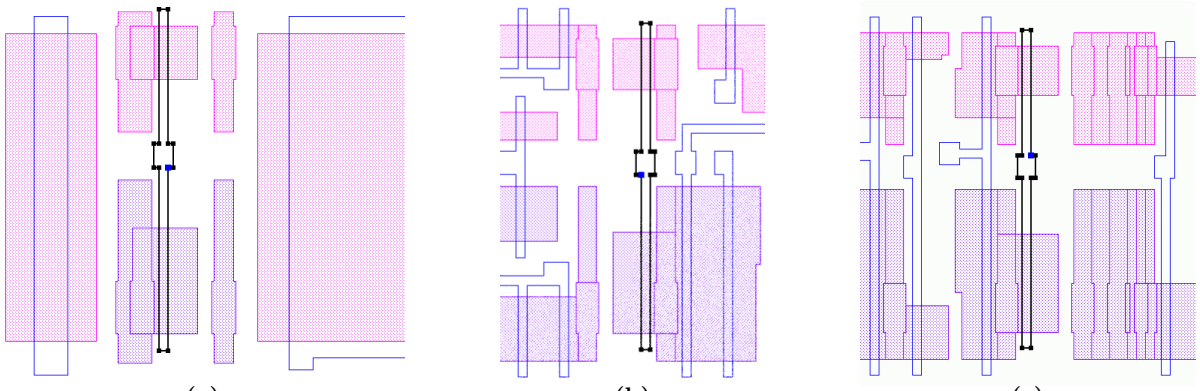
Figure 7: Pin slacks for critical cells.

passes to achieve the new critical ordering. As shown in Figure 4 the range of critical ordering difference is between −195 and +224, implying that paths become up to 195 paths more critical and 224 paths less critical, respectively. Even for paths with positive changes (less critical overall) they typically become more critical in the sense that their absolute slack is often worse than that found in the traditional timing report. The path slack changes are shown in Figure 5, where the worst case slack is increased by 36.4%, and the average slack change is 0.22 with a maximum shift of 0.47 (again these values are normalized to the worst-case slack observed in the Si-based timing report).

- *New Paths.* When post-OPC CDs are used, 21.8% new critical paths are identified. Some of these new paths are highly critical with large slack violations according to the post-OPC analysis (see Figure 6). Path slacks in new path cases are worsened by 0.22 (normalized) on average. As a result, using the traditional timing analysis as a guideline for design optimization will be very misleading in that certain paths will be not be considered for resizing, etc. although they will actually be critical post-fabrication.

3.2 Tracing for Critical Cells

To investigate whether specific cells consistently appear on critical paths, and thus are good candidates for cell redesign and/or close attention during OPC assignment, we define critical cells as instances with pin slack ≤ 0 and compare pin slacks and the top ten most frequently used critical cells under the two timing analysis schemes. As indicated in Figure 7, the distribution of pin slack for critical cells is wider in the Si-based timing report, with a shift to larger slack violations on average. More cells become critical in terms of the total number (increasing by 45.7%) as well as cell types (increasing by 12.7%). These results indicate that more design effort on optimization and cost will be involved. By identifying the most frequently used critical cells, more effort may be placed on optimizing the delay of these cells, and better CD control may be achieved by using a more OPC-friendly cell layout. We find that 53% and 50% of total critical cells in traditional and Si-based timing analysis, respectively, are made up of the top ten critical cell types. As shown in Figure 8 and Figure 9 we observe that the ordering of the top ten most frequently used critical cell types changes slightly while the average pin slack becomes 42.7% worse in the post-OPC analysis. From these results we conclude that library-level design optimizations should be made based on a Si-based analysis.



(a) CD error: 7.33X **(b) 6X** **(c) 1X**

Figure 11: Impact of environment on L_{gate} residuals of the same gate. The error is extracted for the P-transistor only in the highlighted inverter and is normalized to (c).

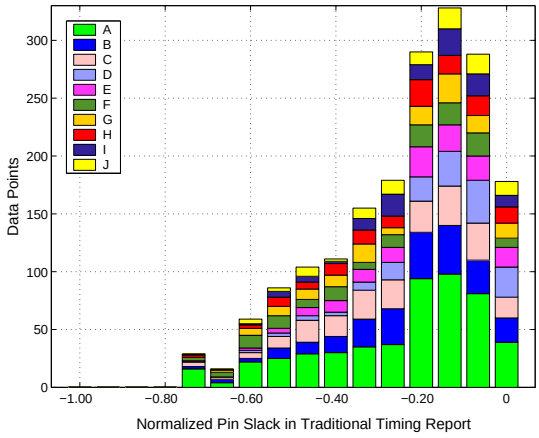


Figure 8: Top ten most frequently used cells in ideal L_{gate} based timing report.

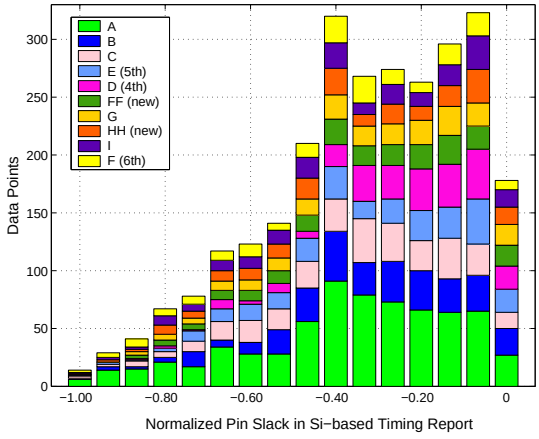


Figure 9: Top ten most frequently used cells in Si-based timing report.

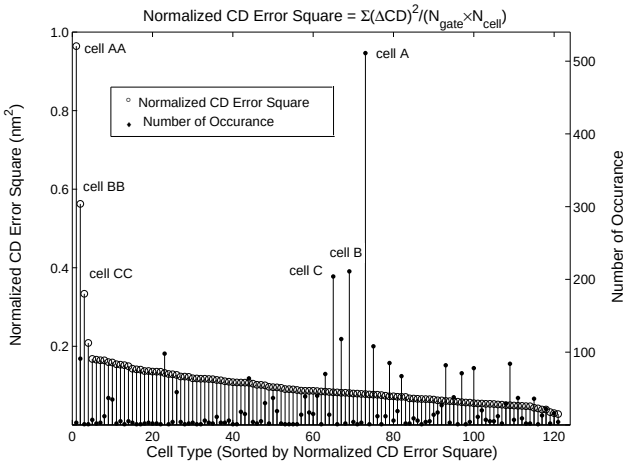


Figure 10: Normalized L_{gate} residual for cells on critical paths.

3.3 OPC-Driven Analysis

Model-based OPC corrects the layout on a point-by-point basis, considering all neighboring features as well as the complex interactions between the stepper and mask. By decomposing the edges of each feature into small fragments, the overall OPC quality can be improved through more fine-grained edge movements. Such movements for each fragment are constrained by neighboring geometries, and the use of a given prioritization scheme for each fragment may limit the convergence of the overall OPC correction. For instance, the number of iterations of edge movements required to converge below the OPC-specified residual error might vary from fragment to fragment. This issue can be dealt with by adjusting the priority scheme based on the identification of these problematic layout patterns. Our flow provides a way to compute the normalized OPC residuals for instances on critical paths and associate them with that cell's occurrence frequency. As shown in Figure 10 there are several cells with both large CD errors and a high frequency of occurrence. In these cases either customized OPC recipes can be created or cell layout patterns could be adjusted to improve the overall printability.

To further diagnose the impact of neighboring features, we examine layout patterns that cause gates to exhibit large CD variations after OPC is applied. Figure 11 shows an example of the impact of environment for three instances of a single (identical) gate polygon in terms of L_{gate} errors. The highlighted gate is an inverter and we focus on the P-transistor (bottom device). Two heuristic rules to enhance manufacturability are often applied: (1) use of a single pitch on the critical layer, and (2) avoidance of non-rectilinear shapes (e.g., L's or T's). This is reflected in Figure 11. The layout in (a) is undesirable due to the large decoupling capacitances nearby while (b) is also poor due to the many L shapes in neighboring poly. For the same inverter layout in (c) the neighborhood around the P-transistor leads to better printability, reducing the L_{gate} errors (normalized) by 7.33X compared to (a).

4. CONCLUSIONS AND ONGOING RESEARCH

An automated flow for post-OPC performance verification is presented. Experimental results on a 90nm microprocessor show significant changes in the timing analysis compared to the traditional methodology of performing final timing analysis before OPC application. The number of critical paths increased by 170% while the worst-case slack violation increased by 36.4%. Among all critical paths found in the post-OPC flow, 21.8% were not reported in the traditional timing analysis. These changes demonstrate that traditional performance analyses are no longer valid in nanometer-scale designs that rely on complex resolution enhancement technologies.

A post-OPC performance verification design flow can enable process variation-aware design optimization as well as drive tradeoffs when significant variability is unavoidable. Using the framework presented in this paper, one design flow based on post-OPC verification with only slight modifications to the traditional flow is given by Figure 12. The post-OPC process CD extraction is performed at the same stage when interconnect parasitics are extracted and back-annotated. In this way the large systematic gate CD variations due to RET/OPC are taken into account during static timing analysis to achieve more accurate performance predictions. The methodology described in this paper is based on the ability to tag critical gates such as those on critical paths or matching gates so that specific corrections can be applied to these gates to achieve better CD control rather than attempting to reduce gate CD variation in all scenarios. This type of back-annotation can be easily extended to the metal and contact layers in order to enable RC extraction based on Si-based post-OPC dimensions. Integrating the OPC step into the design flow effectively will allow design-time optimizations to be aware of the manufacturing process and achieve improved performance and yields in the final as-fabricated design.

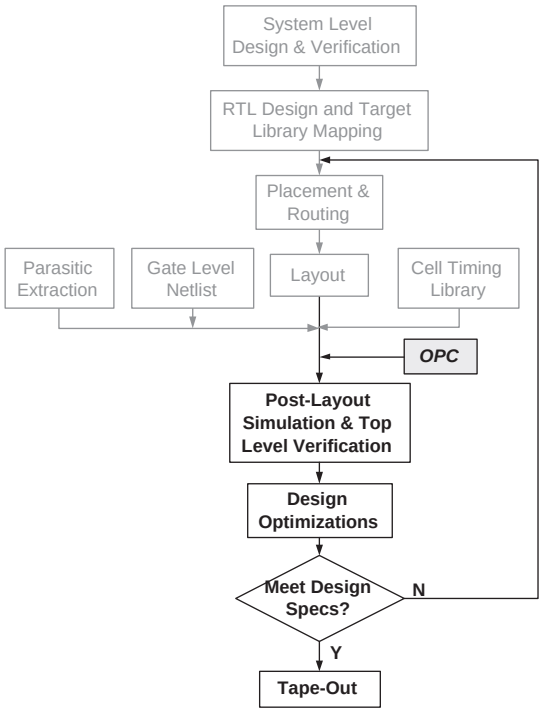


Figure 12: Design flow with post-OPC verification.

5. ACKNOWLEDGMENTS

This work was supported by the Semiconductor Research Corporation and Advanced Micro Devices. The authors would like to thank Norma Rodriguez, Chris Spence, Cyrus Tabery, Marius Evers, Darin Chan, William Voegtli and Robert Williams of AMD for helpful discussions.

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