NASFLOW, a Simulation Tool for Silicon Technology Development

D. David Forsythe, Atul P. Agarwal, Chune-Sin Yeh,
Sheldon Aronowitz, Bhaskar Gadepally

National Semiconductor Corporation
Santa Clara, CA 95052

ABSTRACT

A simulation system is described for linking two-dimensional simulators for process and device to a parameter extraction program, for the purpose of generating artificial parameters for the circuit analysis program, NASPICE. A key feature of the system is that it operates under the control of a shell program which offers a simple and easy to use interface to the user. Results of an initial development using the program sequence

SUPRA = > PISCES = > CADPET = > NASPICE

are described. Good correlation was obtained between system generated drain characteristics and silicon for both N and P-channel MOS transistors, and similarly for CMOS DC transfer characteristics.

I. INTRODUCTION

The industry has long needed a simulation tool for predicting electrical behaviour of the final product directly from the process flow. Enabling the process development and circuit design to proceed in parallel would have a major impact on time to market, and quality of the final product. Delays caused by long development process cycles would be shortened substantially. Silicon runs would be required primarily to maintain calibration of the simulator, rather than exploring all possible process combinations, with a considerable saving of both time and resources. A tool of this kind would also be applicable to process line monitoring, and to examining the effects of introducing novel or undeveloped fabrication technologies.

One approach to this problem [1] has been to set up a linked system of analytical simulators. However, in recent years a number of powerful one and two-dimensional process and device simulators have become available and somewhat standardized. It would be desirable to integrate these programs into a system for simulating the entire product development sequence from process specification to circuit design and evaluation. The industry has been studying methods [2] of standardizing output data from the various process and device simulators in order to facilitate communication between them. This paper, however, is concerned with a particular solution to the problem of simulating technology development.

Examples of process simulators are the one-dimensional SUPREM-3 [3], and the two-dimensional SUPRA [4] and SUPREM-4, all from Stanford University. Device simulators include PISCES [5][6] from Stanford, and MINIMOS [7] from the University of Vienna. For simulating real non-planar devices two-dimensional simulators are of primary interest, although SUPREM-3 cannot be disregarded as it is the most accurate of the available process simulators. However using SUPREM-3 to supply device structures to PISCES or MINIMOS is awkward because of the need to supply multiple one-dimensional SUPREM-3 simulations for different regions of the structure, and the need to provide lateral diffusions at the boundaries of the one-dimensional regions. SUPREM-4, though two-dimensional, is at an early stage of development, is limited in the simulation features provided, and not really ready for general use. MINIMOS is specialized to handling MOS devices, but does this well, including such advanced features as avalanche [8] and energy balance [9]. PISCES, alternatively, can be used for both MOS and bipolar, but is not as advanced as MINIMOS in the areas described. Therefore, for simulating real non-planar devices it is best to use SUPRA, or SUPRA and SUPREM-3 in combination to generate the device structure from process flow; and PISCES or MINIMOS to analyze the device structure.

The sophisticated two-dimensional numerical simulators discussed here use large amounts of computer time and memory capacity, and can only be used for analyzing single devices. Therefore, while offering a great deal more potential for simulation accuracy and predictive ability than the simple analytic models used in Berkeley SPICE and its derivatives, they are not directly suitable for circuit simulation where hundred's and thousand's of devices may be run in a single simulation. This limitation can be overcome by integrating the two-dimensional simulators into an overall system as described, that is by using them in place of processed silicon wafers to generate device I-V characteristics from which model parameters for SPICE can be extracted. Because wafer fabrication is expensive and cycle times are long, this has the potential both of speeding development times for new technology, and reducing development costs. Furthermore, circuit and process design can proceed in parallel since numerical simulators can be used to generate usable circuit model parameters for the latest process iteration without waiting for confirming silicon runs.

NASFLOW accomplishes this by linking together process, device, parameter extraction, and circuit simulation programs in a single system. For the initial investigation the linking sequence was

SUPRA = > PISCES = > CADPET = > NASPICE

where CADPET is a parameter extraction program, and NASPICE a circuit simulator derived from Berkeley

SPICE. CADPET and NASPICE are proprietary to National Semiconductor. A key feature of the NASFLOW system is that it runs under the control of a shell program which takes care of details such as writing the input files and controlling the linking sequence. The system presents a user-friendly interface to the user and is simple, quick, and convenient to operate.

2. DESCRIPTION

Figure 1 shows a detailed flow sequence for the NASFLOW system. In this figure data flow is shown as a solid arrow, control flow is shown dotted. Circles are used to represent programs; data files are shown as rectangles. The main linking sequence is shown from left to right down the center of the diagram. The NASFLOW shell program is shown at the top taking data from the input menu, generating the PISCES input file, and controlling the programs SUPRA, PISCES, and CADPET. Optional graphics monitors are shown along the bottom row of the diagram. These can be used to display useful data from the programs and monitor the operation as needed.

Using the data from its input file, SUPRA generates a complete two-dimensional device structure as indicated in the monitor diagram, and shown as a more detailed example in Figure 2 for N-channel. This N-channel file, and the P-channel file discussed later in this paper form the two halves of a CMOS process. The SUPRA input file contains a complete run description for the process. All process steps are included, both those which affect the SUPRA simulation directly, and others such as photoresist processing, which are included as comments. Masking limits which define photoresist edges and are used to position gate, contacts, dielectric layers, implants and diffusions are included in the input file. Although the graphics data contains a complete description of the device including dielectric layers, polysilicon, and metal, only the diffusion data in bulk silicon is transmitted to the SUPRA output file for passing on to PISCES.

Figure 2 also shows the As drain and source diffusions, the polysilicon gate, source and drain metal, and the field and gate oxide structures for the device. Doping contours display the doping distribution in the bulk silicon, which is the only information transmitted when linking to PISCES. Note the P-well junction indicated by a dotted line, and the field doping diffusion.

Referring again to Figure 1, the NASFLOW shell program interprets the data from the menu, which in the initial version was simply a file, generates an input file for PISCES, and then initiates the PISCES run. PISCES, as specified in its input file, calls the two files containing the doping distribution from SUPRA, sets up its own grid and device structure, performs an initial solution, and then solves for the I-V characteristics specified in the input file.

Figure 3 shows the device structure generated by PISCES for the minimum nominal channel length of 1.6 micron, which has an Leff as shown of 1.2 micron. The doping distribution passed through from SUPRA is shown in the figure; the gate, source, drain, P-well, and substrate electrodes have been re-specified in the PISCES input file and are included.

Figure 4 shows a vertical doping cross-section through mid-channel of the N-channel device generated by PISCES. In this figure the P-well junction, and the critical surface doping at the center of the channel which determines device Vth, can be clearly seen. There is some loss of definition in the profile when passing from SUPRA to PISCES but the effect on accuracy of the overall simulation is negligible.

For P-channel MOS devices the sequence is similar. Figure 5 shows the P-channel structure generated by PISCES for the minimum 1.6 micron channel length device. In this case the SUPRA masking limits were adjusted to maintain Leff = 1.05 micron, required to match the processed wafer.

Referring once again to the NASFLOW flow sequence diagram in Figure 1, we see that in addition to its graphics monitor output, which can serve as a short loop check on the accuracy of the SUPRA = > PISCES simulation with respect to silicon, PISCES generates I-V data in the exact format required for input to CADPET. Separate CADPET files are generated for N and P-channel. Each file contains I-V data for all the N or P-channel geometries being simulated, which consists of various combinations of gate characteristics Ids vs Vgs, and drain characteristics Ids vs Vds with Vgs as a parameter, which are required to properly characterize the device. Normally the I-V data for CADPET is generated by direct characterization of silicon; in this case the data comes from PISCES.

CADPET performs a parameter extraction and optimization on the complete data set for either N or P-channel, each set including all geometries for that device type. The extracted parameters are sent to a NASPICE model file as indicated in Figure 1, and are also used in CADPET's internal model equations, identical to those in NASPICE for the particular model used, to generate a set of drain and gate characteristics. These CADPET generated characteristics are displayed on the CADPET graphics monitor as shown, and compared with similar characteristics from PISCES. This enables the user to gauge the accuracy of the CADPET extraction and optimization.

As indicated in the flow sequence (see Figure 1) the NASPICE model file provides the process-related input to NASPICE, which in combination with the circuit description in the NASPICE circuit file, provides the data required by NASPICE to perform a circuit simulation.

3. RESULTS

As mentioned previously, I-V characteristics displayed by the PISCES graphics monitor, and indicated in the NASFLOW flow sequence in Figure 1, can be used for short loop monitoring of the SUPRA = > PISCES combination, by comparing with measured data from silicon. The results of such a comparison are shown in Figure 6 which consists of drain characteristics for a W/L = 37.5/1.6 micron N-channel test device. As indicated in the key, the PISCES output is shown as a solid line; the silicon data is indicated as a series of black dots. Figure 7 shows similar results for the longer N-channel device, W/L = 37.5/5.6 micron. Likewise for P-channel, Figure 8 shows a drain characteristics comparison for the short channel W/L = 37.5/1.6 micron; a similar match was obtained for W/L = 37.5/5.6 micron. It is apparent that the drain characteristics fit for the short loop comparison (SUPRA = > PISCES vs silicon) is excellent in all cases.

With the SUPRA = > PISCES combination calibrated using the short loop comparison, a correctly formatted I-V file was sent to CADPET for parameter extraction and

optimization. A typical graphics monitor output from CADPET is shown in Figure 9 for W/L = 37.5/1.6 micron N-channel. The CADPET calculated characteristics, equivalent to NASPICE generated characteristics and based on the same model equations, are shown as a solid line and indicated in the key as "IMOB33" (the name of the model equations). The PISCES data is indicated as a series of asterisks.

The average error for each extraction is printed at the bottom of each graph. For the W/L = 37.5/1.6 N-channel extraction plotted in Figure 9, the drain characteristic error was 4.28%, the gate characteristic error was 2.50%. The largest error encountered in this set of extractions from PISCES data was 5.07%. In CADPET the error is calculated as the root-mean-square average over each set of characteristics of the ratio "deviation/input", where "deviation" is the difference between "input" from PISCES and the "output" from CADPET calculated at each point and taken as a percentage. Error as percent of reading is a severe criterion for measuring quality of fit since small deviations at the bottom of the plot will make a large contribution to the average error.

Once the CADPET extraction had been completed for both N-channel and P-channel, it seemed logical to close the loop around the entire NASFLOW sequence shown in Figure 1. That is to use the parameters generated by CADPET, and NASPICE to simulate a single MOS transistor; then compare the drain characteristics generated by NASPICE with the original silicon values. The results are shown in Figures 10 and 11 for the same minimum channel length geometries used previously; that is W/L = 37.5/1.6 micron N-channel and P-channel. As indicated in the key the solid lines represent NASPICE output; the black dots represent the same silicon data shown previously in Figures 6 and 8, and compared against PISCES output. The results are very good, and confirm that all four elements of the NASFLOW sequence, SUPRA, PISCES, CADPET, and NASPICE are functioning correctly and accurately.

As further confirmation, a simple CMOS inverter was set up using individual N and P-channel test-pattern transistors connected together through a probe card. Obviously an inverter fabricated in this manner will have excessive shunting capacitance, and poor AC response. However, the intention was simply to examine DC behaviour, specifically the transfer characteristic, and compare with results from NASPICE. Figure 12 shows a comparison between NASPICE and silicon for an inverter constructed with W/L = 37.5/1.6 micron transistors for both N and P-channel. Again NASPICE data is shown as a solid line, silicon data as black dots; and it is apparent that agreement between the two is very good.

CONCLUSION

NASFLOW, a system linking two-dimensional simulators for process and device to a parameter extraction program, and operating under the control of a shell program which offers a simple interface to the user, provides a powerful, quick, and convenient tool for generating artificial parameters for the circuit analysis program NASPICE. Simulated drain and CMOS DC transfer characteristics generated as part of an initial development using the program sequence

SUPRA = > PISCES = > CADPET = > NASPICE

showed good correlation with silicon for both N and P-channel.

ACKNOWLEDGEMENTS

This project owes a great deal to Randy Parker, Jim Hogan, and Wayne Schwartz who have provided help and encouragement, and above all an environment in which the project could succeed. Special thanks go to Scott Irving for providing the simulation files and experimental data so essential at the beginning of the project, and for valuable help and advice throughout. Also thanks to David Yu for the device measurements.

REFERENCES

[1] Andrzej J. Strojwas, Stephen W. Director, "The Process Engineer's Workbench", IEEE Journal of Solid-State Circuits, Vol. SC-23, No. 2, April 1988.

[2] Steve G. Duvall, "An Interchange Format for Process and Device Simulation", IEEE Trans. CAD, Vol. CAD-7, No. 7, pp. 741-754, July 1988.

[3] C.P. Ho, S.E. Hansen, and P.M. Fahey, "SUPREM III - A Program for Integrated Circuit Process Modeling and Simulation", Technical Report No. SEL84-001, Stanford Electronics Laboratories, Stanford University, Stanford, Calif., July 1984.

[4] D. Chin, M.R. Kump, and R.W. Dutton, "SUPRA: Stanford University Process Analysis Program", Stanford University Laboratories, Stanford University, Stanford, Calif., July 1981.

[5] M.R. Pinto, C.S. Rafferty, H.R. Yeager, and R.W. Dutton, "PISCES II: Poisson and Continuity Equation Solver", Stanford University Technical Report, Stanford University, Stanford, Calif., Copyright 1984.

[6] M.R. Pinto, C.S. Rafferty, H.R. Yeager, and R.W. Dutton, "PISCES IIB Supplementary Report", Stanford University Technical Report, Stanford University, Stanford, Calif., Copyright 1985.

[7] S. Selberherr, A. Schutz, H. Potzl, "MINIMOS - A Two-Dimensional Transistor Analyzer", IEEE ED-27, pp. 1770-1780, (1980)

[8] A. Schutz, S. Selberherr, H. Potzl, "A Numerical Model of the Avalanche Effect in MOS-Transistors", Solid-State Electronics 25, pp. 177-183, (1982)

[9] W. Hansch, S. Selberherr, "MINIMOS 3: A MOSFET Simulator that Includes Energy Balance", IEEE ED-34, pp. 1074-1078, (1987)

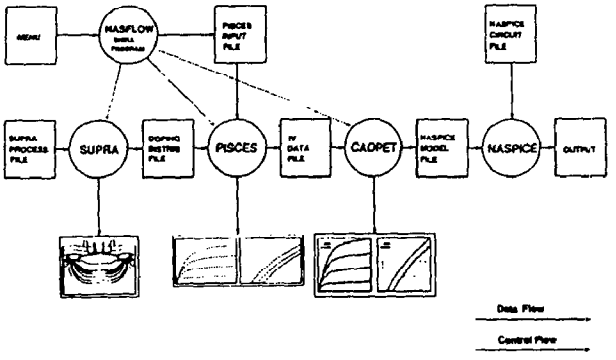

Figure 1 Flow diagram for complete NASFLOW system.

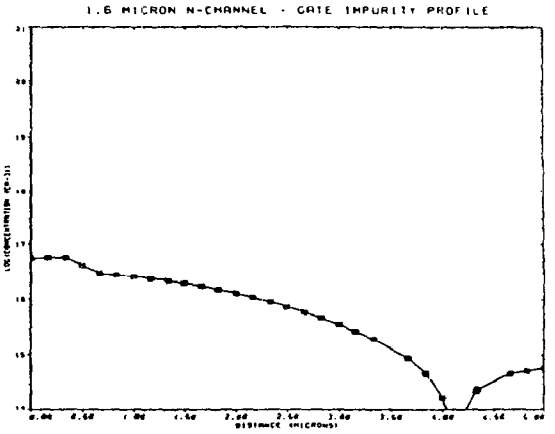

Figure 4 Doping cross-section at center of N-channel device after simulation by PISCES.

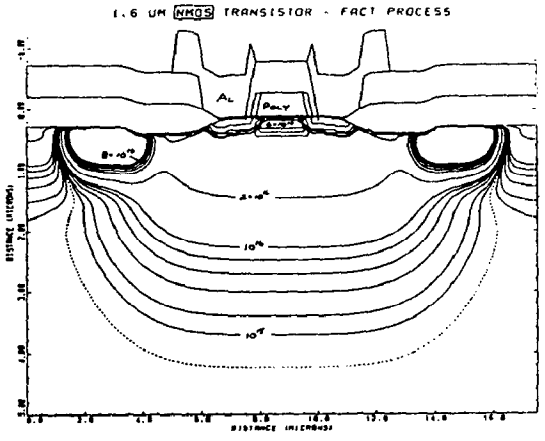

Figure 2 N-channel device cross-section generated by SUPRA.

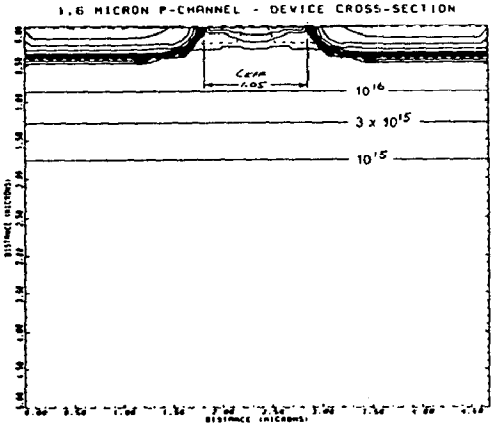

Figure 5 P-channel device cross-section generated by PISCES for minimum 1.6 micron channel length device. Leff = 1.05 micron.

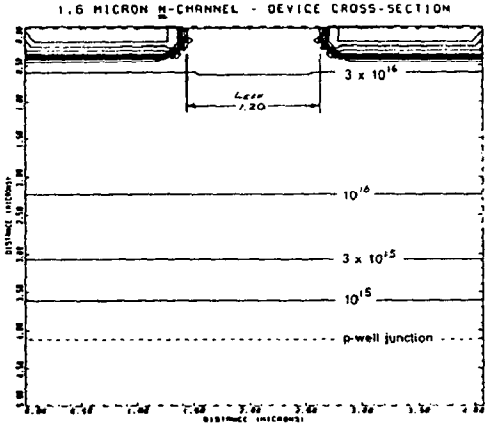

Figure 3 N-channel device cross-section generated by PISCES for minimum 1.6 micron channel length device. Leff = 1.2 micron.

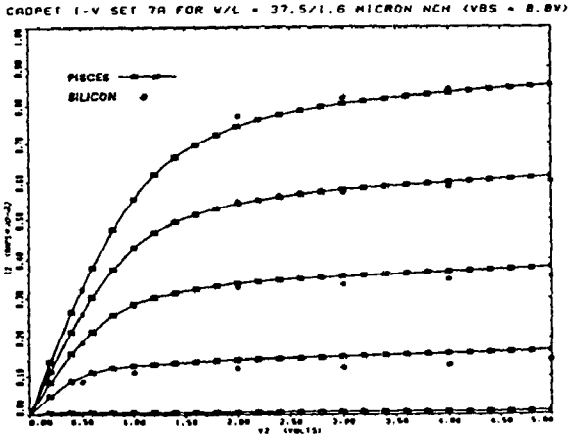

Figure 6 Drain characteristics generated by PISCES for minimum channel length N-channel device, W/L = 37.5/1.6 micron, showing comparison with silicon.

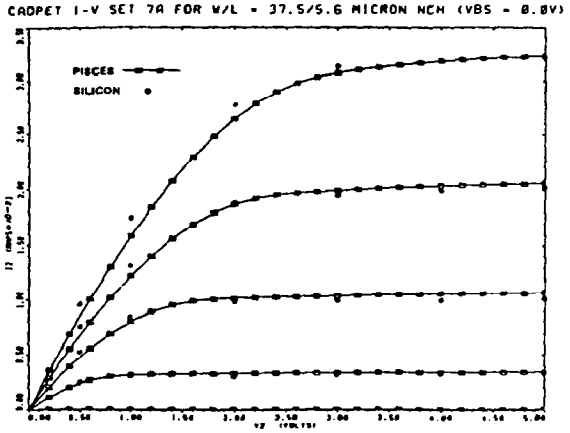

Figure 7 Drain characteristics generated by PISCES for W/L = 37.5/5.6 micron N-channel device, showing comparison with silicon.

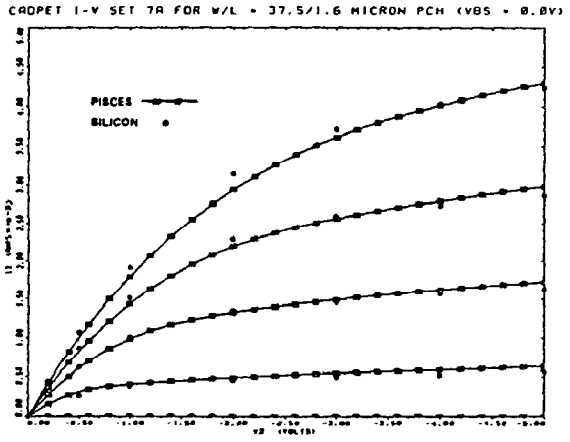

Figure 8 Drain characteristics generated by PISCES for minimum channel length P-channel device, W/L = 37.5/1.6 micron, showing comparison with silicon.

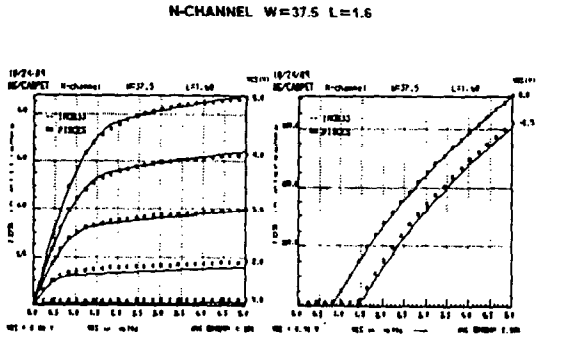

Figure 9 CADPET graphics monitor showing quality of fit obtained for W/L = 37.5/1.6 micron N-channel device.

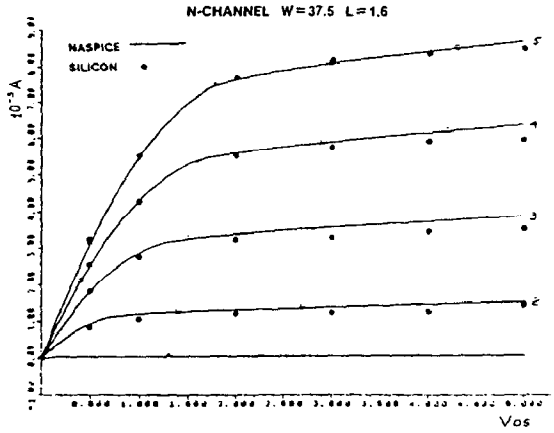

Figure 10 NASPICE generated output for single N-channel transistor (W/L = 37.5/1.6 micron) showing comparison with silicon.

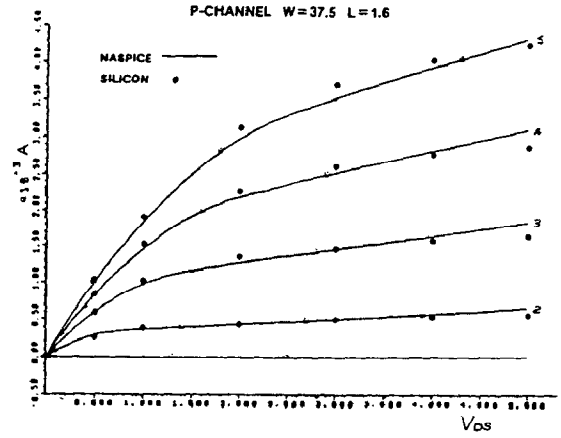

Figure 11 NASPICE generated output for single P-channel transistor (W/L = 37.5/1.6 micron) showing comparison with silicon.

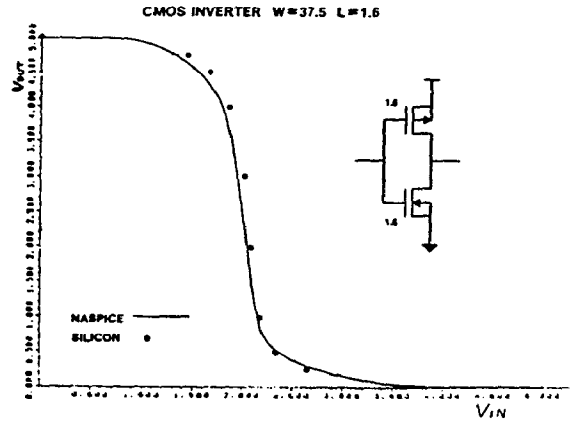

Figure 12 NASPICE generated DC transfer characteristic for CMOS inverter made by combining W/L = 37.5/1.6 micron N and P-channel devices, showing comparison with silicon.