A CMOS AM Demodulator for Instrumentation Applications

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ABSTRACT

This paper describes the design of a CMOS IC AM demodulator. Design details of the monolithic implementation of a highly accurate synchronous rectifier in a standard 0.35 μm CMOS process on a ± 2.5 V voltage supply are presented. The derived circuit implements an envelope detector with a ± 1.5 V output swing on a 15 pF load. Small distortion ($THD = -60$ dB) and low noise ($SNR = 84.7$ dB) are some attractive features of the proposed design.

Categories and Subject Descriptors

B.7.2 [**Integrated Circuits**]: Design Aids—*Verification*

General Terms

Design

Keywords

AM demodulator, integrated circuits, cavitation detector, ideal rectifier

1. INTRODUCTION

Amplitude modulated (AM) demodulator circuits are widely employed in a large variety of instrumentation applications. Nevertheless, the realization of monolithic AM demodulators is still a difficult task (see, e.g., [2]). This paper presents an AM demodulator which is part of a CMOS integrated circuit, whose block diagram is shown in Fig. 1, but that can be easily adapted to other applications. The accelerometer picks up the vibration of a metalic structure and produces an electrical signal composed of an AM waveform embedded in noise.

In a single integrated circuit, an anti-aliasing filter is followed by an accurate bandpass switched-capacitor filter working at 200 kHz, that rejects a large amount of noise and selects the baseband signal. Its output is a sampled-and-held waveform, and hence must be applied to a reconstruction filter, so as to remove the undesired replicas of the bandpass signal produced by the switched-capacitor filter. The result is a 5 kHz baseband component modulated in amplitude around 25 kHz with ± 1.5 V swing on a 15 pF load. Operating as an envelope detector with a rectifier and a lowpass filter [3], the AM demodulator finally extracts the desired signal. This is converted into a digital bit stream by an off-chip A/D converter, and subsequently processed by a DSP, that obtain the signal properties that are of particular interest for the purposes of understanding and minimizing the causes of the structure vibration.

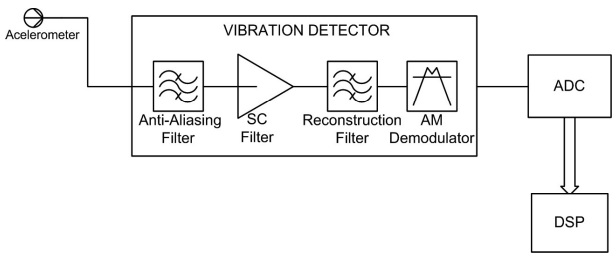

Figure 1: Vibration detector system.

This paper focuses on the IC design of the above AM demodulator circuit, implemented in a standard 0.35 μm CMOS process, using a ± 2.5 V supply voltage. Design details and simulation results are presented in the next Sections. The simulation results obtained with SPECTRE are presented to vedrify the effectiveness of the proposed design approach.

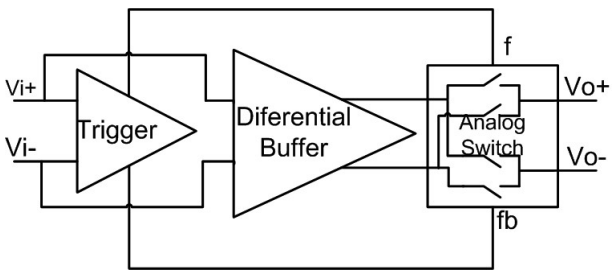

Figure 2: AM demodulator architeture.

2. AM DEMODULATOR DESIGN

The AM demodulator is basically a peak detector followed by a rectifier and a lowpass filter [3]. Since the upper bound frequency of the modulated signal is around 5 kHz, the time

constant of the lowpass filter is 0.2 ms, which requires rather large component values. For this reason, the lowpass filter is implemented externally to the chip.

The envelope detector, after lowpass filtering, requires a rectifier with zero voltage threshold, because the sensor signal level is small and below usual diode threshold voltages. To circunivent this difficulty, the rectifier was designed as a highly precise synchronous rectifier employing an open loop operational transconductance amplifier (OTA), termed trigger in Fig. 2, and analog switches. The voltage differential buffer will be important to increase the capacitive load of the lowpass filter [5].

2.1 Trigger

The open loop differential OTA, shown in Fig. 3, was designed to compare the reference voltage to the sensor signal, as performed by a diode in conventional approaches. The comparator circuit is implemented by a folded cascode stage, since high gain is not a necessary condition for the proper operation of the trigger circuit.

The circuit of Fig. 3 was designed using a fraction of the buffer bias current, I_{bias}. This requires a highly precise current mirror. To this end, V_{B1} and V_{B3} are chosen such as to satisfy the following conditions to guarantee the circuit operation in the saturation region:

$$2\,\Delta\,V_{GS} + V_T \leq V_{B1,3} \leq \Delta\,V_{GS} + 2\,V_T. \qquad (1)$$

With $V_{B1,3} = \sqrt{5}\,\Delta\,V_{GS} + V_T$ the biasing circuit can be implemented by the 5 transistors connected in series, as shown in Fig. 3. As a result, the condition (1) will be always satisfied, regardless of process variation effects, since both the cascode current mirror and its bias circuit will be equally affected.

The outputs are two digital signals, F and $\bar{F}$, which convey the information about from the sign of the input signal, needed for openning or closing the following analog switches (see Fig. 2). The ideal rectifier realizes comparisons between the ground reference and the sensor signal. Consequently, the outputs are logic levels, whose values depend on the signal sign.

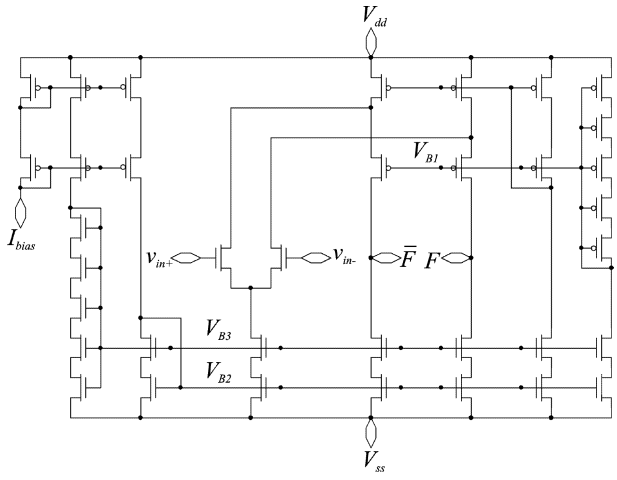

Figure 3: Trigger schematic.

2.2 Analog Switches

Figure 4 shows the schematic diagram of the analog switching circuit that performs zero-threshold signal retification. Its input is provided by the buffer output. The analog switches multiplex the incoming signal into a full wave rectification. This operation is carried out synchronously with the trigger clocks.

If the signal sign is positive, then the F clock is high, and the analog switches conect V_{o+} to V_{DEM+} and V_{o-} to V_{DEM-}. If the signal sign is negative, then the F clock is low, and the analog switches conect V_{o+} to V_{DEM-}, and V_{o-} to V_{DEM+}. As a result, V_{DEM+} is a full wave rectified signal with positive sign, and V_{DEM-} is a negative full wave rectified signal.

The dimensions (width and length) of the switch devices were defined such as to minimize the effects of the output impedance in the wrapped detector response.

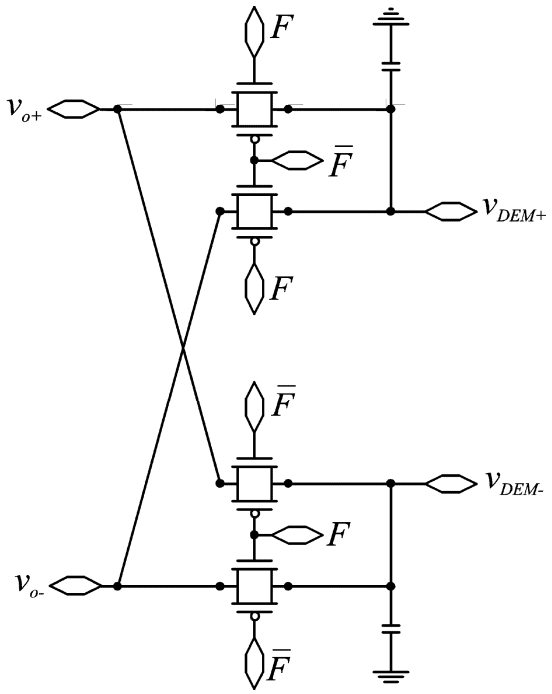

Figure 4: Analog Switches schematic.

2.3 Buffer

The differential, unit-gain, voltage buffer is implemented by an OTA. Similar configuration was presented in [5], except that an operational voltage amplifier was used therein. The unit gain of the buffer proposed in this paper is produced by an internal current feedback, as indicated in Fig. 5. The circuit, shown in Fig. 6, comprises two differential pairs with crossed coupling, output in folded cascode configuration, and common mode control. It was designed to handle a $\pm 1.5\ V$ output swing, a capacitive load of $C_L = 15\ pF$ and achieve a cutoff frequency of 2.5 MHz.

The conventional two-transistor symmetric diferential pair has shown poor linearity because g_m is strongly dependent on the input voltage. A notable increase in linearity can be obtained by using two asymetric and one symetric differential pair, as show in [4]. For the case of unity-gain buffers,

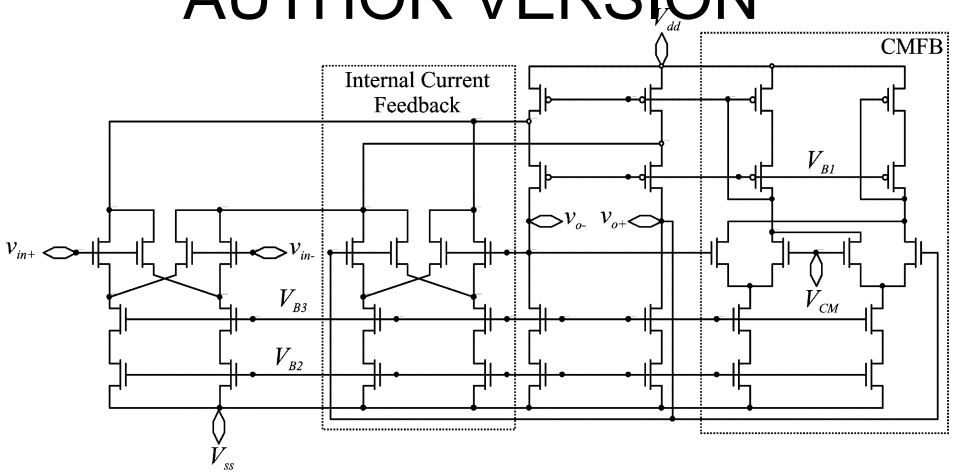

Figure 6: Buffer schematic.

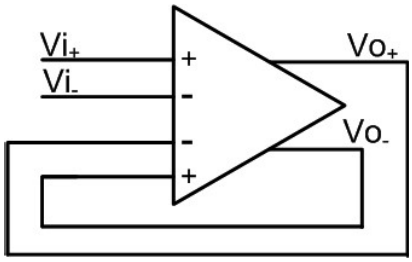

Figure 5: Buffer architeture.

the strong feedback guarantees low THD even if the input stage does not present high linearity.

The MOSFETs are assumed to operate in the saturation region and in strong invesion. Thus, their drain currents are modeled by $I_D = \beta\,(V_{GS} - V_{Th})^2/2$, where $\beta = k_p\,W/L$.

Assuming $\beta_a > \beta_b$, where a and b refer, respectively, to the simmetric and assimetric differential pairs, and that their transconductances (g_m) are asymmetric with respect to the vertical axis at $v_d = 0$, the bias current I_s and the parameters β_a and β_b can be deStermined such as to make the total transconductance gm_0 equirippel inside the interval $[-v_{dM}/2, +v_{dM}/2]$, as illustrated in Fig. 7. This assumption leads to the following design equations:

$$I_s = 1.05133\; gm_0\; v_{dM}, \tag{2}$$

$$\beta_a = 14.3675\;\frac{gm_0}{v_{dM}}, \tag{3}$$

$$\beta_b = 1.51977\;\frac{gm_0}{v_{dM}}, \tag{4}$$

where v_{dM} is the maximum differential voltage.

Numerical computations have shown that the worst THD (2.34%) is obtained, when the input voltage is 21% of v_{dM}.

The common mode voltage control, discussed in [1], was implemented with two differential pairs comparing the output voltage to a reference voltage. The CMFB circuit compensates variations in the common mode voltage by changing the cascode bias current.

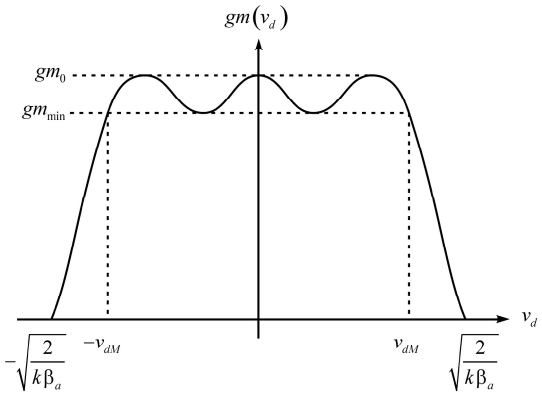

Figure 7: Buffer transcondutance characteristics.

3. RESULTS

The trigger clocks control the switching sequence of the complementary switches, such as to produce a highly precise synchronous rectifier. Both the trigger and the switch circuits were tested under extreme operation conditions, and proved effective solutions for the AM demodulation scheme proposed in this paper.

The circuit produces the resulting full wave rectification as shown in dashed line in Fig. 8. The demodulated (baseband) signal is shown in solid line. This result includes the action of a lowpass filter externally connected to the circuit. The frequency response of the buffer followed by the lowpass filter is presented in Fig. 9.

The buffer was designed with a $\pm 2.5\;V$ supply voltage and its power consumption was mesured during the demodulation operation. Its die area, 0.026 mm^2, is lager than that of the synchronous rectifier, wich is 0.009 mm^2.

The buffer signal swing, presented in Fig. 10, was evaluated with a DC sweep input. The THD was computed with a 5 kHz baseband sine wave input having a $\pm 1.5\;V$ amplitude. The noise was analyzed in the frequency band from 10 kHz up to 30 kHz.

The transcondutance was mesured for an input signal swing of $\pm 1.5\;V$. Finally, its cut-off frequency was 2.5 MHz. The results are obtained in SPECTRE simulator and the gen-

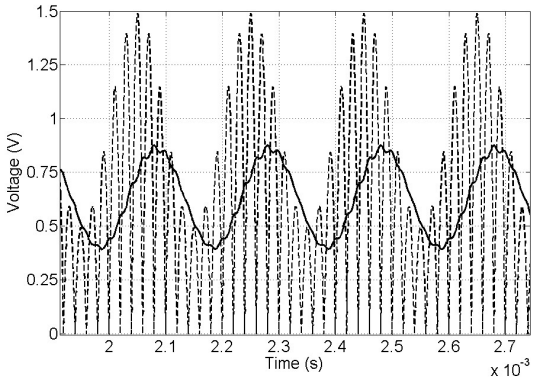

Figure 8: The complete wave rectification and AM demodulation.

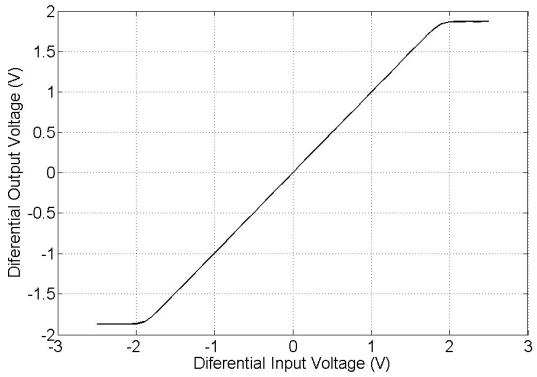

Figure 10: Buffer signal swing.

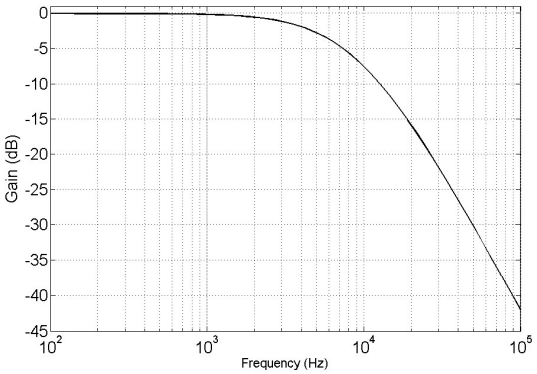

Figure 9: Frequency response: buffer and lowpass filter externally connected.

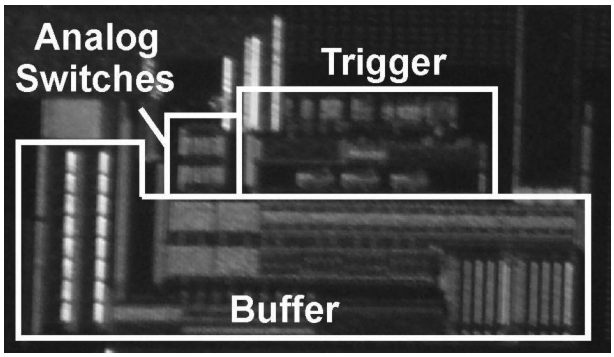

Figure 11: AM demodulator microphotograph.

eral characteristics of the designed buffer are summarized in Table 1.

4. CONCLUSIONS

The AM demodulator advanced in this paper was designed in a standard 0.35 μm CMOS process using a $\pm 2.5\ V$ supply voltage. This solution is suitable to other AM demodulation applications as well. The trigger compares the signal with the reference voltage, as performed by the conventional approach employing a diode threshold voltage. It implements an ideal rectifier model (zero-voltage threshold). The trigger clocks activate the complementary switches as a precision synchronous rectifier. The buffer has a $\pm 1.5\ V$ output swing on a 15 pF load. It has low distortion ($THD = -60\ dB$), low noise ($SNR = 84.7\ dB$), occupies small area (0.026 mm^2) and has low power consumption (16.3 mW).

5. REFERENCES

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Parameter	Value
Power Supply Voltage	$\pm 2.5\ V$
Total Current Consumption	3.26 mA
Total Power Consumption	16.3 mW
Total Area Consumption	0.026 mm^2
Input and Output Voltage Swing - peak to peak	$\pm 1.5\ V$
Transcondutance	$83 \pm 7\ \mu S$
THD	$-60\ dB$
Output Noise	61.69 μV
SNR	84.7 dB

Table 1: Buffer general characteristics.