

Energy Harvesting Photodiodes with Integrated 2D Diffractive Storage Capacitance

Nathaniel J. Guilar, Erin G. Fong, Travis Kleeburg, Diego R. Yankelevich, Rajeevan Amirtharajah
 Micropower Circuits and Systems Group, Department of Electrical and Computer Engineering
 University of California, Davis, CA 95616

ABSTRACT

Integrating photodiodes with logic and exploiting on-die interconnect capacitance for energy storage can enable new, low-cost energy harvesting wireless systems. To further explore the tradeoffs between optical efficiency and capacitive energy storage for integrated photodiodes, an array of photovoltaics with various diffractive storage capacitors was designed in TSMC's 90 nm CMOS technology. Transient effects from interfacing the photodiodes with switching regulators were examined. A quantitative comparison between 90 nm and 0.35 μm CMOS logic processes for energy harvesting capabilities was carried out. Measurements show an increase in power generation for the newer CMOS technology, however at the cost of reduced output voltage.

Categories & Subject Descriptors

[Integrated Circuits]: General.

General Terms

Design, Experimentation, Measurement.

Keywords

Energy Harvesting, Diffraction, Photodiode.

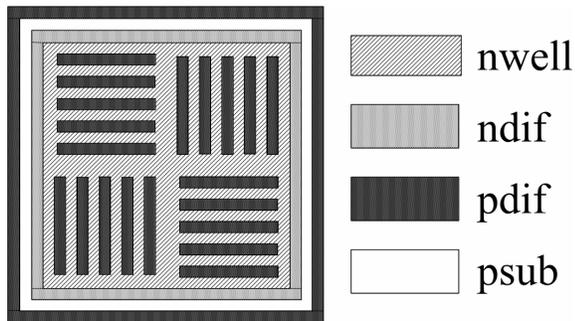


Figure 1: Layout view of 2D integrated photodiode. Metal diffraction gratings are aligned with the pdif figures.

Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. To copy otherwise, or republish, to post on servers or to redistribute to lists, requires prior specific permission and/or a fee.

ISLPED '08, August 11–13, 2008, Bangalore, India.
 Copyright 2008 ACM 978-1-60558-109-5/08/08...\$5.00.

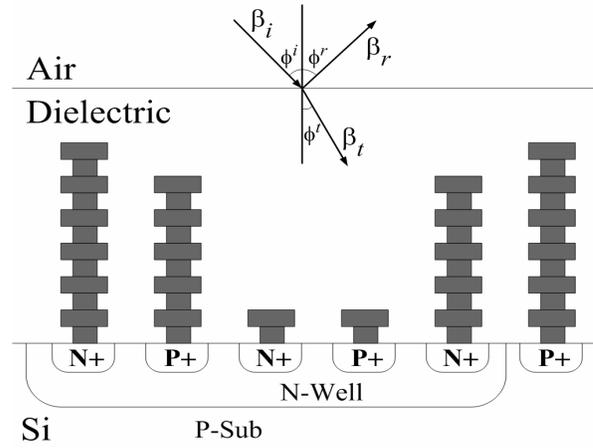


Figure 2: Side view of candidate one dimensional photodiode (design D2 from [1]) together with storage capacitance. Metal pattern helps to reduce reflections and guides light to depletion region.

1. INTRODUCTION

CMOS technology scaling has continued to reduce the size and active power consumption of electronic devices. This trend has opened the door for energy harvesters to power wireless systems through extracting mechanical, thermal or solar energy from the environment. Increased system integration has allowed solar energy harvesters in the form of passive photodiodes to be implemented on the same silicon die as active circuitry, which can be powered by the harvested energy. These integrated photodiodes [1] are modeled after a passive pixel architecture [2], which can form the basis for CMOS imagers. Integrating the solar energy harvesting on the same die as other parts of the system enables reduced system cost and size. However, side effects such as lateral photocurrent may become problematic [3-5]. Previous works have outlined the use of environmental energy harvesting for powering wireless systems [6-16]. For many wireless systems, photovoltaics are a viable source for energy harvesting [7-9]. When solar energy alone is not enough, multiple energy harvesting transducers can be combined to increase the total generated energy [12]. Efficiently combining the multiple sources can prove to be difficult, especially with power budgets in the micro watts.

2. INTEGRATED PHOTODIODES

Figure 1 shows the layout for an integrated photodiode. A 2D photodiode structure was used for the fingers of p-diffusion implanted in the n-well. Vertical parallel plate storage capacitance can be constructed on top of the fingers, forming an optical diffraction grating. Since the spacing between these vertical metal strips doubles as the aperture for the incident light, the storage capacitance will have an optical filtering effect. In order to increase the optical efficiency so the photodiode can harvest additional energy from off-axis illumination (large incident angle, ϕ^i from Fig. 2) a periodic grating sequence can be implemented by varying the height of the metal fingers.

Figure 2 shows the side view of one possible energy harvesting photodiode with integrated storage capacitance, based on design D2 from [1]. The gray metal pillars constructed from vias and metal layers reflect and diffract incident light. Diffraction can be defined as the bending or spreading of light waves when they interact with an obstacle [17, 18]. Diffraction gratings were originally designed for acoustic waves, but have applications in optics as well. Much of the initial investigation into these types of gratings was done by Schroeder [19, 20]. His goal was to design a surface for enhancing the acoustics in concert halls. Schroeder applied number theory based on a quadratic residue sequence to determine the geometric periodicity used in the diffusion grating. His original concept was to design a ceiling that would limit the amount of direct reflections heard by the audience. He accomplished this by designing a surface that would limit the amount of reflections into the audience over a wide bandwidth. For audio, the diffusion provided by the periodic grating reduces the sense of localization for the reflected waves. By reducing the amount of reflected light, the diffraction grating can increase the transmitted energy into the photodiode. Feldman was the first to suggest using a primitive root sequence instead of the quadratic residue sequence for the diffraction gratings [21].

In total six different geometries (D1-D6) for the storage capacitance were designed and tested. Each diode occupied the same area and had the same diffusion layout, from Fig. 1, but incorporated a different metal diffraction grating using metal interconnect layers M1-M6. A goal of this work is to determine the impact which the metal storage capacitance has on the photodiodes' optical efficiency. The first diode D1 is the control, where only M1 was used to connect the p-diffusion fingers together. Diodes D2 and D3 used M1 through M6, and were based on quadratic residue sequence diffusers with periods 5 and 7, respectively. Diodes D4 and D5 also used M1 through M6, but were based on a primitive root sequence with periods 4 and 6, respectively. Diode D6 was also a control, where its diffraction grating occupied all six layers throughout for a maximum metal fill density.

Figure 3 shows diagrams depicting the side view for the various diffraction grating sequences [22]. Each diode from

D2-D5 has its own periodicity ranging from 4 to 7 fingers. Gray rectangles indicate metal interconnect. Light passes between the vertical metal plates and then into the substrate, shown as a white rectangle. Table I shows the metal height of the diffraction grating as a function of position for each photodiode. The metal fill density is also reported, where 100 % corresponds to D6 which has every position filled to M6.

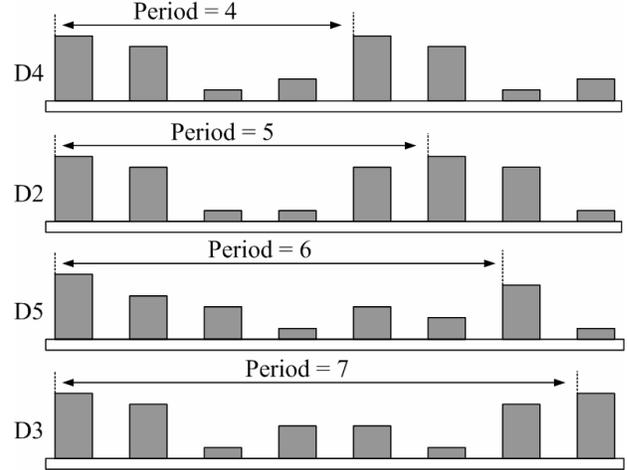


Figure 3: Side view of photodiodes with gray metal diffraction gratings showing periodicity for various sequences.

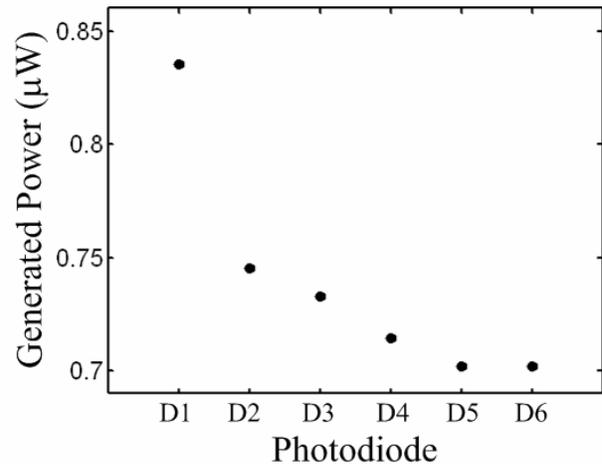


Figure 4: Generated electrical power for various photodiodes with an optical illuminance of 5 kLUX.

**Table 1
Diffraction Grating Sequence and Metal Fill Density**

Diode	1	2	3	4	5	6	7	Fill Density
D1	1	1	1	1	1	1	1	16%
D2	6	5	1	1	5			60%
D3	6	5	1	3	3	1	5	57%
D4	4	1	5	6				67%
D5	4	5	1	3	2	6		53%
D6	6	6	6	6	6	6	6	100%

Figure 4 shows the generated power for each photodiode. Measurements were conducted with white light illumination from a normal tungsten filament of 5 kLUX and an active diode area of $10000 \mu\text{m}^2$ at room temperature. Since each photodiode has the same area and diffusion geometry, the differences between the various photodiodes originate only from optical losses. Each photodiode has an increasing amount of fill density, ranging from the low density of D1 to the maximum density of D6. It can be seen here that there is a direct correlation between metal fill density and optical loss. Therefore, a tradeoff exists between optical efficiency and capacitive energy storage. The duty cycle for the periodicity between the metal width and metal spacing is near 32 %. The period for a single aperture-metal pair is near $1 \mu\text{m}$ and the space between the vertical parallel plates is $0.675 \mu\text{m}$.

Figure 5 shows the generated electrical power for photodiode D2, which uses the quadratic residue diffuser (QRD) with period 5, plotted versus load resistance. Each trace is for a different illumination, ranging from 400 LUX to 20 kLUX. It can be seen that the optimal resistance for the photodiode becomes more selective at higher light intensities. Often a method known as maximum power point tracking (MPPT) is employed to ensure that the photodiode operates near the optimal load condition [23-26]. The optimum matching of photodiodes to resistive load has been previously outlined [23]. Various techniques using switching regulators have also been proposed for tuning the photodiode for maximum power generation [24-26]. Each of these techniques requires additional energy overhead to carry out the MPPT algorithm. The curves from Fig. 5 suggest that MPPT could have substantial benefits for the integrated photodiodes, especially at higher power generation. At lower light intensities ($< 1 \text{ kLUX}$), the energy overhead required for an MPPT algorithm might offset any additional energy harvesting benefits. A well designed power management system for solar energy harvesting would turn on an MPPT algorithm for larger power generation, but then turn it off as illumination decreases. Figures 6 and 7 show the generated electrical power for photodiodes D1 and D6, respectively. These measurements were taken with a white light source directly on-axis (i.e., normal to the surface of the chip). The characteristic shapes of the power curves are similar since they have identical diffusion patterns. Photodiode D1 generates the most power with on-axis illumination due to a high optical efficiency from a low metal fill density.

Thin metal gratings, similar to the ones discussed here, have previously been used in photovoltaic applications as a back reflector, which traps light reflecting off the air to glass interface [27-29]. When optimized, the diffraction gratings have been shown to increase efficiency of the photodiode by more than 6.2 % [29]. Some rules of thumb have been developed for designing gratings for superior optical performance: grating period should equal $0.7 \times \text{wavelength}$ of light, optimal grating depth = $0.18 \times \text{wavelength}$ of light, and, for thicker gratings, a duty-cycle near 50 % is optimal [28].

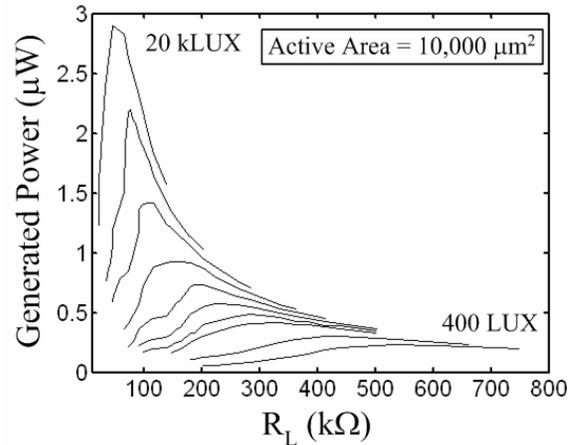


Figure 5: Generated electrical power for photodiode D2 (QRD, $p=5$) for various light intensity levels ranging from 400 to 20 kLUX.

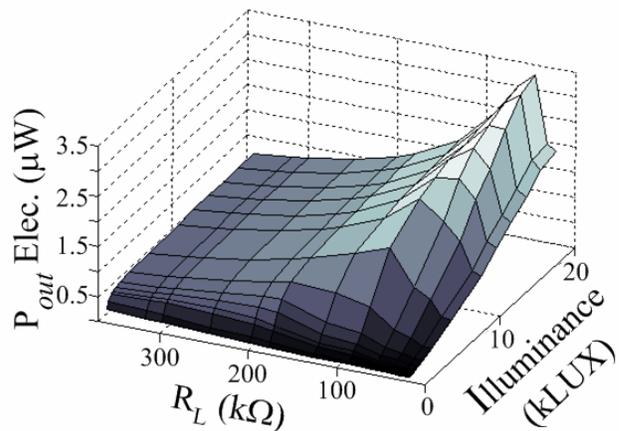


Figure 6: Device characterization for photodiode D1 (control), Active area = $10,000 \mu\text{m}^2$.

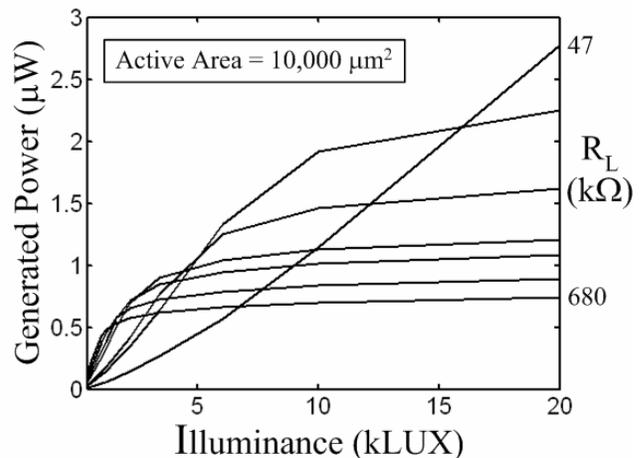


Figure 7: Power curves for photodiode D6 (maximum metal fill density). Each trace is for a different load resistance ranging from 47 to 680 kΩ.

Figure 8 shows the open circuit voltage of two different photodiodes swept over incident light angle. These measurements were conducted with a green laser with $\lambda = 532$ nm. When the light is positioned directly above the chip, the photodiode with the minimal amount of metal capacitance (D1) has the highest generated voltage. There exists an angle, near 45° off-axis, where the photodiode with a diffraction grating (D4) generates the larger voltage. In many wireless sensor network scenarios, direct on-axis illumination cannot be guaranteed; therefore having a photodiode with a good off-axis response can maximize the harvested energy.

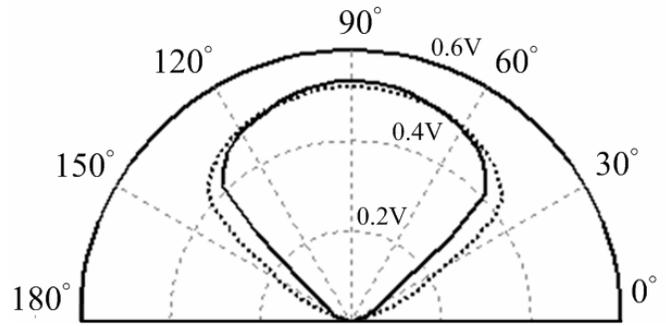


Figure 8: Polar plot of open circuit voltage versus angle of incident light, measuring the photodiodes' off-axis response. Solid line is control D1 (only M1). Dashed line is D4 with periodic diffraction grating (M1-M6). $\lambda = 532$ nm. Peak generated voltage near 0.5 V.

Figure 9 shows a simplified schematic for testing the transient response of a photodiode. Typically, a switching regulator is used to modulate the current flow from the photodiode to a load. Here the load is modeled as a resistor R_L in parallel with a capacitor C_p . When ϕ rises, the switch in Fig. 9 closes and charge is shared between the photodiode and the load. This additional loading will force the photodiode's voltage to decrease, causing a fluctuation in the generated power. This fluctuation on the power supply is highly undesirable and, for sensitive circuits such as analog-to-digital converters, may be a limiting factor restricting resolution or accuracy. A storage capacitance C_t in parallel with the photodiode can be used to mitigate this fluctuation. The additional storage capacitance acts as a filter reducing the voltage ripple caused by the switching.

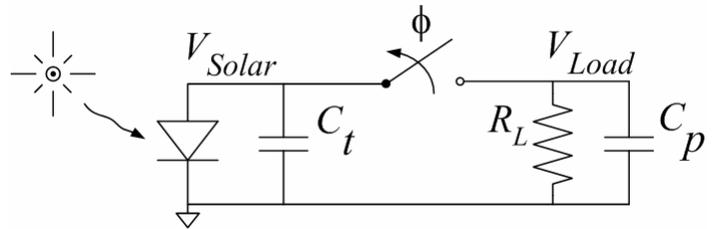


Figure 9: Simplified schematic of solar energy harvesting power supply. A switched RC is used to model a digital load. A larger C_t will function as a filter to smooth current pulses through the switch.

Figure 10 compares the transient response for photodiodes D1 and D2. For these measurements, an input light intensity of 5 kLUX was used along with $R_L = 100$ k Ω and $C_p = 6$ pF. When ϕ rises, the switch in Fig. 9 closes and connects V_{Solar} to V_{Load} . The additional capacitance associated with D2's metal diffraction grating reduced the transient spike when the switch closes. Photodiode D2 with the additional metal storage capacitance exhibits roughly one half of the peak ripple caused by the switching when compared to photodiode D1, which has no additional capacitance. There exists a direct tradeoff between optical efficiency and electrical filtering. A minimal diffraction grating provides a good balance between solar energy harvesting and electrical energy storage.

3. EXPERIMENTAL COMPARISON

In order to better understand the effects of technology scaling on integrated photodiodes, experiments were conducted to compare photodiodes implemented in 90 nm and 0.35 μ m CMOS logic processes. The increased dopant concentrations used in the newer technology resulted in a smaller open circuit voltage when compared to the older technology, for equivalent input illuminance. However, the overall power generation and fill factor was higher for the more advanced 90nm process. Figure 11 plots the open circuit voltages for the two technologies versus input illuminance.

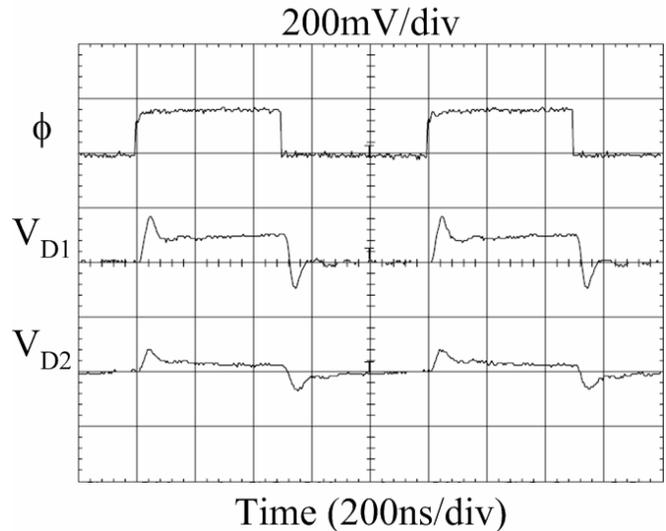


Figure 10: Measured waveforms showing clock signal ϕ and V_{solar} voltages for photodiodes D1 and D2. The additional metal capacitance associated with photodiode D2 allows for a reduced voltage ripple.

Data for single- and double-stacked energy harvesting photodiodes are shown. It can be seen here that the 90 nm technology has a more consistent open circuit voltage over a wider range of input illuminance conditions. The fill factor (defined as the ratio of diode output power at a particular load condition to the product of the diode's open circuit voltage and short circuit current), is a common figure of merit used in characterizing photodiode technologies. The photodiode prototypes in this work have an average fill factor of 0.8.

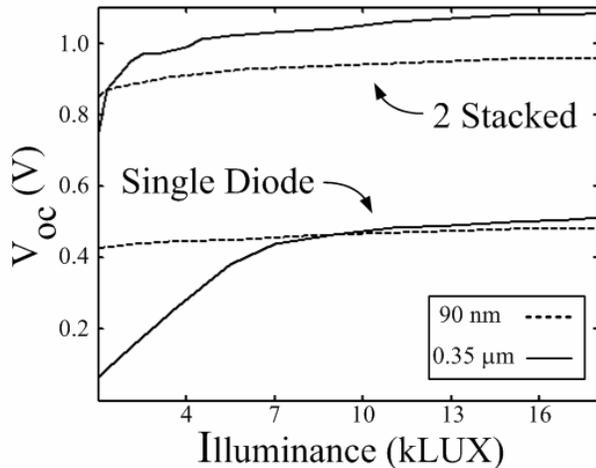


Figure 11: Open circuit voltage for a single diode and two diodes stacked in series for 90 nm and 0.35 μm CMOS technologies.

4. CONCLUSION

In this paper we have outlined both optical and electrical design considerations for integrated energy harvesting photodiodes. By using a diffraction grating based on number theory, metal storage capacitors can be integrated with the photodiodes while causing minimal optical losses. A tradeoff between optical efficiency and transient response can be realized with a moderately dense metal capacitance constructed on top of the photodiode. By using a numerical pattern for the metal capacitance such as a quadratic residue sequence, an increase in off-axis photodiode response can be obtained, at the expense of a slightly diminished on-axis response. Table 2 summarizes the measured results for a few select photodiodes. These measurements were conducted with an input light intensity of 10 kLUX. At 20 kLUX, the output power for diode D1 is $325 \mu\text{W}/\text{mm}^2$, a 44 % increase over [1]. Figure 12 shows the die photograph for the 2D test structures built in 90 nm CMOS. Photodiode D2 appears to have the best overall performance, showing a good balance between power generation, storage and transient response.

Table 2

Measured Performance (25 °C, Area=10,000 μm^2)

Parameters	D1	D2	D4	D6
Power Generated (μW)	1.32	1.30	1.26	1.20
Energy Stored (pJ)	0.86	1.43	1.55	1.98
Capacitance C_t (pF)	7.52	12.74	13.57	17.47
V_{OC} (mV)	479	473	478	477
I_{SC} (μA)	5.96	5.76	5.63	5.43

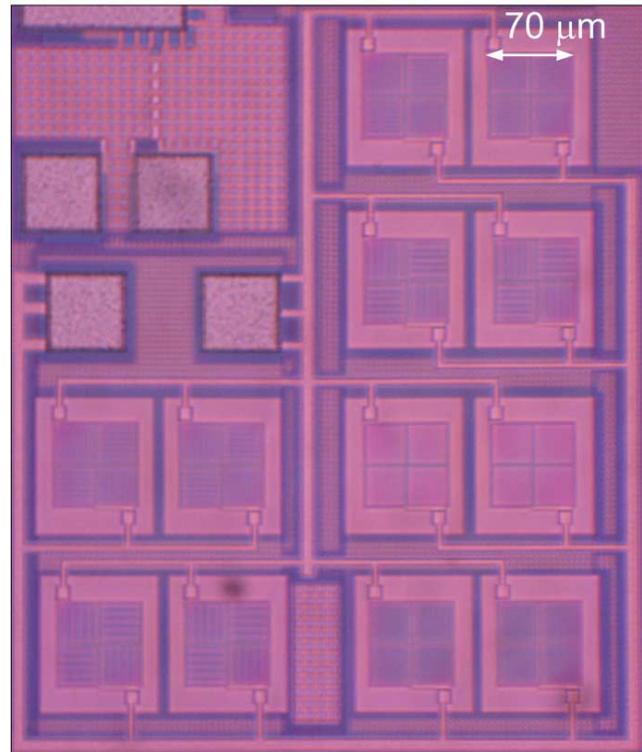


Figure 12: Die photograph showing multiple photodiodes constructed in the 90 nm CMOS process, each diode is 70 μm on a side.

Acknowledgments

The authors are grateful to S. Bruss, P. Hurst, A. Knoesen, and S. Lewis for their help with designing and testing the prototype. Fabrication was graciously provided by TSMC. N. Guilar and T. Kleeburg are supported by the U.S. Dept. of Education GAANN fellowship and the UC Micro grant.

5. REFERENCES

- [1] N. Guilar, A. Chen, T. Kleeburg, and R. Amirtharajah, "Integrated Solar Energy Harvesting and Storage," *ACM/IEEE ISLPED*, pp. 20-24, 2006.
- [2] I. Fujimori, C. Wang, and C. Sodini, "A 256×256 CMOS Differential Passive Pixel Imager with FPN Reduction Techniques," *IEEE JSSC*, vol. 35, pp. 2031-7, Dec. 2000.
- [3] J. Soo Lee, R. I. Hornsey, and D. Renshaw, "Analysis of CMOS Photodiodes-Part I: Quantum Efficiency," *IEEE Trans. on Electron Devices*, vol. 50, no. 5, May, 2003.

- [4] J. Soo Lee, R. I. Hornsey, and D. Renshaw, "Analysis of CMOS Photodiodes-Part II: Lateral Photoresponse," *IEEE Trans. on Electron Devices*, vol. 50, no. 5, May, 2003.
- [5] P. B. Catrysse, P. and B. A. Wandell, "Optical Efficiency of Image Sensor Pixels," *J. Opt. Soc. Am.*, vol. 19, no. 8, pp.1610-1620, Aug. 2002.
- [6] A. Kansal and M. Srivastava, "An Environmental Energy Harvesting Framework for Sensor Networks," *ACM/IEEE ISLPED*, pp. 481-6, Aug. 2003.
- [7] V. Raghunathan, A. Kansal, J. Hsu, J. Friedman, M. Srivastava, "Design Considerations for Solar Energy Harvesting Wireless Embedded Systems," *International Symposium on Information Processing in Sensor Networks*, pp. 457 - 462, April, 2005.
- [8] X. Jiang, J. Polastre, and D. Culler, "Perpetual Environmentally Powered Sensor Networks," *In Proc. 4th Int. Conf. on Information Processing in Sensor Networks*, pp. 463-468, April, 2005.
- [9] F. Simjee and P. H. Chou, "Everlast: Long-life, Supercapacitor-Operated Wireless Sensor Node," *ACM/IEEE ISLPED*, pp. 197-202, Oct. 2006.
- [10] R. Amirtharajah, J. Wenck, J. Collier, J. Siebert, B. Zhou, "Circuits for Energy Harvesting Sensor Signal Processing," *ACM/IEEE Design Automation Conference*, pp. 639 -644, 2006.
- [11] A. Kansal, J. Hsu, M. Srivastava, V. Raqhunathan, "Harvesting Aware Power Management for Sensor Networks," *ACM/IEEE Design Automation Conference*, pp. 651 - 656, 2006.
- [12] V. Raghunathan, P. H. Chou, "Design and Power Management of Energy Harvesting Embedded Systems," *ACM/IEEE ISLPED*, pp.369-374, 2006.
- [13] J. Hsu, S. Zahedi, A. Kansal, M. Srivastava, V. Raghunathan, "Adaptive Duty Cycling for Energy Harvesting Systems," *ACM/IEEE ISLPED*, pp. 180 - 185, 2006.
- [14] P. Stanley-Marbell, D. Marculescu, "An 0.9 x 1.2", Low Power, Energy-Harvesting System with Custom Multi-Channel Communication Interface," *Design, Automation & Test in Europe Conference*, pp. 1-6, April, 2007.
- [15] J. Elmes, V. Gaydarzhiev, A. Mensah, K. Rustom, J. Shen, I. Batareseh, "Maximum Energy Harvesting Control for Oscillating Energy Harvesting Systems *IEEE PESC*, pp. 2792-2798, June, 2007.
- [16] H. Shao, C.-Y. Tsui, W.-H. Ki, "An Inductor-less Micro Solar Power Management System Design for Energy Harvesting Applications," *IEEE ISCAS*, pp. 1353 - 1356, 2007.
- [17] P. Beckmann and A. Spizzichino, *The Scattering of Electromagnetic Waves from Rough Surfaces*, Pergamon Press, 1963.
- [18] E. G. Loewen and E. Popov, *Diffraction Gratings and Applications*, NewYork: Marcel Dekker, 1997.
- [19] M. R. Schroeder, "Diffuse Sound Reflection by Maximum-Length Sequence," *J. Acoust. Soc. of America*, vol. 57, no. 1, pp. 149-150, 1979.
- [20] M. R. Schroeder, "Binaural Dissimilarity and Optimum Ceilings for Concert Halls: More Lateral Sound Diffusion," *J. Acoust. Soc. of America*, vol. 65, no. 4, pp. 958-963, 1975.
- [21] E. Feldman, "A Reflection Grating that Nullifies the Specular Reflection: A Cone of Silence," *J. Acoust. Soc. of America*, vol. 98, no. 623, 1995.
- [22] G. Ballou, *Handbook for Sound Engineers: New Audio Cyclopedia*, Focal Press, 1998.
- [23] K. Y. Khouzam, "Optimum Load Matching in Direct-Coupled Photovoltaic Power Systems-Application to Resistive Loads," *IEEE Trans. on Energy Conversion*, vol. 5, no. 2, pp. 265 - 271, June 1990.
- [24] C. R. Sullivan, M. J. Powers, "A High-Efficiency Maximum Power Point Tracker for Photovoltaic Arrays in a Solar-Powered Race Vehicle," *IEEE PESC*, pp. 574 - 580, June 1993.
- [25] C. Hua, C. Shen, "Study of Maximum Power Tracking Techniques and Control of DC/DC Converters for Photovoltaic Power System," *IEEE PESC*, pp. 86 - 93, May 1998.
- [26] K. K. Tse, M. T. Ho, H.S.-H. Chung, S.Y. Hui, "A Novel Maximum Power Point Tracker for PV Panels Using Switching Frequency Modulation," *IEEE Trans. on Power Electronics*, vol. 17, no. 6, pp. 980 - 989, Nov. 2002.
- [27] C. Heine and R. H. Morf, "Submicrometer Gratings for Solar Energy Applications," *Appl. Opt.*, vol. 34, no. 14, pp. 2476-2482, May 1995.
- [28] C. Eisele, C. E. Nebel, and M. Stutzmann, "Periodic Light Coupler Gratings in Amorphous Thin Film Solar Cells," *J. Appl. Phys.*, vol. 89, no. 12, pp. 7722-7726, Jun. 2001.
- [29] N.-N. Feng, J. Michel, L. Zeng, J. Liu, C.-Y. Hong, L. C. Kimerling X. Duan, "Design of Highly Efficient Light-Trapping Structures for Thin-Film Crystalline Silicon Solar Cells," *IEEE Trans. on Electronic Devices*, vol. 54, no. 8, pp. 1926 - 1933, Aug. 2007.