

# The ORDVAC

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**T**HE ORDVAC is a general purpose machine which has been built by the University of Illinois for the Ballistic Research Laboratories at Aberdeen, Maryland. The design has followed in a general way that of the computing machine discussed by Burks, Goldstine, and von Neumann in the "Preliminary Discussion of the Logical Design of an Electronic Computing Instrument" issued in 1946 by the Institute for Advanced Study.<sup>1</sup>

We are indebted to the Computer Project at the Institute for Advanced Study for much information and many suggestions such as the basic philosophy of an asynchronous machine with direct-coupled circuits. Furthermore some of the circuits in our machine are the same as those of that machine and some others are similar but differ in detail.

It is convenient to display the characteristics of the machine by means of Table I. Some of these will be described in more detail in the appropriate sections which follow. For this purpose we shall divide the machine into five parts: the arithmetic unit, the input-output, the memory, the control and the power supply. Two general views of the machine, with and without its covers, are shown in Figures 1 and 2.

## Arithmetic Unit

The arithmetic unit is made up of three parts: the registers, the adder, and the digit resolver. The registers are four in number, the accumulator, the arithmetic register, the number register, and the order register. The register gates and flip-flops used in the ORDVAC follow exactly designs furnished by the Institute for Advanced Study. Of the registers named above, the latter two are nonshifting registers each of which consists of 40 binary digits held in 40 flip-flops. Information is communicated through them to the arithmetic unit and control from the memory. The number register holds addend, multiplier, and divisor for arithmetic operations. The order register receives from the memory all orders to be handled by the control.

The shifting registers (accumulator and arithmetic register) each consist

of two rows of 40 flip-flops, one row above the other. Since a nonshifting register contains one row of 40 flip-flops, two nonshifting registers can be made out of one shifting register, and the appearance of the ORDVAC is that of a machine with three double registers.

In addition to the two rows of flip-flops, a shifting register also has two rows of gate tubes. These gate tubes furnish four gates for each stage of the register—two "up" gates and two "down" gates. The "up" gates transfer straight up, while the "down" gates transfer down one place to the left or one place to the right. The bottom row of a shifting register holds the digits while they are being sensed during an operation; the top row is used as transient storage. A shift is accomplished by clearing the upper row, gating up to it from the lower row, clearing the lower row, and finally gating down either one place to the left or one place to the right. When shifts are made in this way information is not cleared from one location until it has been deposited in another.

Figure 3 illustrates part of a register, the down gates into a lower flip-flop being shown. The plate supplies of a flip-flop come from busses which are normally at +150 volts but which can be lowered for the purpose of clearing the flip-flop to either state. Thus if the supply to pin 1 is dropped, the flip-flop is put into the 1 state. The 1 state is arbitrarily defined as the state when pin 2 is high and is distinguished by a neon on pin 2.

The plate of a gate tube goes to the plate of the flip-flop to which information is being transferred; the gate grid is attached to the grid of the flip-flop from which information comes. When the gate cathode is lowered, the gate tube conducts if the grid is high and changes the second flip-flop if it is connected to the high plate.

This means that the second flip-flop must be in the proper state for receiving the gated information. Suppose a down right gate is wanted. First,  $F_3$  is cleared to the 0 state by lowering pin 2, thus making pin 1 high. Then the cathode of  $G_R$  is lowered. If  $F_1=0$ , pin 6 is low,  $G_R$  does not conduct, and  $F_3$  remains in the 0 state. It is thus the same as  $F_1$ . On the other hand, if  $F_1=1$ , pin 6 is high

and  $G_R$  conducts. This causes pin 1 of  $F_3$  to fall and turns  $F_3$  to the 1 state. Therefore  $F_3$  is the same as  $F_1$ .

The gating up in the registers is similar to the gating down except that only one "up" gate is ever used. This results in an extra set of gates which are not needed for shifting operations and are thus available for other use.

Access to the memory is in parallel from the accumulator and information from the input is supplied serially to the accumulator, utilizing the shifting properties of the register to put it in.

Similarly, the output is made serially from the arithmetic register, it being possible for the memory to communicate with this register.

The adder is a Kirchhoff adder. It is basically the same as that in the Institute for Advanced Study machine, but it differs in detail, largely because of the difference in power supplies. The addend and augend digits control gates from two constant current sources which can allow current to flow through a summing resistor. The carry from the preceding stage controls the input voltage to the summing resistor. There are four possible voltages across the summing resistor, depending upon whether the sum at that particular stage is 0, 1, 2, or 3. If it is either of the latter two, a carry is produced for the next stage.

It may be seen in Figure 4 that the summing resistor is a 10,300-ohm resistor and the constant current sources are cathode followers supplying 4.85 milliamperes. The carry causes the input voltage to the 10,300-ohm resistor to

Table I. ORDVAC Characteristics

|                                                                 |                                 |
|-----------------------------------------------------------------|---------------------------------|
| Machine type.....                                               | Parallel, Asynchronous          |
| Register capacity.....                                          | 40 binary digits                |
| Memory capacity.....                                            | 1,024 words of 40 binary digits |
| Adder carry time.....                                           | 9 1/2 microseconds              |
| Allowed carry time.....                                         | 13 microseconds                 |
| Addition time.....                                              | 42 microseconds                 |
| Multiplication Time (all ones, positive multiplier).....        | 1,000 microseconds              |
| Multiplication time (all zeros, positive multiplier).....       | 570 microseconds                |
| Division time.....                                              | 1,000 microseconds              |
| Memory period.....                                              | 24 microseconds                 |
| Time to load entire memory.....                                 | 38 minutes                      |
| Time to print contents of entire memory.....                    | 38 minutes                      |
| Number of tubes.....                                            | 2,718                           |
| Machine d-c power.....                                          | 8.3 kw                          |
| Machine a-c power.....                                          | 8.8 kw                          |
| Total primary power (including power supplies and blowers)..... | 35 kw                           |
| Kind of input.....                                              | 5-hole Teletype tape            |
| Input system (space is holes).....                              | 5...Sexadecimal                 |
| Output system.....                                              | Sexadecimal Teletype            |
| Number of digits assigned to an order.....                      | 9                               |
| Number of digits assigned to memory address.....                | 10                              |
| Number of orders available.....                                 | Greater than 50                 |

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drop from 210 volts to 160 volts. The result is that the four voltages are in 50-volt steps, being 204, 154, 104, and 54 volts respectively. The time required to propagate a carry through the 40 stages of the adder is  $9\frac{1}{2}$  microseconds.

The digit resolver is required to convert the adder voltages back to digital information. The addend and augend come into the adder from the accumulator and the number register, and the sum is returned to the accumulator after passing through the digit resolver. It is the function of the digit resolver to distinguish those sums having the digit 1 left in a stage from those having a zero. The former are the quantities 1 and 3 (having binary representation 01 and 11) while the latter are the quantities 0 and 2 (having binary representation 00 and 10). The digit resolver thus furnishes 0 volts for the accumulator if the adder output is 204 volts or 104 volts and furnishes -40 volts if the adder output is 154 volts or 54 volts.

## Input-Output

The input-output equipment consists of modified Teletype units of the kind which were developed by the Bureau of Standards for the Institute for Advanced Study. It operates at standard Teletype speed, although the input has frequently been operated at about twice standard speed. The input is by means of standard 5-hole Teletype tape of which four holes are used to represent numbers in the sexadecimal or base-16 number system by means of a binary code. A 40-digit binary number is then written as a 10-digit sexadecimal number.

Output from the machine can be either to a tape punch or to a teletypewriter. In either case it is in the sexadecimal system, although if it is desired the output can be programmed and converted by means of a simple routine to decimal quantities.

The input and output are slow and in this facility the machine is unbalanced for some types of problems. At present consideration is being given to speeding both operations up by a factor of about five, but beyond this no immediate increase in speed is contemplated.

## Memory

The memory is of the electrostatic "Williams" type using 40 3KP1 cathode-ray tubes.<sup>2</sup> Each cathode-ray tube stores 1,024 binary digits and can receive binary information from one digit of the accumulator and can release its stored

*The following introductory remarks by Dr. Herman Goldstein of the Institute for Advanced Study, preceded the presentation of this paper:*

Primarily, I wanted to say just a few words about the over-all history of the computer field with minor remarks about some of the things that characterize the machines that Dr. Meagher is going to discuss.

The history of the subject is extremely ancient. There has been and always will be a great need and desire not only in the obvious field, such as engineering, where answers are wanted for quite specific and quite clear reasons, but also in both pure and applied mathematics for results of an essentially computational nature. The desire to compute, then, is very old, but the mechanisms, as we well know, have been rather slow in development in any substantial way, and any of the things of the sort we are interested in can be traced to the confluence of two evolutionary streams in the last war. On the one hand, there was a development of electronic techniques in radar guidance and, on the other hand, an extremely pressing need among mathematicians for practical results. I think our present field of modern computation represents the confluence of these two evolutionary streams. But I would like to say a word about the particular thing which I think makes it possible.

Clearly, what one does in a computing machine is to represent mechanistically what a human computer performs. If it were not for the deep functions of the human intellect we would never be able to produce a machine. Fortunately, if one looks at what goes on when one does a computation, he finds it is possible to relate or resort to the ordinary vocabulary and transmit it to a computer in a dozen or so different words. Also there are problems of analysis characterized by this fact: that the total set of instructions in the "Pidgin English" of a dozen or so words, would run roughly to one printed page of instructions. One wants then to do this same page over and over again, perhaps each time changing some of the parameters which enter into the page. Therefore, it is possible to mechanize computational work and it is this fortunate fact, I think, which is the key to

the whole success of the modern work from a logical level, at least.

Now, a word about the type of machines which Dr. Meagher is going to describe. It is true, there are a fair number either built or being built. All differ in certain respects but are of sufficient fundamental likeness that it is possible for me to say a word about them collectively, and for Dr. Meagher to essentially describe them all in describing the one at the University of Illinois.

The first thing about these machines I would like to mention is that they operate in a binary number system as distinguished from decimal machines. I do not particularly want to go in to processing methods and number bases, and of course the human does operate at base ten, but it is difficult to understand why there is any necessary reason for a mechanism to operate in the base ten. Therefore, one asks what is the best number of base to operate from? One thing that immediately strikes one—all machines have a logical and arithmetical part. The nature of mathematical logic is its binary character. So there is some reason for feeling the binary system has a certain advantage from that point of view. From the point of view of the arithmetic, the fact is that most of the units that one can produce electronically are fundamentally binary in character and to use another number base, such as base ten, one has to pyramid them. There is necessarily a certain wastefulness in such operation, because it takes four binary devices to produce a decimal digit. So one obtains, essentially, using groups of four binary devices, the ability to build up a decimal system. Since in this case it is possible to recognize 16 states and one uses only 10—six are lost. But I will not go into the subtleties that go into this machine. Suffice to say, it is binary. Secondly, it is parallel, namely that all of the digits of two numbers are operated on simultaneously instead of starting seriatim with a pair and then a pair, et cetera.

The third classification is that these machines all use Williams' tubes; all use 40 of them in parallel, I believe. That is, all the deflection plates are swung in parallel with one digit for each of the 40 tubes. Some use 2-inch, some 3-inch, some 5-inch tubes.

I think this, by and large, describes the broad features of this type of machine.

information to the corresponding digit of the arithmetic, number, or order registers. Thus the total storage is 1,024 words of 40 binary digits. A slave cathode-ray tube and a 40-position switch are provided so that the contents of any one of the operating tubes can be viewed at one time. The cathode-ray tubes are operated with their deflection plates and second anodes at about 150 volts positive with respect to ground and with their cathodes at about 1,900 volts negative with respect to ground, giving an accelerating potential of about 2,050 volts.

Each cathode-ray tube is mounted in a horizontal position with its own shield consisting of a layer of copper, a layer of mu metal, and then a second layer of copper and a second layer of mu metal. Each cathode-ray tube is provided with an adjustment for intensity, focus, and astigmatism.

Associated with each memory tube is a chassis which can be seen in Figure 2 and which contains a 4-tube "video" amplifier with a gain of about 50,000 for a 1.5-microsecond pulse. The chassis also contains the logical circuit to provide for regeneration in the usual way and

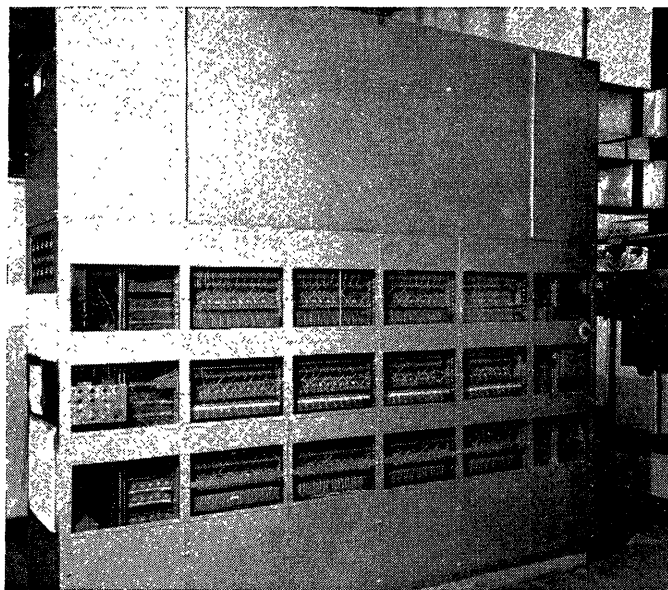


Figure 1. A front view of the ORDVAC showing the registers

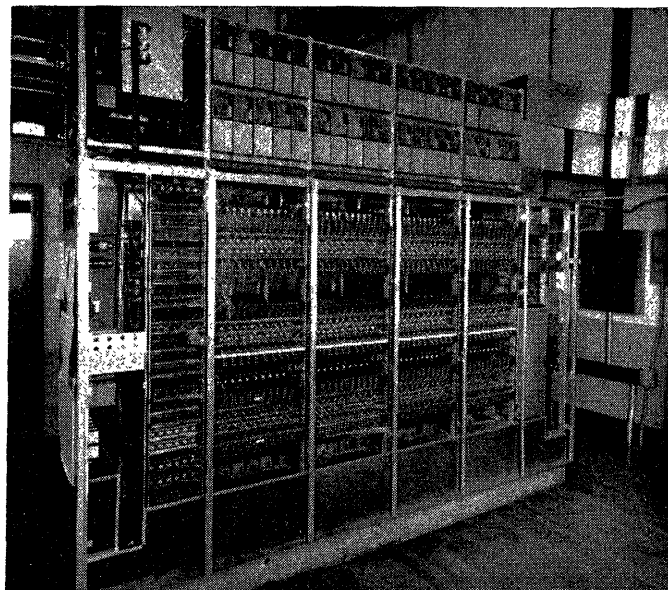


Figure 2. A front view of the ORDVAC without covers. The upper section contains the memory composed of 40 3KP1 cathode-ray tubes and their associated chassis

for transfers of information to and from the appropriate registers. The output of this chassis is capacitively coupled and then d-c restored to the grid of the cathode-ray tube. The "2-dot" system of storage is used where the sensing position of the beam is called the dot and the other position is called the "dash." The beam is on for about 1.2 microseconds in the "dot" position and about 2.5 microseconds in the "dash" position. The period between cycles of memory operations has commonly been set at 24 microseconds, although all of the useful operations, including the clearing and gating of information, require about 16 microseconds.

The voltages for the deflection plates of the cathode-ray tubes which specify the position of the beam for each of the 1,024 memory addresses are obtained from an "address generator" which converts ten binary digits into 32 vertical positions and 32 horizontal positions by adding the currents from five binary stages for each. Some special care has been taken to insure that the deflection voltages are free from noise by providing special regulation for two of the voltages and by suitable limiting of the voltages on the wires which carry the ten binary digits to the "address generator."

It seems appropriate to summarize the useful performance of the memory with the following remarks.

It is necessary to check the adjustments of each memory tube daily by observing the video signals on an oscilloscope when the memory is in active use so that the signals corresponding to both dots and dashes can be seen. It is usually necessary to adjust about two or three

intensities each time this is done.

We are currently using 40 3KP1 tubes having a total of about 50 flaws on their phosphor screens which are bad enough to prevent satisfactory storage. About 15 of the 40 tubes have no flaws of this type. A process of tube selection is presently under way to reduce the flaws but the present 40 tubes represent the best 40 out of about 175 tubes. Currently we are operating by moving the raster on all 40 tubes in such a way that it does not use any of the flaw positions.

If one defines the "read-around-ratio" as the number of times that a dash can be read into or out of a single address without causing a nearby dot to change to a dash, and assuming that no regenerations occur, then it is possible to state that out of the 40,960 storage locations about three have a read-around-ratio as low as 20, about 20 have a read-around-ratio as low as 32 and about 200 have a read-around-ratio as low as 50. The way in which these results have been obtained is explained in a later section.

### Control

As has been mentioned the control of the ORDVAC is direct coupled and asynchronous. Rather than have an external timing device for signalling each of the operations it is to perform, it operates by having each of its operations signal the one to follow. The speed with which it operates is therefore determined by its own ability to carry out the sequencing operations which are required.

Since it is direct coupled the machine will simply stop if no signal is supplied for an operation. On the other hand, the machine can be made to stop by deliberately inhibiting a signal.

Let us consider one flip-flop F and two operations A and B as shown in Figure 5. When F is in the 0 state, A occurs and causes F to turn to 1. This initiates B which returns F to 0, and the sequence is repeated. Thus one flip-flop can be used to sequence a pair of operations. In the same way,  $n$  flip-flops can be used to sequence  $2^n$  operations.

There are obvious defects in the simple example just cited. In the first place, the signal from A may turn F to 1 before A has had a chance to do its work. If this happens, the enabling signal to A will disappear and A will never be completed. Secondly, B may take place while A is still on. This could have disastrous results if the two signals were related, as, for example, when A clears a register and B gates information to that register. If B gates while A is still on and, worse still, if B never gets really turned on, the information would never be gated.

In order to prevent failures of these kinds, safety circuits have been designed into the ORDVAC control. These circuits do the following things:

1. They make the turnover requirements for control flip-flops more stringent than the turnover requirements for the flip-flops being controlled. Therefore, if the latter do not turn, neither will the former, and the machine will stop.
2. They require that when a control flip-flop is being turned over and sensed, the

signal from it be used only when it has been positively turned.

3. They require that before an operation in a sequence can occur the previous operation must not only have taken place but that it must also have been turned off.

Examples of circuits of these kinds may be found in the shift sequencing control. Shifting in the ORDVAC requires four operations, two clears and two gates, and these are sequenced with two flip-flops. Let us take a look at one of these flip-flops, the one which is turned over by a register gate bus. But first let us recall the register gating.

When the cathode of the gate tube is pulled down from +10 volts to -10 volts the contents of the second flip-flop will transfer if the grid was positive. Flip-flop grids are either 0 volts or negative about -20 volts. Since the cutoff of the 6J6 used for gating is about -4 volts, the gate will start to conduct when the cathode is at about +4 volts, and the transfer will have occurred by the time the cathode gets to 0 volts.

The same gate bus which pulled down the gate cathodes in the register is used to turn the control flip-flop F (Figure 6). But now the gate tube G is pegged at -5 volts instead of at 0 volts. This gives a 5-volt safety margin in the turnover of F, and it can be safely assumed that the register flip-flops turned over if F did.

Negative signals are used in nearly all of the ORDVAC control. Before F was turned, pin 6 was negative. After it is turned by G, pin 5 is negative, and one might be tempted to take the

signal for the next operation from here. But this would be a mistake, for pin 5 might go far enough negative to initiate the next operation before F is safely and permanently turned over. Therefore the signal will be taken from the positive-going grid 6 which is the last moving element of F. It will be sensed with the inverter  $N_1$  which is built just like F. Because of the cutoff properties of  $N_1$  it will not conduct until the grid gets up to -4 volts, and by then we know that F is safely over. The output of  $N_1$  therefore says that the register gate bus has gone down and that F has been turned over. The turnover of F will shut off the gates in the register.

We still need to know that the gate bus is back up again before proceeding with the next step. This information is obtained from the inverter  $N_2$ . With pin 5 pegged at +5 volts, the signal from  $N_2$  will not be negative until the gate bus is safely off again. The outputs of  $N_1$  and  $N_2$  then go to the "and" circuit A which starts the next operation when its cathode goes negative.

This is the kind of philosophy which has prevailed in the design of the control. Throughout the control an effort has been made to assure the safe operation of each step. If any step should fail, the result is not a loss of the information in the register but merely a "hanging up" of the machine. The control waits until the proper enabling signal comes along, and then it proceeds. This kind of construction makes it possible to test the operation step by step by putting switches in appropriate places so that

the turnover of flip-flops can be controlled. One such place is in the cathode of the gate turning over the flip-flop F in the previous example. If this switch is open, the register gate will not turn off and the machine will wait until the switch is closed.

A price must be paid for these safety features, and the price, of course, is speed. The machine will run faster if it is not necessary to wait for checks on the operation. It will also run faster if operations are done as much as possible in parallel. Here again, although the ORDVAC is a parallel machine, a price has been paid in speed for convenience in doing certain control operations sequentially rather than in parallel.

The ORDVAC memory is synchronous with a period of 24 microseconds. When the control is carrying out operations which do not involve the memory, it works independently while the memory regenerates its storage locations. But if an operation requires use of the memory, the control and memory must be synchronized for one 24-microsecond interval, called an action cycle. In order to get into synchronization the control furnishes a signal to the memory. Since this signal may occur at any time during the 24-microsecond cycle, the control must then wait for an appropriate memory pulse, the action sense pulse, to come along. When this pulse comes, the action cycle normally takes place. During this cycle information is transferred to or from the memory, the necessary clearing and gating operations for these transfers being executed more or less directly

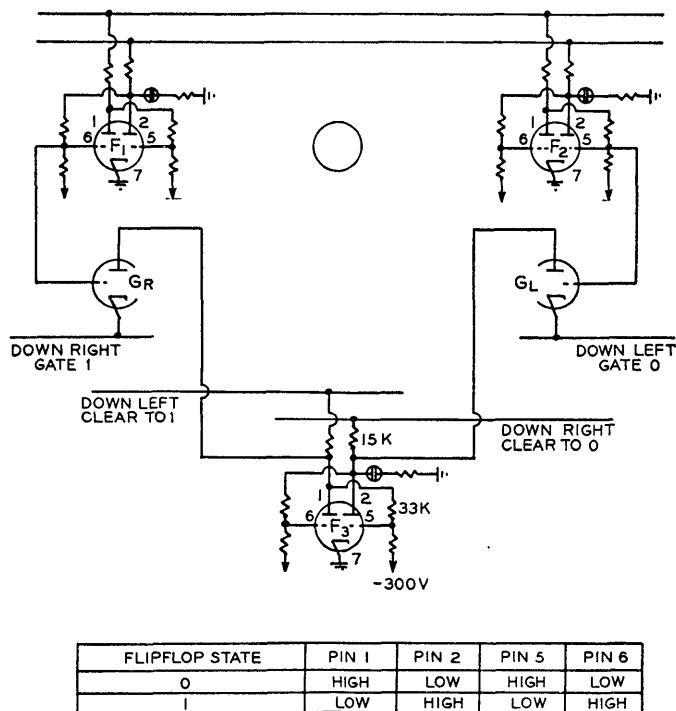
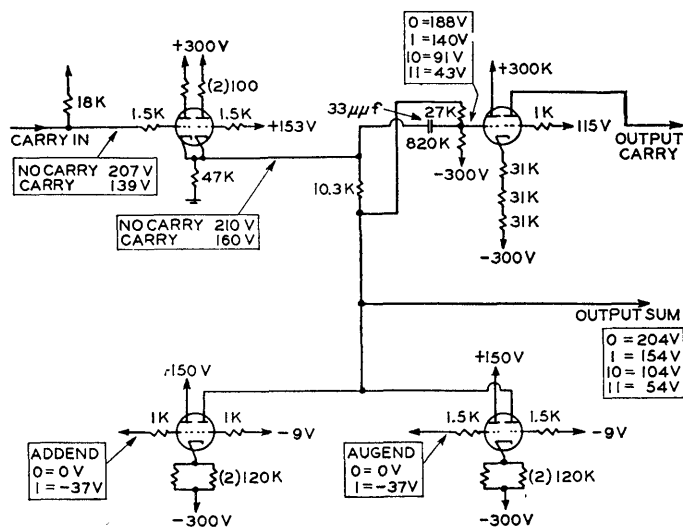


Figure 3 (left). Register circuit showing two upper flip-flops, one lower flip-flop and the "down" gating system

Figure 4 (below). Analogue adder showing input for addend and augend, output, and the carry circuit



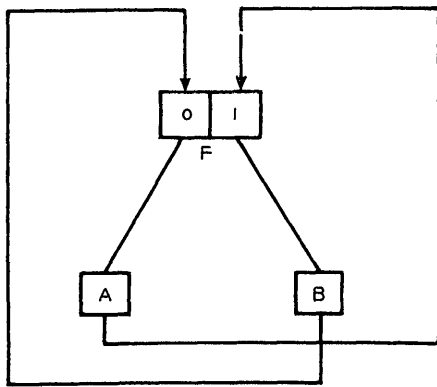


Figure 5. A single flip-flop F used to control two operations A and B in sequence

by the memory pulses themselves. This one case where the memory clears and gates in the registers is the only synchronous control operation in the machine.

The action cycle ends when the next action sense pulse occurs 24 microseconds after the one which began the cycle. At this time a "have used memory" signal goes to the control to indicate that the use of the memory has been completed. The memory returns to regenerating, and the control resumes its asynchronous activity.

The synchronization process requires two flip-flops. One distinguishes between an action cycle and a regeneration cycle. The second distinguishes between the time before the action cycle, when the memory is still regenerating, and the time afterward when it has returned to regenerating but while the "have used memory" signal is on.

A large part of the control is devoted to setting up the proper clear and gate sequences for the registers. Fundamentally, of course, everything that is done in the arithmetic unit must be a combination of sensing flip-flops, adding, clearing, and gating. The decisions about these things are made after certain combinations of digits, called orders, have been decoded with logical circuits. The number of orders that is actually necessary for the convenient coding of the kinds of problems which the ORDVAC is expected to solve is probably between 20 and 30, and this many orders can be described with 15 flip-flops, ten of them being needed for memory addresses. A decoding matrix using five flip-flops would then be used to cause one of 32 wires to be actuated whenever the corresponding order is presented. However (as suggested by the group at the Institute for Advanced Study) since there are 20 digits available for an order of

which only ten are needed to describe the 1,024-memory locations, we can use as many as ten for an instruction. Actually nine have been used with the result that the number of tubes required for decoding has been decreased and the number of orders has been increased. The number of orders which has actually been used in programming is about 50, some of which were not foreseen when the control was designed. A complete matrix is not used, the decoding circuits being made up of a number of submatrices.

The arithmetic of the machine is one which handles numbers in the range from  $-1$  to  $+1$  (actually excluding  $+1$ ) and which carries negative numbers as complements relative to 2. This is the kind of arithmetic which was described by Burks, Goldstine, and von Neumann.<sup>1</sup> However, the methods described by them have not been followed in the arithmetic operations of this machine. In particular, the method by which multiplication is carried out is not used, as far as we know, in any other machine. (This method was suggested by Mr. J. E. Robertson of the University of Illinois.)

Multiplication without roundoff by two positive numbers poses no problems. If an operand  $x$  is negative, the machine holds the number  $2+x$ , and if the sign digit of  $x$  is ignored multiplication by a positive  $y$  gives the result  $xy+y$

Figure 6. Safer way by which flip-flop F can control an operation A

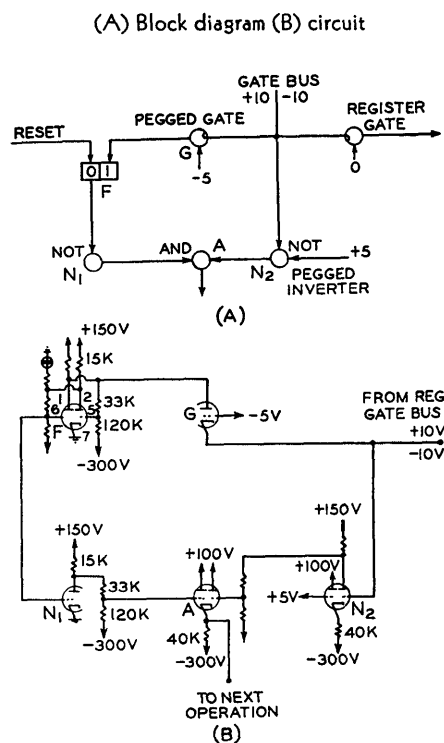


Table II. Multiplication with Negative Multiplicand Showing System Given in Burks, Goldstine, and von Neumann and System in ORDVAC

| Operation                       | Multiplicand | Multiplier Digit | Accumulated Product |
|---------------------------------|--------------|------------------|---------------------|
| Burks, Goldstine, von Neumann   |              |                  |                     |
| (1) Add multiplicand without... | 1            | 0.101            | 0.101               |
| (2) Shift right                 |              |                  | 0.0101              |
| (3) Change sign and shift right | 0            | 0.10101          | 0.10101             |
| (4) Add multiplicand without... | 1            | 1.01001          | 1.01001             |
| (5) Shift right                 |              |                  | 0.101001            |
| (6) Add correction term         | 1.001        | 1                | 1.110001            |
| ORDVAC                          |              |                  |                     |
| (1) Add multiplicand            | 1            | 1.101            | 1.101               |
| (2) Divide by 2                 |              |                  | 1.1101              |
| (3) Divide by 2                 | 0            | 1.11101          | 1.11101             |
| (4) Add multiplicand            | 1            | 1.10001          | 1.10001             |
| (5) Divide by 2                 |              |                  | 1.110001            |

so that subtraction of  $y$  will give the desired answer. If  $x$  is the multiplier, there is no difficulty because  $y$  is available at the end and can be subtracted. But if  $x$  is the multiplicand,  $y$  is lost during the process of shifting to inspect its digits. Hence it must be subtracted during the stepwise formation of the partial products. The method proposed by Burks, Goldstine, and von Neumann which does this, requires varying the gating of digits to the adder as well as making a "correction" at the end.

The ORDVAC multiplication scheme makes no distinction between positive and negative multiplicands. This is accomplished by making an algebraically correct division by two at each step, and always adding the complete multiplicand with its sign if an addition is required. No corrections are required at the end. The same circuits are used as those which carry out the right shift order, this order giving a correct division by 2 in the accumulator. A sample problem may be followed in Table II.

The problem posed by the roundoff, which requires that the product be rounded to a sign and 39 places after the addition of  $2^{-40}$ , has been solved by doing the roundoff before the multiplication begins. If there is no roundoff, the accumulator is cleared and the product  $xy$  is formed. If there is to be a roundoff, the accumulator is cleared,  $2^{-1}$  is gated into it, and the quantity  $xy+2^{-40}$  is formed. Since the accumulator holds only the sign and first 39 digits of the product, it holds the rounded product.

This method of rounding off has the advantage of being fast, because there is no need to do an additional step at the

end which involves waiting for carries in the adder, and it also provides the facility for gating the digit  $2^{-1}$ , into the accumulator for other orders. In connection with a shift order a digit can be put any place in the accumulator without requiring additional memory storage space.

The division process is different from the nonrestoring process described by Burks, Goldstine, and von Neumann and is almost the inverse of the multiplication process.

## Power Supplies

The machine uses about 8.8 kw of a-c power to operate the filaments of the vacuum tubes.

The d-c power consumption is:

|                   |              |
|-------------------|--------------|
| -2,000 volts..... | 0.09 ampere  |
| - 300 volts.....  | 16.0 amperes |
| + 100 volts.....  | 10.1 amperes |
| + 150 volts.....  | 3.8 amperes  |
| + 300 volts.....  | 5.2 amperes  |
| + 680 volts.....  | 0.4 ampere   |

The -2,000-volt and the +680-volt potentials are obtained from vacuum tube regulated power supplies which were built at the University of Illinois.

The intermediate four voltages supply the bulk of the d-c power for the machine and insofar as possible all circuits have been designed to use these voltages directly without additional regulation or "bleeders." In a few cases such as adder circuits "odd" voltages are required and these are furnished by a "bleeder" which supplies voltages for vacuum tube grids where the current drain is very low. These four "main" voltages are furnished by commercially built and controlled rectifier units which are regulated against line voltage changes and fast and slow load changes to  $\pm 2$  per cent.

All of the d-c loads are divided into separate circuits of about 3 amperes each and arranged with individual fuses in such a way that the failure of any individual circuit will open a relay thus turning off a "holding circuit" on all of the d-c power.

## Operation of the ORDVAC

To date no mathematical problems other than trivial ones have been solved by the ORDVAC. A considerable number of test routines have been run, some of them having 100 words or more and using some 25 of the available orders of the machine. Most of the more complicated routines have been concerned with testing the memory for read-around-ratio, although they serve also, of course, to test the arithmetic unit and control at the same time.

One of the more useful routines is one which tests every storage location of the memory for its read-around characteristics. The raster now is arranged so that the spots form hexagons. The routine is put into the top of the memory and causes the first spot in the lower half to be bombarded a given number of times with dashes. It then inspects the surrounding spots, which have been previously cleared to dots, to see if any have become dashes. If so, it causes the tube number (0 to 39) and address of the bombarded spot to be printed. This is repeated for all of the addresses in the lower half of the memory. The routine then transfers itself to the lower half and inspects the upper half in the same way. At the end of the complete inspection it changes the number of bombardments and repeats the process.

A program for the over-all testing of the machine has been run. This program generates a set of 352 pseudo-random numbers  $b_i$  and stores them in successive memory locations. It then performs multiplication and divisions of  $b_i$  by  $b_{i+1}$ , checking multiplication results by multiplying in both directions and comparing and checking division results by multiplication. If all of these are correct, the numbers are transferred to 352 other locations and the transfers are checked. If there is no failure,  $i$  is increased by one and the process is repeated, transferring each  $b_i$  to a different address this time. When  $i$  reaches 352 (a major cycle), the process starts again.

At any failure the machine prints pertinent data and stops. Upon being started again it goes through a subroutine which checks all of the principal orders, trying to find the cause of the first failure. If an order fails, the machine again furnishes information and stops.

This program ran continuously for 12 hours and then failed when one memory location changed from a dot to a dash.

The machine has been "on" about 2,900 hours and during this time about 190 tube failures have occurred. However, it should be remembered that the machine has "grown" during this time and only about 1,000 of 2,700 tubes have actually been in service during the full interval.

The cathode-ray tube life is inadequately noted by our system because of the selection process which has been in progress.

## Conclusion

The work on the ORDVAC started in the spring of 1949 and has been supported by a contract from the Ordnance Department for \$250,000. The University of Illinois has provided a comparable sum which is to lead to a second machine. The Ordnance contract was concluded on October 31, 1951 and since that time the ORDVAC has been under test. It is currently expected that it will be moved to the Ballistic Research Laboratories at Aberdeen about February 1952. Its presence at the University until then allows a further understanding of its operation and use, and aids in the work on the machine for the University of Illinois.

## References

1. PRELIMINARY DISCUSSION OF THE LOGICAL DESIGN OF AN ELECTRONIC COMPUTING INSTRUMENT, A. W. Burks, H. H. Goldstine, John von Neumann. Institute for Advanced Study (Princeton, N. J.) June 1946.
2. A STORAGE SYSTEM FOR USE WITH BINARY DIGITAL COMPUTING MACHINES, F. C. Williams, T. Kilburn. *Proceedings, Institution of Electrical Engineers* (London, England), volume 96, part II, number 50, April 1949, pages 183-200.

## Discussion

**Charles Corderman** (MIT): First, speaking of the tubes you have in the ORDVAC, what is the consistently obtainable read-around ratio, and of the tubes that do not show flaws, what is the average read-around ratio?

**R. E. Meagher:** We usually do not check the average read-around ratio because the

lowest read-around ratio is the one which would limit the use of the machine. Testing any one address may give read-around ratios of several hundred, but we have to impose an operating limit of something like 16, at this time.

**David Mayer** (Philco Corporation): I would like to ask for a definition of "read-around ratio". My second question is, are you using crystals in the machine? Third, how do you perform your division and sub-

traction operations?

**R. E. Meagher:** If the read-around ratio is " $n$ ", it means that we can write a dash or read a dash " $n$ " times at that particular address without causing an error at any nearby address or any other addresses. That means when I say the read-around ratio is 16, there is some address on some tube which will fail when you hit it 17 times. We have no crystal diodes at all in the machine.

Division is carried out in the machine by a

process which may be thought of as being the inverse of the multiplication process which you saw. If we confine our attention to the division of one positive number by another, then at each step of the process we form a partial remainder which is held in the

accumulator. At the beginning we have the dividend in the accumulator. We subtract the divisor from the partial remainder to form a new partial remainder. If the sign of the difference is positive, the new partial remainder is the difference shifted left one

place and the quotient digit is a 1. If the sign is negative, the new partial remainder is the old partial remainder shifted left one place, and the quotient digit is a 0. The quotient is shifted with the accumulator, and digits are inserted at the right.

## Design Features of the ERA 1101 Computer

F. C. MULLANEY

**T**HE ERA 1101 computer is a single-address binary-system parallel computer using magnetic drum memory. The word length is 24 binary digits, equivalent to seven decimal digits plus sign. The logic is quite conventional.

A machine instruction consists of an operation code plus one execution address. The execution address usually specifies the location of an operand or the place where a result is to be stored. There are a total of 38 different operations which may be grouped as follows:

Ten arithmetic operations, including regular and special additions and subtractions, divide, and multiply.

Thirteen "insert" or transmissive operations.

Four "jump" or transfer operations to allow interruption of the instruction sequence in progress.

Four manipulative aids such as logical multiplication.

Two shifting operations, each shifting left one of two registers.

Two output operations; print and print punch.

Three stops; optional, intermediate, and final.

The memory element is a magnetic drum with a capacity of 16,384 words, each 24 binary digits long. The drum, which is  $8\frac{1}{2}$  inches in diameter, rotates at 3,500 rpm. The resulting surface speed of 1,600 inches per second, together with a peripheral spot density of 80 per inch, produces a basic pulse rate of 125 kc for the memory section of the machine.

Although the random average access time is 8 milliseconds, an average access time of less than 1 millisecond can be obtained by placing the orders and operands in locations on the drum which will permit a number of references in the same drum revolution.

The arithmetic section consists of the "X" and "Q" Registers and the Accumulator. The "X" Register, 24 bits long, functions as the repository for multiplier, divisor, augend, and subtrahend. The "Q" Register, also 24 binary digits in length, possesses shifting properties. This register contains the multiplier during multiplication and the quotient after a division. It also may be used as a rapid-access 1 word storage. The principal arithmetic register, and the place where the actual arithmetic is performed, is the 48-place Accumulator. It possesses subtracting and shifting properties.

The number representation is in a one's complement system in which the highest order binary digit designates the sign of the number. Negative numbers are represented as complements on  $2^n - 1$ , where  $n$  is 24 or 48 depending on which register contains it and on whether single or double precision operation is being used.

The basic clock rate at which the control and arithmetic systems function is 400 kc. The time necessary for addition or subtraction is 96 microseconds. This time includes procurement of both operands and the next instruction from the magnetic drum memory and assumes that the drum addresses are placed to obtain minimum access time. The cor-

responding time for division is 415 microseconds and for multiplication, 352 microseconds.

The computation and control sections operate asynchronously with respect to the memory. Once a storage reference has been initiated by main control, further action in this section is suspended until a "resume" is signalled by the control circuitry of the memory system.

The main sequence control receives the operation code and issues the necessary operation pulses to perform the main steps involved in the particular instruction being processed. To control, the more complex arithmetic operations, such as shift, multiply, and divide, an auxiliary control system is employed. It is known as the arithmetic sequence control.

The machine may be manually controlled from two locations. The operator's control panel contains a minimum number of controls and indicators for operating the machine. The maintenance control panel contains a complete display of indicators and a sufficient number of switches for complete control of the equipment for test and trouble diagnosis.

The input medium is a photoelectric paper tape reader. Standard 7-channel perforated paper tape is used, six channels of which are used for information. Four lines, therefore, contain a 24-bit word. The seventh channel contains the coded loading instructions. This code is used to direct the operations necessary to assemble the 6-bit word pieces into the standard 24-bit size, and store them in the proper location on the magnetic drum. The loading rate is 35 words per second. At this rate, the entire drum could be loaded in less than eight minutes if desired.

The output section consists of an electric typewriter and paper tape punch. The maximum output rate is about seven characters per second.

The machine logic, while not basically novel, has certain distinctive features which are worthy of mention. Two

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