THE IBM MAGNETIC DRUM CALCULATOR TYPE 650 ENGINEERING AND DESIGN CONSIDERATIONS

E. S. Hughes, Jr.
International Business Machines Corporation
Endicott, New York

Resume

This paper covers the engineering principles and design considerations given to the components that are used in the International Business Machines Corporation's Type 650 Calculator. The factors that led to the selection of the particular systems and components are discussed, rather than the way and manner in which the calculator functions.

The general topics that are covered include a review of the machine as a unit, self-checking features, and storage systems. Self-checking codes supplemented by control checks to form a self-checking system are covered in some detail.

The storage system is broken down into two types - main storage and buffer storage, with comments on their adaptability and flexibility in the complete system. Significant test data are presented.

The IBM Magnetic Drum Calculator Type 650 is a stored program, two address calculator, intermediate in speed, capacity, and cost. Its comprehensive order list, punched card input - output, memory capacity, and self-checking features give it the flexibility that is required in both the commercial and scientific field. Its moderate cost, ease of operation, and small size places it within the reach of many users.

Machine specifications and special features include:

1. Two thousand words of storage on the magnetic drum with an average access time of 2.4 milliseconds.
2. Input of 200 cards per minute with full 80 columns.
3. Output of 100 cards per minute with full 80 columns.
4. 10 X 10 multiplication to give 20 digit product. Average time is 11.6 milliseconds including access times.
5. Twenty digits divided by 10 digits to give 10 digit quotient. Average time is 14.5 milliseconds including access times.
6. Addition and subtraction of 10 digit words to give 20 digit sums. Average time 5.2 milliseconds including access times.
7. Consult storage for both reading and writing -- 5.2 milliseconds.
8. Instructions are stored on the drum as 10 digit numbers plus sign.

An instruction consists of two digits for operational codes, four digits for address of data or alternate instruction address (D Address), and four digits for address of the next instruction (I Address). See Order List, Figure 1.

A seven bit biquinary code is used for input, output, accumulator, and program control. Drum storage uses a condensed five bit code for economy. Information is stored parallel by bit, serial by digit, and word.

A table look-up (TLU) operation is performed automatically with one operation code. An equal or high search may be performed on arguments stored in an ascending order. Related functions may be located by normal programming procedures after a constant has been added to the storage location of the argument.

The built-in, self-checking features include a validity check for number transmission, read-in and punch-out checks, control checks on the program, and timing and synchronizing checks. Figure 2 shows the data flow paths and validity checks.

Figure 3 shows the operator's control console which serves as a comprehensive means for monitoring and manually controlling the operation of the machine.

The storage display lights show the contents of any memory location, or the contents of the program register, distributor, upper accumulator or lower accumulator. The display switch and the address selection switches select the proper location for display. The storage entry switches provide a means for entering information, either in the form of data or instructions, manually into the machine.

The order, address and operating lights indicate the operating condition of the machine. The checking lights indicate the source of a detected error, except for the error sense light which indicates that an error has been detected and a self-correcting routine has been employed. This error sense light can only be turned off manually, and it will remain off only if the error is not repetitive. The address selection switches provide a unique means for choosing key points in "de-bugging" a program. They allow a stop at any desired instruction in particular routine being "de-bugged" by merely setting the switches to the location of this instruction and setting the control switch to the address stop position.

The power requirements are as follows:

Either 208 volts or 230 volts with ± 10 per cent regulation
60 Cycles
Single Phase
100 ampere service
16.8 kilovolts-amperes power dissipation
45,500 BTU/hour heat dissipation

The direct current power is provided by selenium rectifiers with primary power regulated by saturable reactors thus avoiding the need for electronic regulation.

Figure 4 shows the three units that make up the complete calculator. The unit in

the foreground is the Type 533 read-punch unit, the center unit houses the drum, program control, and computing circuits, and the rear unit provides the card scan, translating and power supply circuits.

A broad outline of the complete calculator has been given. With this in mind it is possible to review the calculator from an engineering evaluation of the logic and components used.

The general specifications are that the machine is intermediate in cost and speed, simple to operate, and self-checking.

The self-checking feature determined the selection of the biquinary code. The binary code is excellent for large, high-speed machines where the cost of conversion can be absorbed. The forms of binary coded decimals were eliminated in favor of the positive checking features, and ease of use of the biquinary code, since it closely resembles the decimal code.

Since the biquinary code requires seven bits per digit, there is a question as to its worth because of extra bits that must be stored. When serial - serial recording is used in drum storage, the extra bits of storage cost very little in terms of dollars. However, if the pulse repetition frequency (prf) and bit density remain the same, the drum circumference must be increased thus resulting in an increase in access time. In a parallel-by-bit, serial-by-digit system, the dollar cost increase is directly proportional to the bit increase but the access time remains the same.

The MDC is based on the parallel-by-bit, serial-by-digit system and the extra cost is partially nullified by other means. This is accomplished by taking advantage of the simplicity of the biquinary system as illustrated by a few examples.

In Figure 5 (Operation Code Matrix) it is shown how decoding is eliminated, a timed output is obtained, and grouped signals are automatically available.

In Figure 6 (Static Head Selection) the circuitry for the selection of the forty bands is shown. Since there are 50 words per band, selected on a dynamic basis, this will give a total of 2000 words. The outputs from the address registers energize the three dimensional matrix directly, eliminating the necessity for decoding or buffer amplifiers. This also gives the optimum load distribution since any one line drives a maximum of five intersections. These are only a few of the advantages that are realized due to the simplicity of the biquinary code. Others include simplification of the matrix adder, ease of reading on the display lights, and ease of interpretation by the service engineer.

The selection of a magnetic drum for storage is a natural choice since it offers a large volume of storage at medium access and cost. The details of resolving the size, configuration, frequency, surface speed, revolutions per minute, and bit density present a more complicated problem. It is necessary to determine the frequency early in the design stage since amplifiers and synchonrizing circuits are not readily redesigned for various frequency characteristics. When a reasonable bit density has been established, it,

combined with the chosen operating frequency, will determine the surface speed. The remaining characteristics are merely determined by the access time that is desired. In the MDC design, an operating frequency of 125 kilocycles per second (8 microseconds bit spacing) and 50 bits per inch were chosen.

$$\text{Surface speed} = \frac{1{,}000{,}000\ \mu s}{8\ \mu s \times \text{bit/in.}} = 2500\ \text{in/sec.} \qquad (1)$$

The drum layout is shown in Figure 7. It is readily apparent that once the bit density and frequency (bit spacing) is determined, the remaining characteristics are fixed by access time and capacity.

The mechanical aspects of the drum must also be given special consideration since dynamic balance, concentricity, and long life is of prime importance. The drum assembly is shown in Figure 8. In the simplest sense it consists of a one inch steel tube placed inside a four inch steel tube with a set of precision ball bearings in between. A drive pulley is fastened to the outside tube and it rotates about the inside tube which is clamped to the mounting plate. The assembled drum is then turned in its own bearings which results in almost perfect concentricity. After the unit has been dynamically balanced and mounted in its final assembly (Figure 9), a run out of more than 0.0001 inch is not accepted.

A general requirement in many calculators is several one word buffer storage registers. The Type 650 uses four such registers with specifications illustrated in Figure 10. The scan pulse repetition frequency (prf) is 125 kilocycles per second and the delay varies between +2, and 0 cycles to give a right and left shift. The normal operation is to read out one digit early, delay one digit time, and then store on time. Several types of storage were considered for this application. Tube shifting registers and cathode ray tube storage were too expensive. Core storage, as either a shifting register or static single turn arrays, was compared in cost and operating characteristics to a form of condenser storage.

Both methods are comparable in cost, in an advanced stage of development, and known to operate reliably. After considerable investigation, condenser storage was chosen for the following reasons:

1. Basic components readily available.
2. Large output signals of 30 to 35 volts adaptable to the rest of the calculator units.
3. Matrix drive for condenser storage is less rigid than that required for core storage.
4. Assembly and manufacturing techniques same as those for other electronic components.

The basic circuit[1] and waveform is shown in Figure 11. A stored "1" is represented by no charge on the condenser, and a read-out signal at 1 will produce a differentiated

[1] For other work done on condenser storage see A. W. Holt, "An Experimental Rapid Access Memory Using Diodes and Capacitors", National Bureau of Standards, Washington, D. C.

signal at point "3". If a "1" is to be regenerated a pedestal will appear at point "4" at the same time a clamp signal appears at point "2". As a result the condenser is left uncharged as shown by waveforms 3 and 5.

The circuit in Figure 11 is arranged in a 7 X 12 matrix as shown in Figure 12 to give a one word storage unit.

Self-Checking

The Type 650 has been designed with reliability as a paramount consideration. Conservative circuit design, and components chosen for their high reliability, are employed throughout. The Type 650 also employs built-in self-checking as a supplement which further improves this degree of reliability.

Self-checking within the machine is separated into two categories - validity check and control checks.

Validity Check

The validity check consists of checking all information in the distributor, the accumulator, and the program register for a valid biquinary code. Since all information used in a problem eventually passes through these units, any invalid codes will be detected.

In addition to the above, if any brushes in the card-read-unit are shorted together (touching each other) they will read in double digits and cause a validity check. If a brush has short strands, it will read the same hole twice and cause a validity check.

Control Checks

The control checks are dependent upon the proper combination of signals within the machine, the proper sequence of signals or double circuitry. Some of these are as follows:

1. Meaningless address and operation codes are detected and cause an error indication.
2. Checks are provided to insure that the signal to perform the operation was received and that the operation was completed.
3. The main timing circuits and their outputs to the machine are continuously checked. Any timing error is detected and an error is indicated.
4. The accumulator is designed to detect an accumulator overflow or a division error resulting from more than a ten digit quotient.

Address Selection Checking

Checks are provided to insure that information is read and recorded in the proper location.

Input Checking

Should incorrect reading occur as a result of misfeeding or open or shorted circuits, the error will be detected by a combination of the control and validity checks when the information is processed. In the event that misfeeding results in the card being exactly one hole early or late, too little or too much information will be read as a result of brushes reading the bare contact roll at 9 or 12 times. In this case, the error will again be detected by the validity check. To completely satisfy input checking, the signs, both plus and minus, must be punched in the card.

Output Checking

Punched results are checked by means of double punch and blank column detection. This is equivalent to a validity check. In addition, there are internal machine checks to make sure that the drum is reading out a digit corresponding to the correct punch timing for that digit.

Programming for Error Correction

When the machine detects an error by means of a validity check or a timing circuit check, it is very possible that this error is a random one which will not occur again, or at worst occur very infrequently. Hence, it is reasonable to assume that the machine will probably perform the problem correctly if given a second chance. Therefore, it will prove profitable in some applications to program the machine to repeat a problem in the case of errors detected by self-checking.

In practice, very large problems will be broken up into smaller segments, each segment representing a small part of the whole. In this way, it will not be necessary for the machine to repeat the whole problem, but to repeat only that segment in which the error occurred.

The use of a self-checking code alone is not sufficient to determine a satisfactory system check. Storage selection, translation, synchronizing of input-output, and program control in general are directly dependent upon the clocking system. In the 650 a complete check is applied to the clocking system and is illustrated in Figure 13. The start and completion of each ring is checked by a recorded pulse on the drum. As an example, the word ring would be started by sector pulse "0" and checked by sector pulse "1". Since they are open ended rings, it will be started again by sector pulse "1" and then checked by sector pulse "2". The process is continuous. This check determines that each ring cycle is correct, but in itself is not sufficient to say that each individual output is correct. This check is determined by a characteristic of the latch circuit which is used in the ring. A cathode follower output is used as a feedback on each individual stage, and it must be correct to insure the cycle completion at the prescribed time as dictated by the clock drum recording. This results in a complete check on all the output synchronizing signals that are distributed throughout the machine. Experience has shown that faulty components, located throughout other units of the machine that are associated with synchronizing signals, will usually indicate a timing error on a particular ring and timing output. This aids materially in quickly locating the faulty component.

A complete analysis of the checking system is not within the scope of this paper, nor can its effectiveness be fully revealed until considerable field experience has been realized. It can be stated however, that approximately one year's experience of useful work on an engineering prototype model has shown that no errors, to the operator's knowledge, have escaped the machine detecting circuits. The type of problems that have been applied to the machine do not include programmed checks, and are of such a nature that the results can be checked to a reasonable degree of accuracy.

A total of 2100 tubes and 3600 diodes are used in the production model. The tubes are mounted in a total of 1856 pluggable tube units which consist of 29 different standard types. The diodes are mounted in 516 pluggable diode units of which there is one standard type. The various combinations of logical "and" and "or" circuits are determined by the manner and position in which the individual diodes are clipped in the diode unit.

Tube operating experience on an engineering model during a period of controlled test from December, 1952 through September of 1953 (a total of 1848 operating hours) has shown the following results:

Table I

Tube Type	Number of Replacements	Total Used	Per Cent Replacements
5965	3	765	0.4
2D21	2	120	1.7
12AY7 [1]	7	113	6.1
6211	0	35	0.0
12BH7 (Type 6350 to be used in production model)	2	92	2.6

Diode operating experience during the same controlled test period:

Table II

Diode Type	Number of Replacements	Total Used	Per Cent Replacements
Germanium diodes of several manufacturers	19	2800	0.7

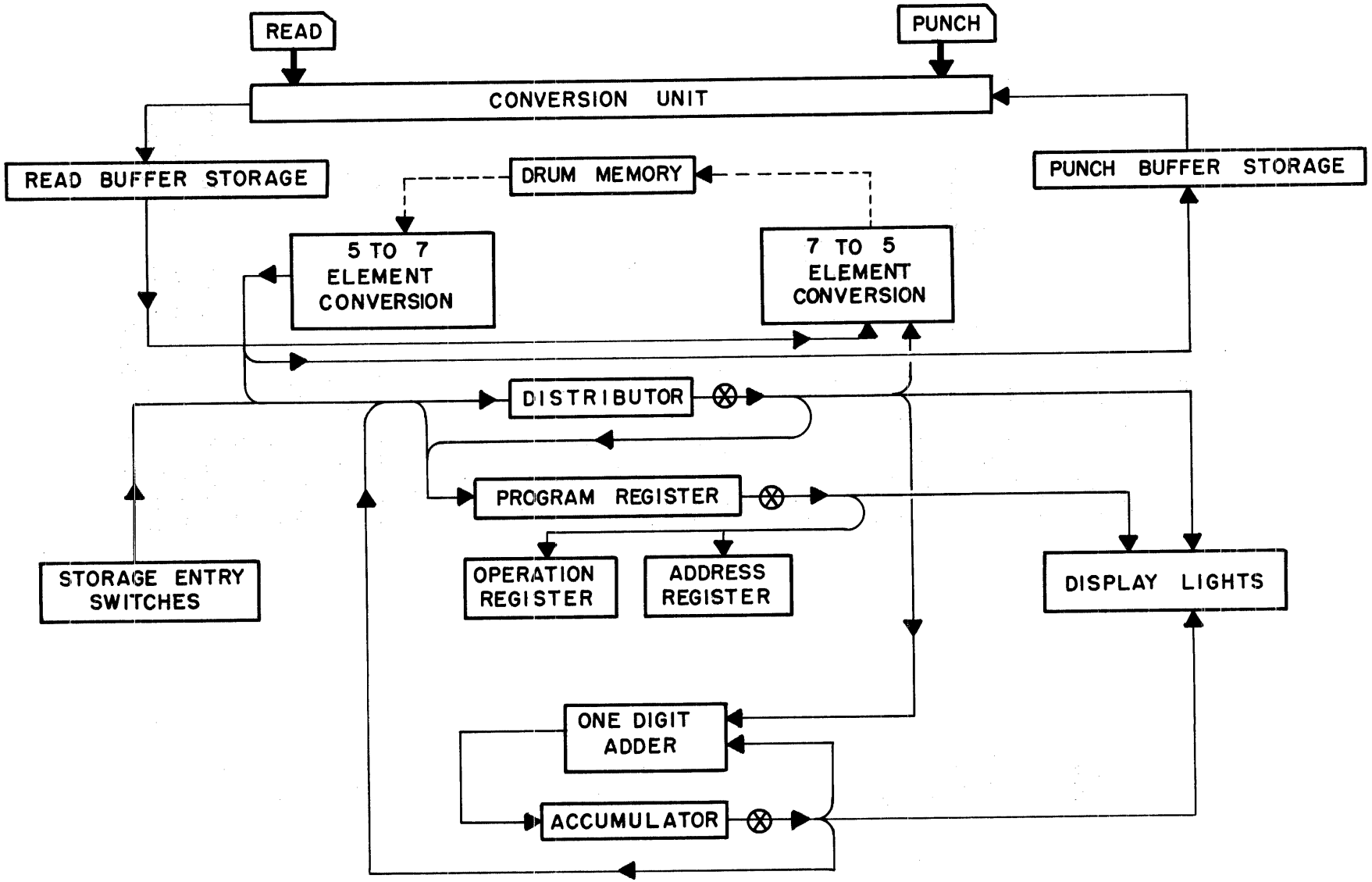
Additional tube types which will appear in the production model include the 5687, 6350, and the 6AL5.

[1] Eighteen Type 12AY7 tubes are used in the production model and may be replaced with the Type 6072.

Order List

Code	Abbreviation	Order
00	No OP	No operation
01	STOP	Stop
10	AU	Add to upper
11	SU	Subtract from upper
14	DIV	Divide
15	AL	Add to lower
16	SL	Subtract from lower
17	AABL	Add absolute value to lower
18	SABL	Subtract absolute value from lower
19	MULT	Multiply
20	STL	Store lower
21	STU	Store upper
22	STDA	Store lower data address
23	STIA	Store lower instruction address
24	STD	Store distributor
30	SRT	Shift right
31	SRD	Shift and round
35	SLT	Shift left
36	SLC	Shift left and count
44	BRNZU	Branch on non-zero in upper
45	BRNZ	Branch on non-zero
46	BR MIN	Branch on minus
47	BR OV	Branch on overflow
60	RAU	Reset-add to upper
61	RSU	Reset-subtract from upper
64	DIV-RU	Divide-reset remainder
65	RAL	Reset-add to lower
66	RSL	Reset-subtract from lower
67	RAABL	Reset-add absolute value to lower
68	RSABL	Reset-subtract absolute value from lower
69	LD	Load distributor
70	RD	Read one card
71	PCH	Punch one card
84	TLU	Table look-up
90	BR D10	Branch on 8 in 10th position of distributor
91	BR D1	Branch on 8 in 1st position of distributor
92-99	BRD2-BRD9	Branch on 8 in 2nd position through 9th position of distributor

Figure 1



NOTES:
1. ⊗ VALIDITY CHECK POINTS.
2. HEAVY LINES SHOW HOLLERITH CODE TRANSMISSION.
3. LIGHT LINES SHOW 7 ELEMENT CODE TRANSMISSION.
4. DASHED LINES SHOW 5 ELEMENT CODE TRANSMISSION.

Fig. 2. Basic 650 circuit

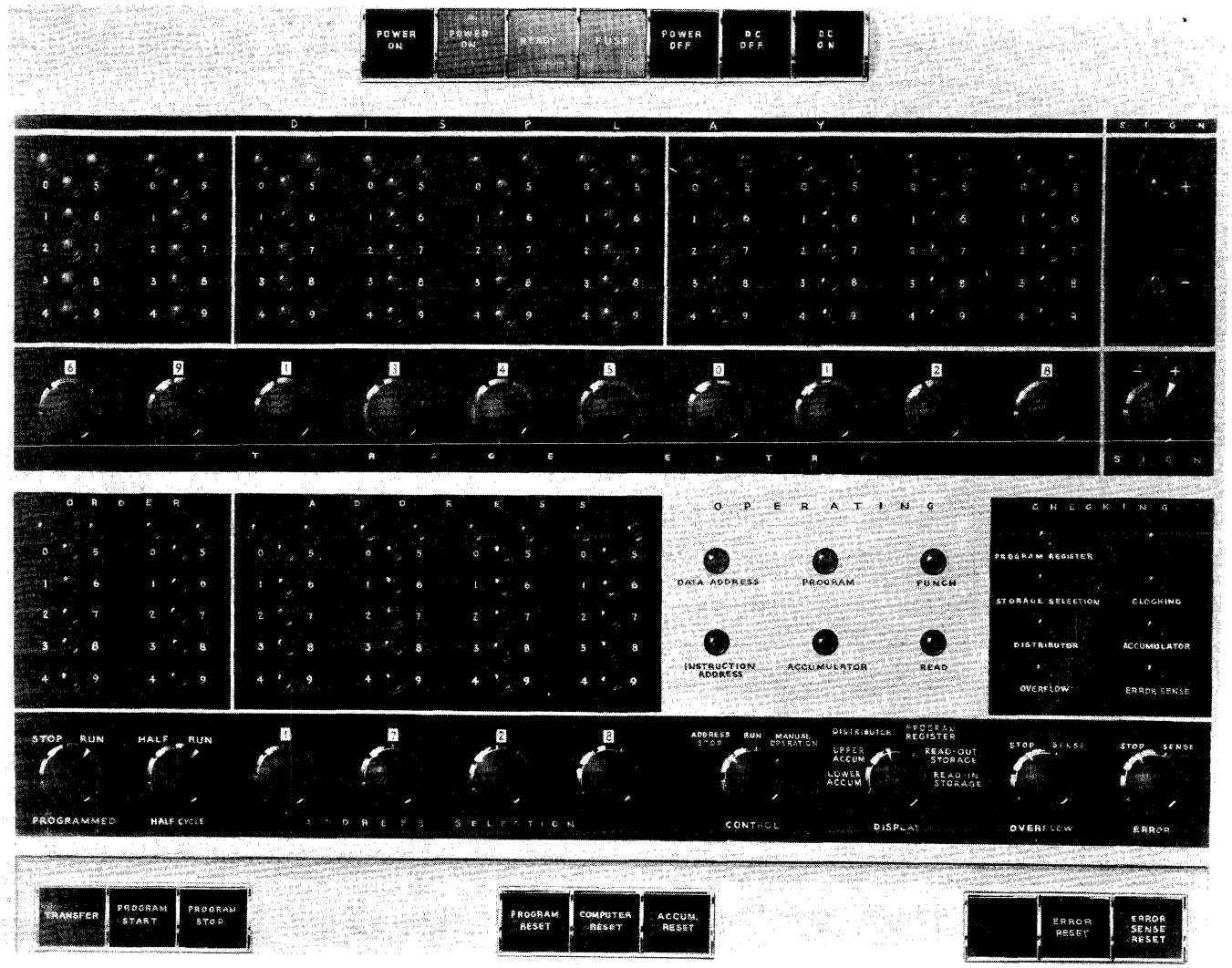


Fig. 3. Operators control console

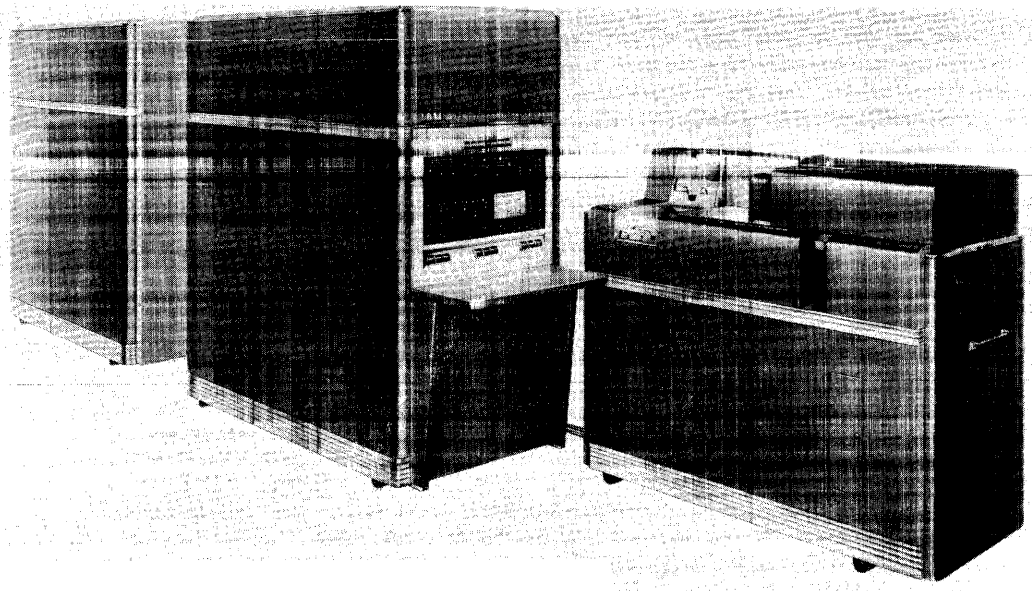


Fig. 4. Magnetic drum calculator type 650

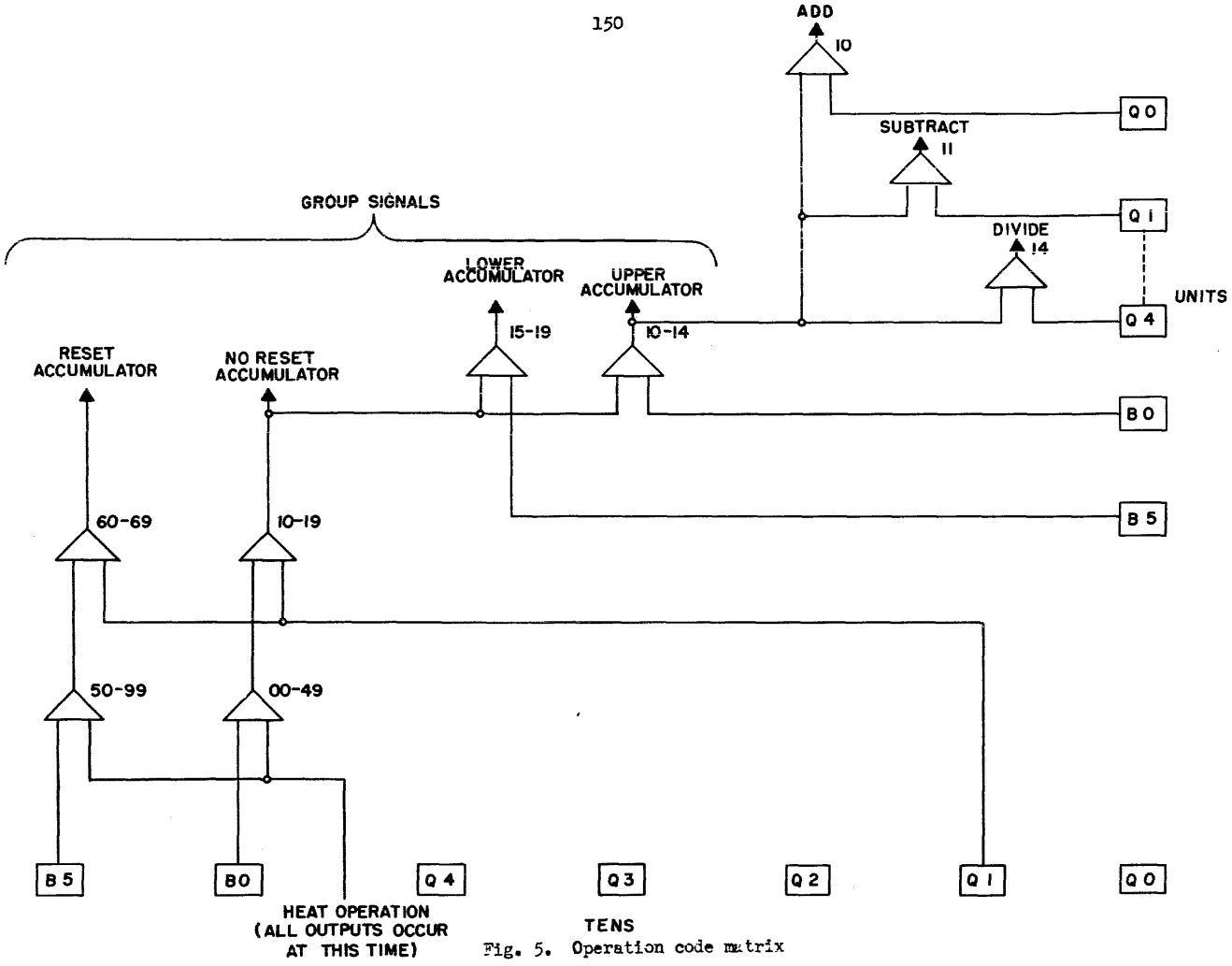
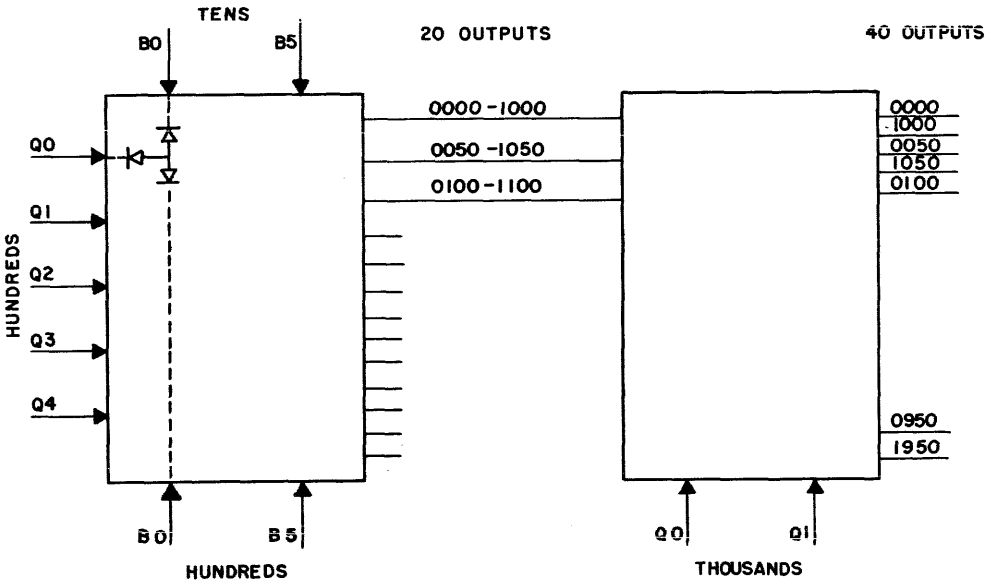
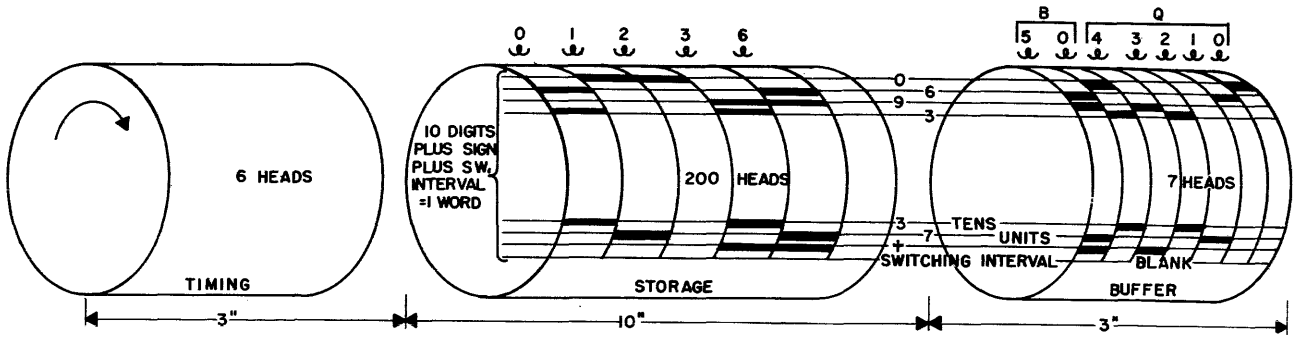


Fig. 5. Operation code matrix



BI-QUINARY	5 X 2 X 2	- 60 DIODES - NO DECODING		60
	10 X 2	- 40 DIODES - 20 DIODES DECODING		60
BINARY CODED DECIMAL	10 X 2	- 40 DIODES - 33 DIODES DECODING		73

Fig. 6. Static head selection



50 BITS PER INCH

8 MICROSECONDS BIT SPACING

12 BITS PER WORD

50 WORDS PER REVOLUTION

50 X 12 = 600 BITS PER REVOLUTION

600 X 0.008 MILLISECONDS = 4.8 MILLISECONDS PER REVOLUTION

$\frac{600 \text{ BITS PER REVOLUTION}}{50 \text{ BITS PER INCH}}$ = 12" CIRCUMFERENCE

$\frac{60{,}000 \text{ MILLISECONDS}}{4.8 \text{ MILLISECONDS PER REVOLUTION}}$ = 12,500 REVOLUTIONS PER MINUTE

$\frac{2000 \text{ WORDS}}{50 \text{ WORDS PER BAND}}$ = 40 BANDS

40 X 5 HEADS PER BAND = 200 HEADS

$\frac{200}{20 \text{ HEADS PER INCH}}$ = 10 INCHES

Fig. 7. Drum layout

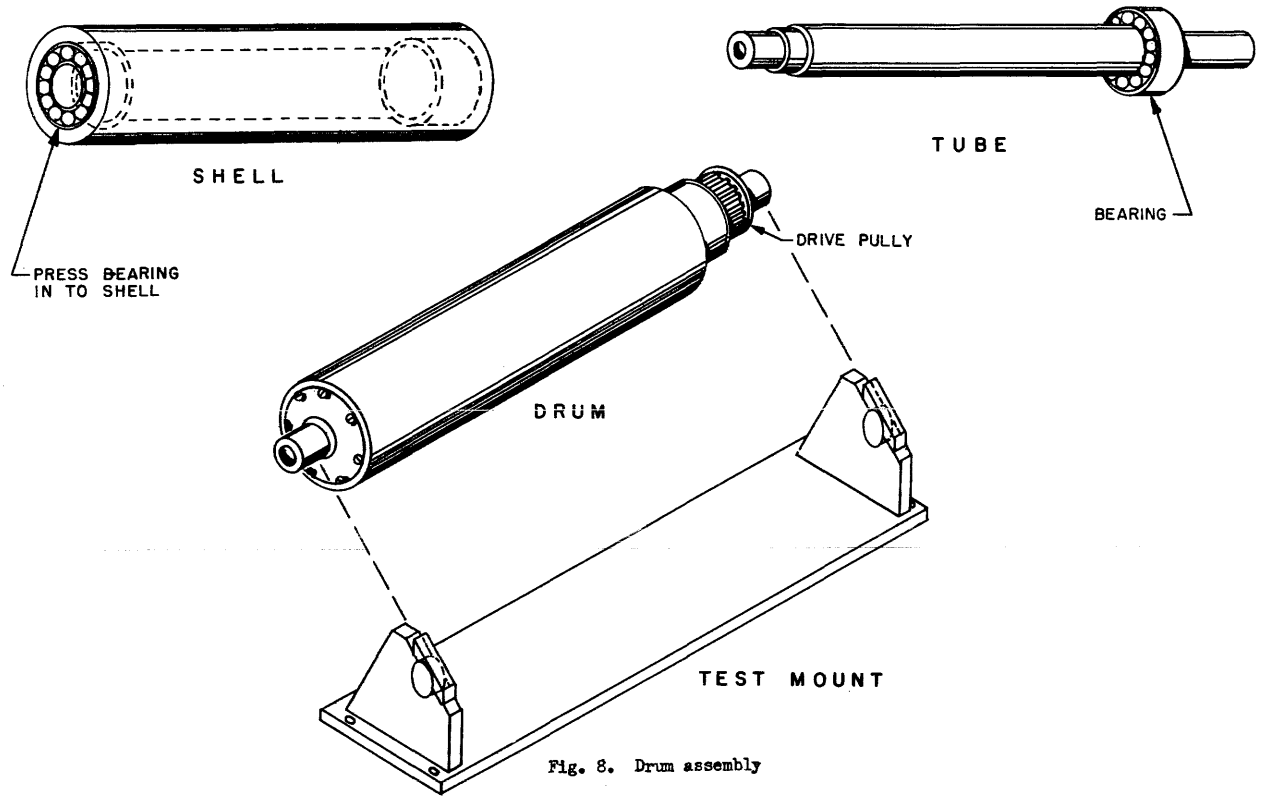


Fig. 8. Drum assembly

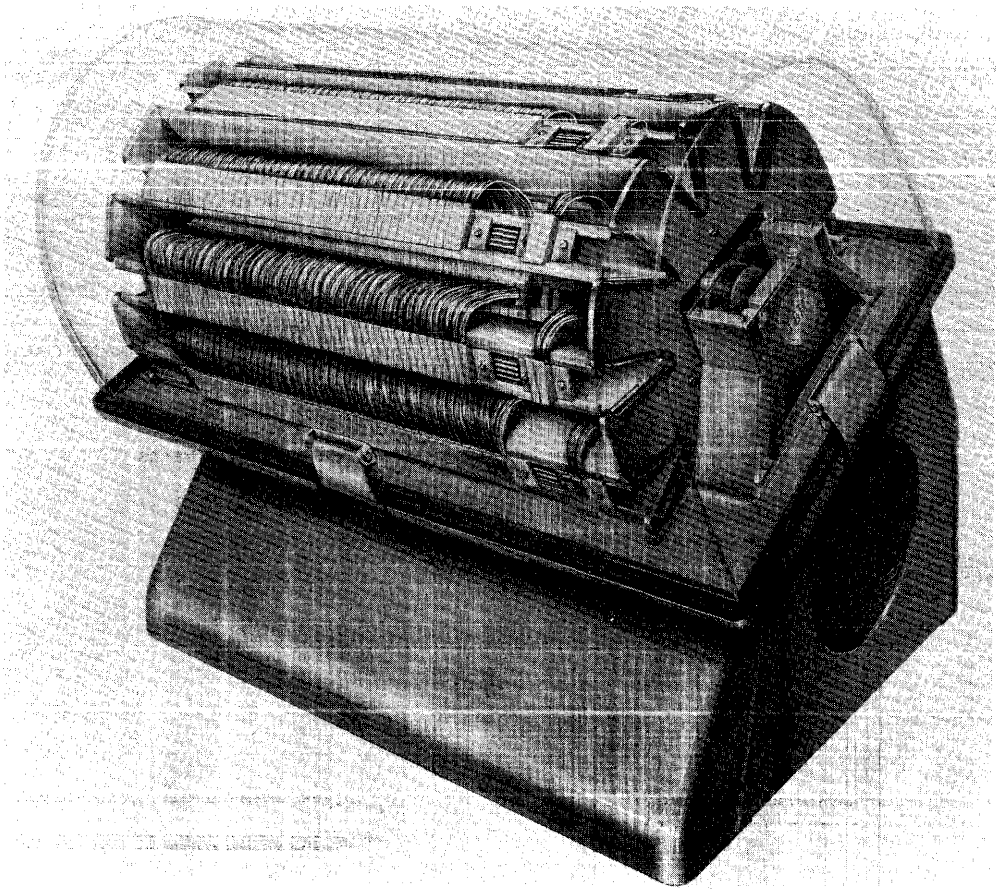
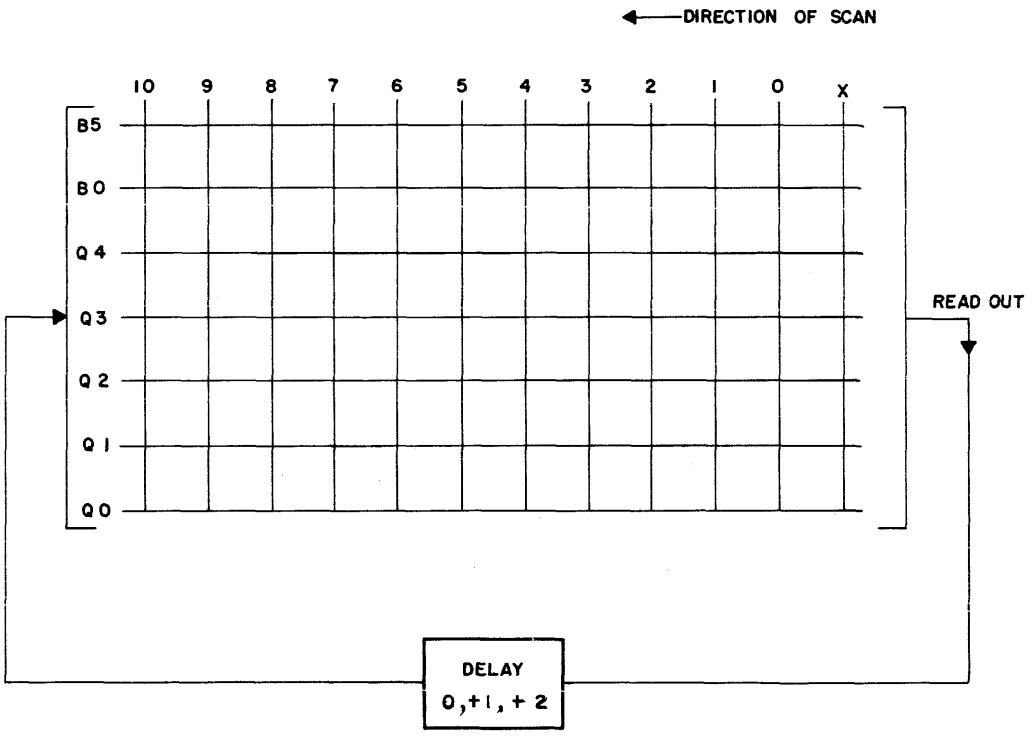


Fig. 9. Magnetic drum final assembly



DIGIT SPACING-8 MICROSECONDS

Fig. 10. Buffer storage specifications

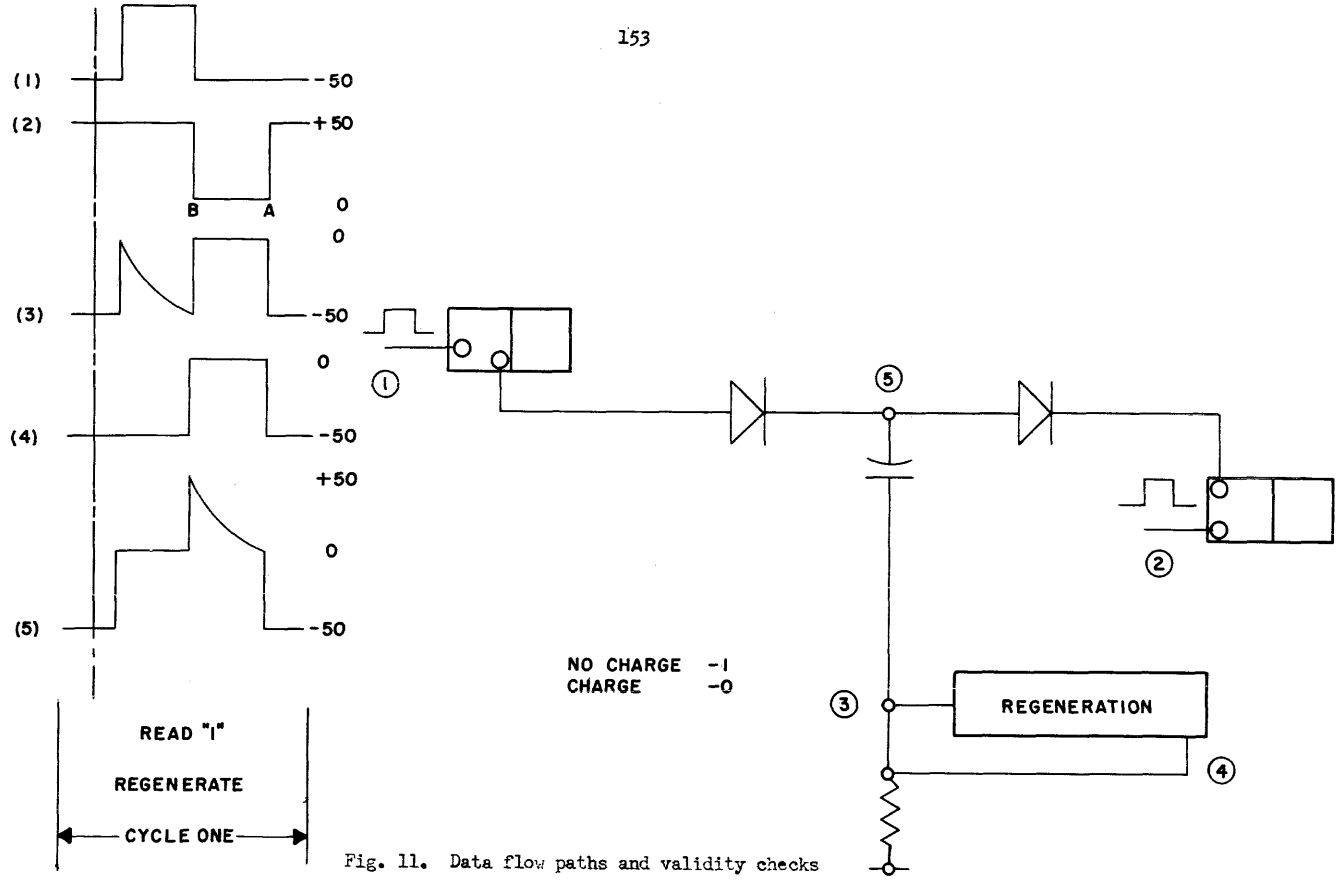


Fig. 11. Data flow paths and validity checks

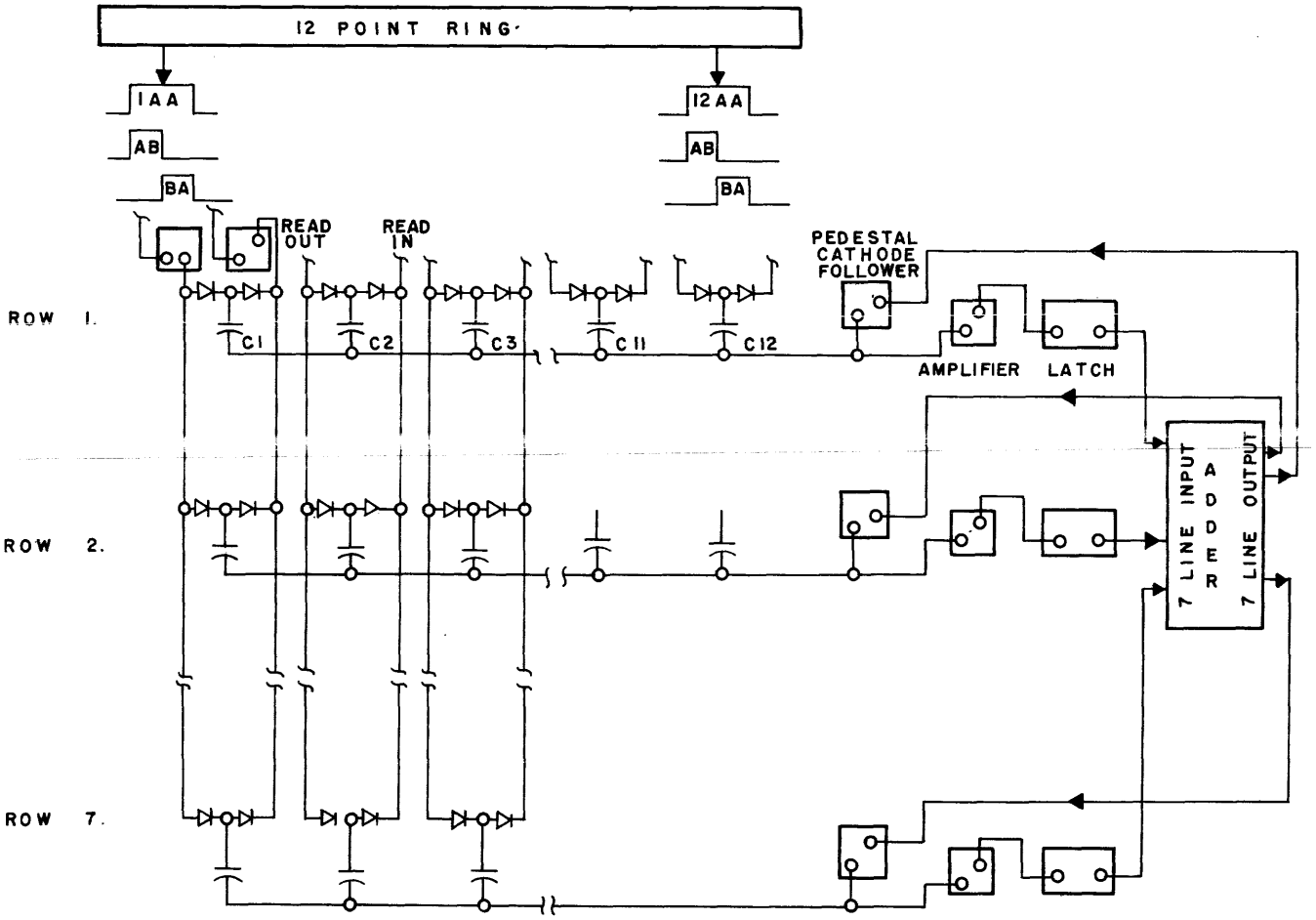


Fig. 12. Capacitor storage, 12 x 7 array

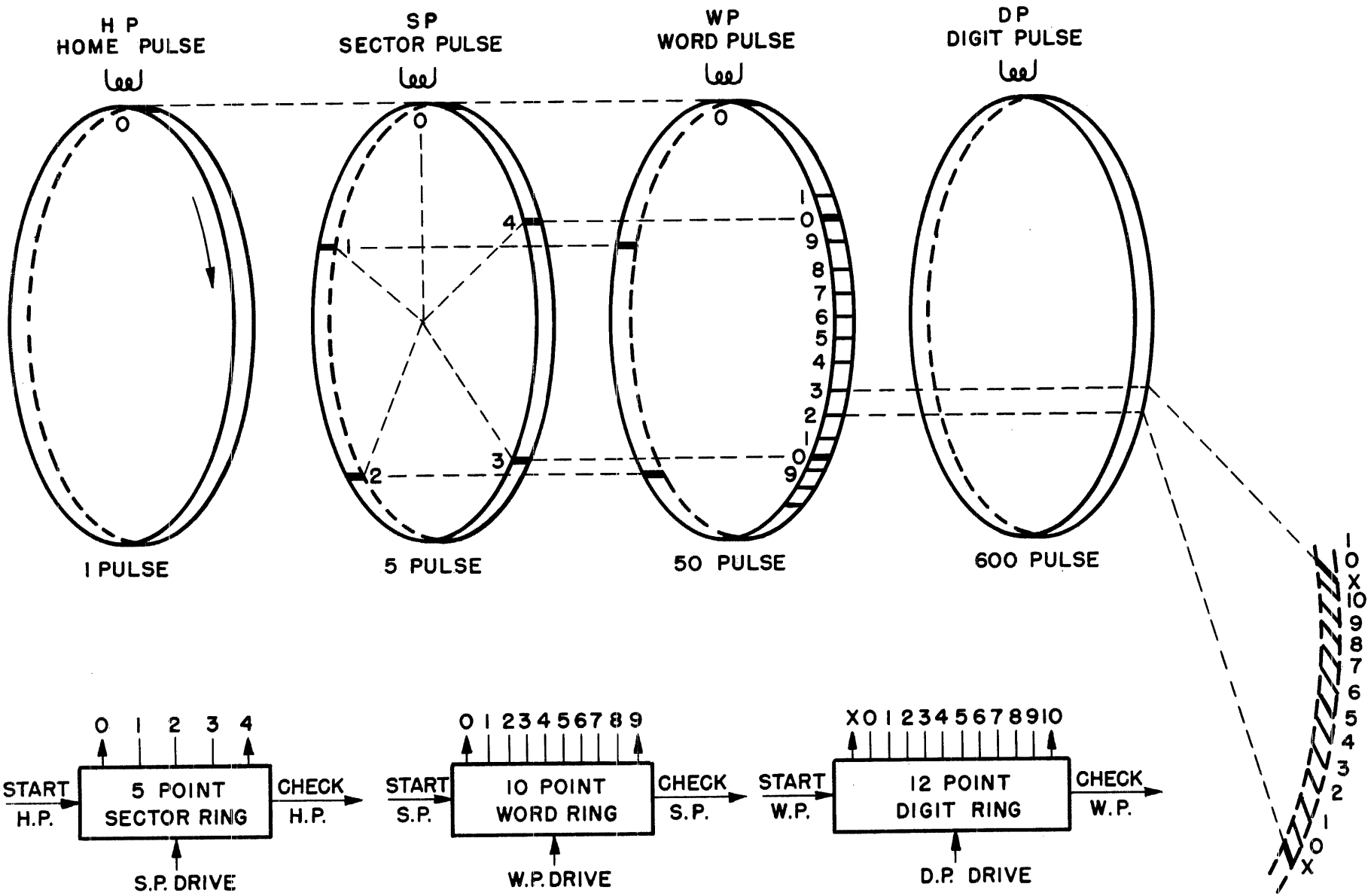


Fig. 13. Recorded timimg pulses