Square-Loop Magnetic Logic Circuits

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Introduction

FERRITES, ferroelectric capacitors, and some ferromagnetic materials all possess bulk characteristics which are usually referred to as square-loop properties. It has been recognized for some time that these properties are particularly compatible with digital-device requirements. This paper attempts to categorize the various methods which are utilized in device synthesis. In addition, it introduces an equivalent circuit model of the devices to determine some of their attributes and limitations. The model is essentially a nonlinear resistive and reactive network whose parameters are determined by the internal state of the device and by its present state of excitation. For the sake of simplicity, the discussion will be limited to magnetic devices. Other authors have pointed out that a direct ferroelectric equivalent exists for multiple-aperture magnetic devices.[1]

Significant Properties of Network Elements

The significant properties of an element of square-loop material are threshold, memory, and saturation. These properties are described more precisely below. Some rather gross assumptions are made; however, a more refined description does not seem warranted because of the increased analytical difficulty. The basic magnetic element, shown in Fig. 1, is a cylinder whose

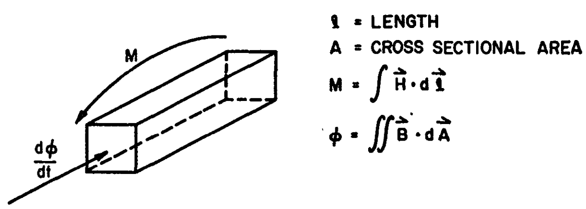

Fig. 1—Elementary magnetic element.

length is considerably larger than either of its other dimensions. The properties of the element are described in terms of the terminal magnetic variables. The cylinder is a two-terminal circuit element. The magnetomotive force M between the two terminals is a function of the flux ϕ passing through any cross section. In this approximation, the magnetic field is assumed to be constant over the length of the element.

Threshold Property

For values of M below a threshold value M_0, the terminal relationship is

$$\frac{d\phi}{dt} = K_1 \frac{dM}{dt}.$$

However if M exceeds M_0, switching may take place. The terminal variable relationship is

$$\frac{d\phi}{dt} = K_1 \frac{dM}{dt} + K_2(M - M_0).$$

The first term represents the reversible flux change and the second term represents the irreversible flux change during switching. The element has a negative threshold as well as a positive one. If M is negative and has a magnitude greater than M_0, switching may also occur, hence

$$\frac{d\phi}{dt} = K_1 \frac{dM}{dt} + K_2(M + M_0).$$

Memory Property

The change in ϕ during switching is the sum of two terms. The first term, proportional to K_1, is a reversible term. It represents the lossless linear flux change caused by an applied magnetomotive force. The second term, proportional to K_2, is an irreversible change. A net change in ϕ proportional to K_2 will occur during switching. The implication is that ϕ has many stable values for zero applied magnetomotive force. The memory of the element is associated with this property. We can define an internal state S, which is related to the flux ϕ, in the element with zero applied field as

$$S = K_0\phi \quad \text{with} \quad M = 0.$$

Choose K_0 so that the magnitude of S never exceeds unity.

Saturation Property

The total irreversible flux change that can take place is limited by saturation. When the material is saturated by a positive drive, the terminal relationship is

$$\frac{d\phi}{dt} = K_1 \frac{dM}{dt}$$

for any applied magnetomotive force greater than $-M_0$. In negative saturation a similar expression is obtained:

$$\frac{d\phi}{dt} = K_1 \frac{dM}{dt}$$

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[1] T. E. Bray and B. Silverman, "Shaping magnetic and dielectric hysteresis loops," *Proc. Special Tech. Conf. on Solid-State Dielectric and Magnetic Devices*, Catholic University of America, Washington. D. C.; April, 1957.

for all M less than $+M_0$. Saturation is related to the irreversible flux changes which have taken place. We have chosen the constant K_0 so that

$$S = +1 \text{ for positive saturation}$$

and

$$S = -1 \text{ for negative saturation.}$$

Now we can summarize the complete set of terminal relationships.

1) We define $S=K_0\,(\phi-K_1M)$, where we have subtracted the reversible flux contribution caused by an applied mmf.

2) $$\frac{d\phi}{dt} = K_1\frac{dM}{dt} \quad \text{for} \quad M < |M_0|,$$

3) $$\frac{d\phi}{dt} = K_1\frac{dM}{dt} \quad \text{for} \begin{bmatrix} S = 1 \\ M > -M_0 \end{bmatrix}$$

4) $$\frac{d\phi}{dt} = K_1\frac{dM}{dt} \quad \text{for} \begin{bmatrix} S = -1 \\ M < M_0 \end{bmatrix},$$

5) $$\frac{d\phi}{dt} = K_1\frac{dM}{dt} + K_2(M - M_0) \quad \text{for} \begin{bmatrix} |S| \neq 1 \\ M > M_0 \end{bmatrix},$$

6) $$\frac{d\phi}{dt} = K_1\frac{dM}{dt} + K_2(M + M_0) \quad \text{for} \begin{bmatrix} |S| \neq 1 \\ M < -M_0 \end{bmatrix}.$$

The constants K_1, K_2, K_0, and M_0 depend on the bulk material and the dimensions of the element. M_0 is usually a function of S, but this fact will be neglected here.

A fourth property implicit in the above relationships is symmetry. If we conduct an experiment starting from state S, applying a drive $M(t)$, we observe the response $\phi(t)$. This experimental result implies that an experiment starting at $-S$, consisting of the application of $-M(t)$, will have the result $-\phi(t)$.

All of the terminal relationships listed are linear differential equations. The magnetic element is nonlinear because the applicable differential equation depends on the applied drive and the internal state. The next section introduces a nonlinear electrical circuit equivalent to the magnetic circuit element.

Equivalent Electrical Circuit

The equivalent electrical circuit will consist of linear electrical components and switches which are actuated at the turning points

$$|S| = 1$$

or

$$|M| = M_0.$$

We choose to relate

$$\frac{d\phi}{dt} \sim i \text{ electrical current,}$$

$$M \sim e \text{ voltage.}$$

The constraints on $d\phi/dt$ and M, imposed when several elements form a magnetic network, are exactly the constraints on i and e in electrical networks. In Fig. 2 we show three two-terminal electrical networks for which the relationship of the terminal variables e, i is identical to the relationship between M and $d\phi/dt$. The equivalent electrical network that should be used is a function of the internal state S and the applied voltage.

A capacitor appears in the equivalent circuit because we are forming the analog of the magnetic variable relationship. This relationship is different from that observed at the electrical terminals of a winding on the magnetic element.

If an electrical circuit, such as a drive winding or an output winding, is coupled to an elementary magnetic element, the relationship between the terminal variables M and $d\phi/dt$ is modified. Fig. 3(a) shows a magnetic element with a coupled electrical circuit which has been reduced to its Norton equivalent circuit. The previously derived circuit is appropriately modified by the addition of a series impedance numerically equal to Y_eN^2 and a series voltage source numerically equal to NI_e. Modification of the magnetic-network-element parameter relationships by means of coupling to electrical circuitry is useful in some synthesis problems.

When two or more magnetic elements are coupled by the same electrical circuit, an extension of the preceding technique is used to obtain an equivalent circuit. This procedure is not always desirable because there is no longer a close relationship between the graph of the derived equivalent circuit and the geometry of the magnetic device. In such cases, it is preferable to solve the network using a mixed (magnetic and electrical) set of independent variables.

Physical Interpretation

It is reasonable to expect that the equivalent circuit parameters can be determined from the dimensions of the element and the properties of the bulk material. From the magnetic material properties, we obtain:

B_s = saturation flux density,
H_0 = threshold magnetic field,
S_w = switching constant,
μ = small signal permeability.

The magnetic element has a length l, and a cross-sectional area A. We solve for the circuit parameters:

$$K_0 = \frac{1}{B_sA}$$

$$K_2 = \frac{2B_sAS_w}{l}$$

$$K_1 = \frac{\mu A}{l}$$

$$M_0 = H_0l.$$

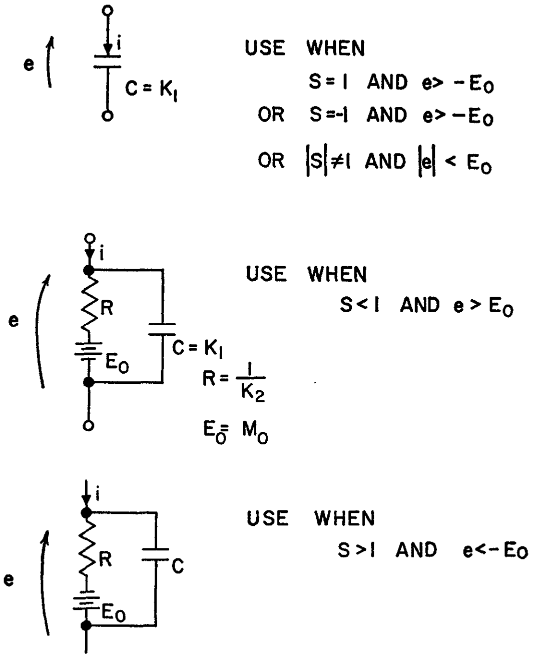

Fig. 2—Equivalent electrical circuits.

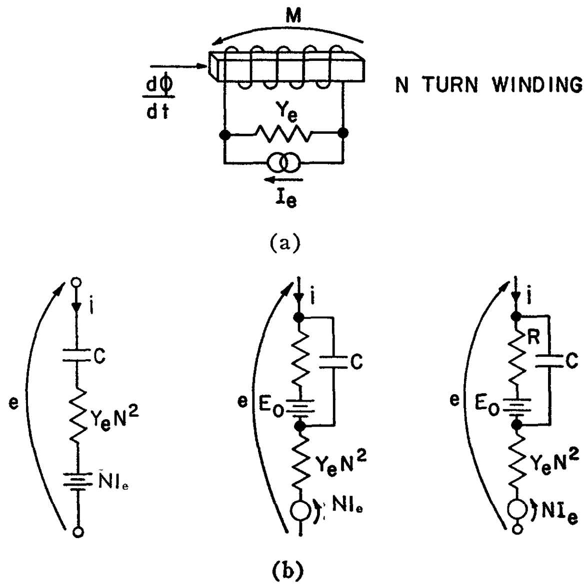

Fig. 3—Modified equivalent circuits for magnetic element coupled to an electrical circuit.

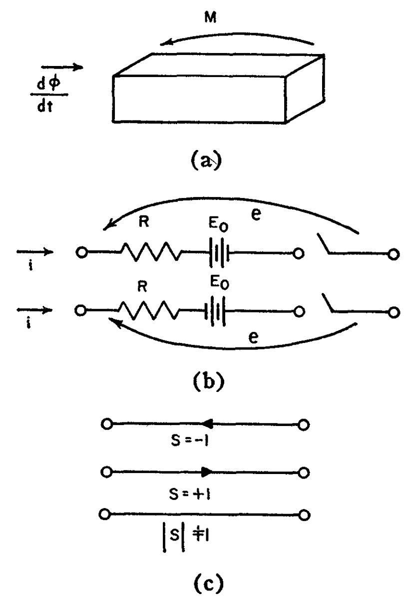

Fig. 4—(a) Elementary unit, (b) simplified equivalent circuits, (c) graphical notation.

In practice, these values are reasonably accurate with the exception of the solution for K_1. K_1 represents the reversible flux-change term and depends quite noticeably on dimensional relationships other than those mentioned, upon the electrical winding configuration and the internal state S. One contributing reason for this effect is that the small signal permeability of the materials used is often less than two orders of magnitude greater than that of air. It has been assumed that the flux entering or leaving the magnetic element through its walls was negligibly small compared to the amount of flux entering or leaving the ends of the element. Careful design is necessary if this assumption is to be a useful one.

Although the reactive nature of the equivalent circuit plays an important part in the analysis of a given device, it does not have the nonlinear property utilized in the digital-device synthesis. For this reason only the nonlinear resistive portion of the equivalent circuit will be used during the discussion of synthesis techniques. As a result, the network will consist of linear resistors, batteries, and switches which provide the nonlinear characteristic. In addition, an internal state of $S = \pm 1$ will be indicated by an arrowhead in the usual way. Elements in other internal states will have no arrowhead notation. Once a network has been synthesized in graph form, it is essential to perform a thorough analysis to fix the optimum geometric ratios and winding configurations. Fig. 4 shows the simplified equivalent circuit and notation.

Logical Function Synthesis

One method of synthesis may be called flux steering. In this type of operation, the device is put into an aggregate internal state dependent on the input binary variables. For each internal state, the output binary function is either equal to unity or equal to zero. When the internal state corresponds to a unity output, the device will respond to a drive D by having a large flux change all along a closed loop L called the output loop. The output function is zero when the response to the drive D is different from that previously described. Either the path along which switching takes place (along which $d\phi/dt$ is large) will differ from L, or there may be no switching at all. Any Boolean function may be written in canonical form as the conjunction of disjunctive polynomials or, alternatively, as the disjunction of conjunctive polynomials. We choose the former representation to show a direct device synthesis. As an example, let

$$g = f(X_1, X_2, X_3, X_4)$$
$$g = (X_1 + X_2)(X_3 + X_4)(X_1 + X_3)$$

where g is a binary function of the four binary-input variables.

A device which will generate to this function is a three-input AND gate as shown graphically in Fig. 5. It is shown initially in its rest state prior to the reception of input drives. The closed path formed by l_1, l_2, l_3, is the output loop L. The control legs l_{c1}, l_{c2}, and l_{c3} may be switched during the input period by drive windings controlled by the input variables X_1, X_2, X_3, X_4 placed on the control legs. Fig. 6 shows the approximate equivalent circuit of the device during an input period in which

$$X_1 = 1$$
$$X_2 = 1$$
$$X_3 = 1$$
$$X_4 = 0.$$

This input signal will cause all three elements forming the output loop L to switch. The device may be designed so that the control legs saturate, or reach $S=-1$, at the same time that the controlled legs l_1, l_2, l_3 reach $S=-1$. A subsequent drive tending to switch the output loop L will switch each element of the output loop. If the input state had been

$$X_1 = 1$$
$$X_2 = 1$$
$$X_3 = 0$$
$$X_4 = 0,$$

then leg l_2 would not have been switched during the input period. Consequently, l_2 would not switch during the output drive. There are a number of variations of this operation which tend to improve its characteristics. The example given, however, sufficiently illustrates the principle of operation of a class of gates called flux-steering gates. We restate this principle for emphasis.

In a flux-steering gate the internal states of a number of elements in an output loop L are controlled by a number of control elements. Switching takes place in every element in L during the output period if, and only if, the output binary function is equal to unity.

It is clear from the discussion that theoretically a single flux-steering gate can generate any combinational logical function.

Gates of this type have been constructed at the General Electric Electronics Laboratory. Reasonable power gain is available. Fig. 7 shows photographs of the output signal of a two-input flux-steering gate for unloaded and loaded operation.

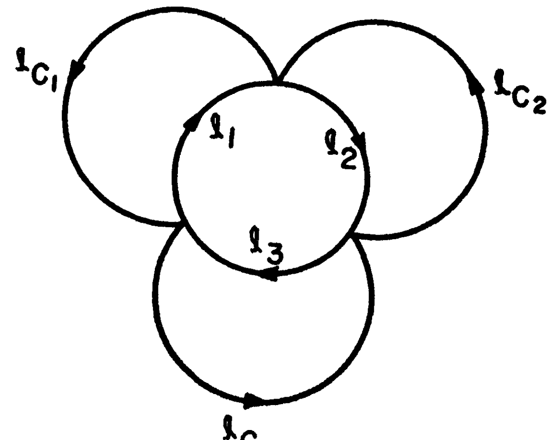

Fig. 5—Graph of three-input AND gate in initial stage.

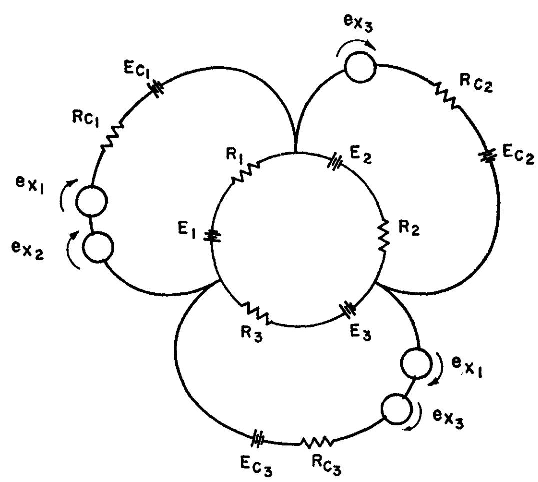

Fig. 6—Equivalent circuit of three-input AND gate during input period.

A second method of synthesis is named flux summation.[2] Again the function is written as the conjunction of a number of disjunctive polynomials. If the Boolean function is the conjunction of n disjunctive polynomials, the device will have n input elements, $n-1$ shunt elements, and one output element. The device has a rest state which precedes any input time period. The geometry is such that switching takes place in the output element only when all the input elements are switched during the input period. As an example, we will synthesize the function

$$g = (X_1 + X_2)(X_3 + X_4)(X_1 + X_3).$$

A graph of the device in its rest state is shown in Fig. 8. Elements l_1, l_2, and l_3 are input elements; elements l_4 and l_5 are shunt elements which may be combined if desired; and element l_6 is the output element. All elements have the same cross-sectional area. During the input period, elements l_1, l_2, and l_3 may be driven and switched. The element l_6 has a high threshold because of its additional

[2] N. F. Lockhart, "Logic by ordered flux changes in multipath ferrite cores," 1958 IRE NATIONAL CONVENTION RECORD, pt. 4, pp. 268–278.

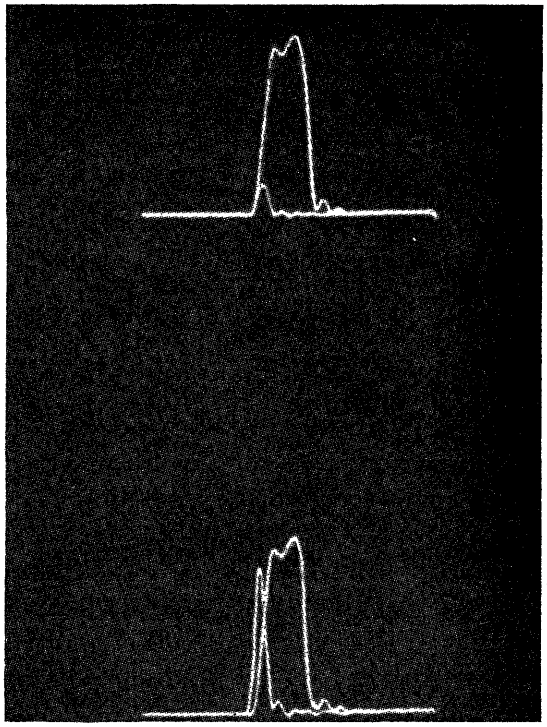

Fig. 7—Flux-steering gate output. Scale: 0.05 v per turn per division (vertical) and 0.2 μsec per division (horizontal). Top: unloaded; bottom: loaded.

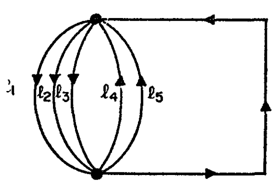

Fig. 8—Graph of flux-summation gate.

length. As a result, if two or less of the input elements are switched, the output element will not switch. The output element will switch only if all three of the input elements are switched. This results from the fact that the two shunt legs will saturate when any two of the input legs switch under the influence of input drives. If all three input elements are switched, the two shunt legs become saturated before the input elements saturate and cannot undergo further large flux changes. Switching in the output element ensues. The threshold M_0 of the output element is made considerably greater than that of the two shunt elements.

It is obvious that the device forms a three-input AND gate as shown. Multiple windings on the control elements perform the disjunction operation. On element 1, two windings are placed; one is excited whenever $X_1=1$, and the other is excited whenever $X_2=1$. The excitation provided by either winding is sufficient to switch element 1. The other control elements are wound in the same way. Various means are available for sensing the output element. The shunt elements may be combined into a single element or may be used to generate other functions of the input variables. This type of gate is only briefly discussed here but is covered thoroughly by Lockhart.[2] A single gate of this type can generate theoretically any combinational logical function. The principle of this gate is restated for emphasis. In a flux-summation gate, switching of an output element is controlled by the presence of shunt elements in parallel with the output element. During the input period, the switching of input elements will cause switching in the shunt elements. Switching will occur in the output element only if the shunt elements saturate before the input elements saturate. Actually this description has been restricted in order to emphasize the principle.

A third type of logical-function synthesis is the relay analog method. It is related to the flux-steering gates but is sufficiently different to warrant separate treatment. The graphs of the relay analog unit in its two possible input states are shown in Fig. 9. The closed loop formed by l_0, l_1, and l_c is capable of storing information in the same way as a magnetic-memory core, by saturation of the three elements in a clockwise or counterclockwise direction. All three elements have the same cross-sectional area, and normally l_c has a higher threshold than either l_1 or l_0. The closed loop is initially saturated in one direction or the other by means of an input variable X. Suppose $X=1$ corresponds to counterclockwise saturation. Now the element is read out by applying one mmf, M, as shown in Fig. 10. As a result of M, a flux change will take place in Z_i (the input lead) and in Z_1 (the unity output lead). Little or no irreversible flux change will take place in Z_0 (the zero-output lead). It is clear that these devices can be cascaded to form a wide variety of functions. A symmetric tree of three input variables is shown in Fig. 11, along with the relay equivalent. The output leads are Z_0, Z_1, Z_2, Z_3 where the subscript refers to the number of input variables equal to unity. Fig. 11 shows the internal state of the device when $X_1=0$, $X_2=1$, $X_3=1$. Theoretically, devices of this type may be cascaded to generate any combinational function.

Relay analog elements have been built at the Electronics Laboratory. The ratio of the irreversible flux changes which take place in the two output paths, Z_1 and Z_0, is about 15:1 for a single stage. Fig. 12 is a photograph of $d\phi/dt$ for the two paths.

We have described three different techniques of synthesizing a gate to generate a combinational logical function. The problems associated with the input and output circuitry have not been considered. There are a number of different types of circuitry which may be used to couple the magnetic gates.[3–7]

[3] A. Wang, "Magnetic delay line storage," Proc. IRE, vol. 39, pp. 401–407; April, 1951.
[4] R. D. Kodis, *et al.*, "Magnetic shift register using one core per bit," 1953 IRE Convention Record, pt. 7, pp. 38–42.
[5] V. Newhouse and N. Prywes, "High-speed shift registers using one core per bit," IRE Trans. on Electronic Computers, vol. EC-5, pp. 114–120; September, 1956.
[6] D. Loev, *et al.*, "Magnetic core circuits for digital data-processing systems," Proc. IRE, vol. 44, pp. 154–162; February, 1956.
[7] M. Karnaugh, "Pulse-switching circuits using magnetic cores," Proc. IRE, vol. 43, pp. 570–584; May, 1955.

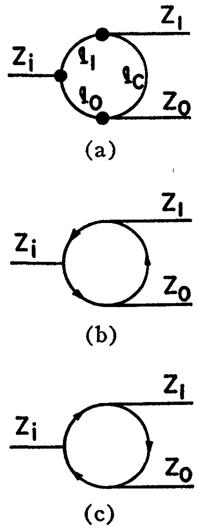

Fig. 9—(a) Relay analog unit, (b) relay analog unit storing a "1," (c) relay analog unit storing a "0".

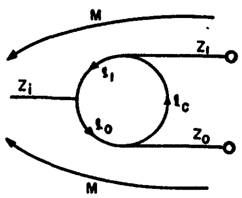

Fig. 10—Output period drives applied to relay analog unit.

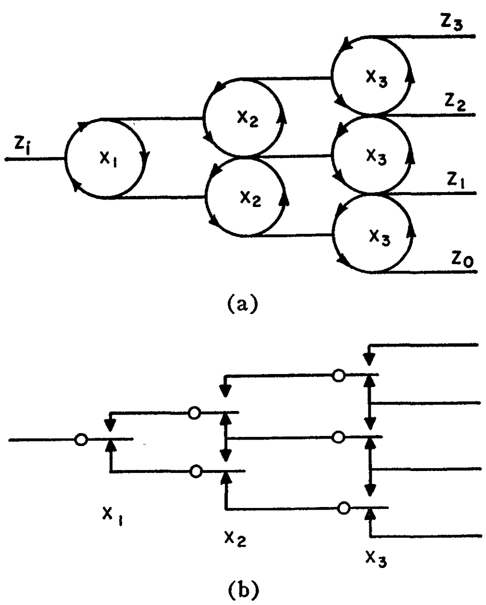

Fig. 11—(a) Relay analog symmetric tree, (b) relay symmetric tree.

In general, all the techniques successfully used in conventional-core logic may be used for multiple-aperture gates. In the next section, we discuss another technique of interconnection fundamentally different from core logic output circuitry and unique to multiple-path logic gates.

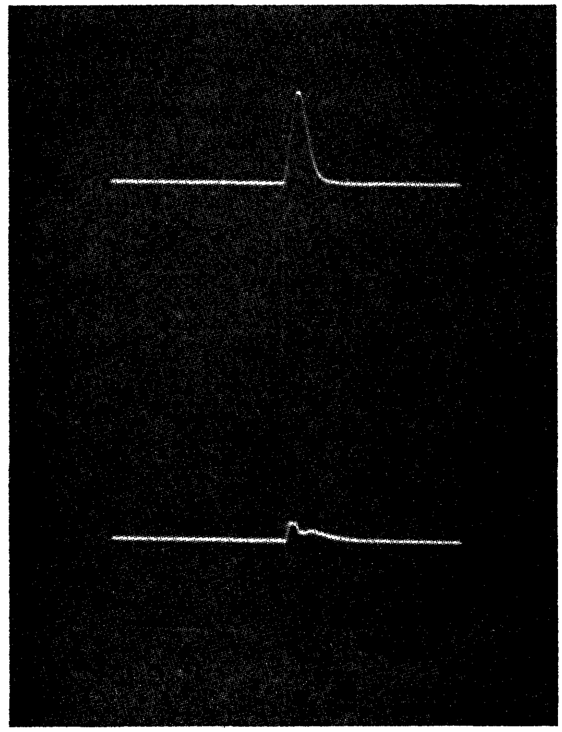

Fig. 12—Signal and noise responses of the relay analog unit. Time scale: 1 μsec/cm.

Magnetic Interconnection

The conventional magnetic-core logic interconnection circuitry is used to force switching of the input leg of one gate when switching occurs in the output leg of another gate. Since both these events are merely flux changes, the possibility of coupling the two entirely within the magnetic medium seems promising. The magnetic-interconnection network should permit unambiguous signal propagation and should not adversely affect the operation of the units which it couples.

Fig. 13(a) shows a graph of a magnetic-network element with properties similar to an electrical diode. The approximate terminal characteristics are given in Fig. 13(b). Leg l_d is saturated as shown. Leg l_r has a much higher threshold than l_d, and a much higher cross-sectional area and saturation flux. The element is shown in its initial state. The diode element will be much more responsive to a positive-applied M than to a negative-applied M. Information can be transmitted from left to right, but not in the reverse direction. If the diode unit is used to transmit information, switching may take place in l_d. As a result, it will no longer have the desired diode characteristic and must be reset. A drive applied to l_r forces l_d back to its original saturation state. These diode units have the required properties for direct interconnection of two magnetic elements. The next paragraph demonstrates their utility by describing a digital-delay unit in which the storage locations are coupled through magnetic diodes. It is important to note that repeated transmission of information in a single direction will lead to saturation of l_r so that l_d cannot be

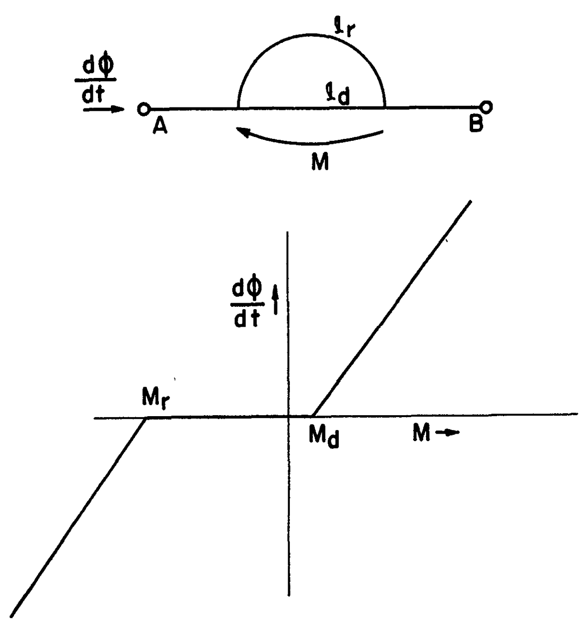

Fig. 13—Magnetic diode terminal characteristics.

reset. In any specific design, techniques can be found to prevent this occurrence. Also, other types of coupling networks can be used in which this problem does not arise. The diode described above is only intended to indicate an approach to the problem.

Digital-Delay Component

Fig. 14 illustrates a section of a digital-delay device which uses magnetic diodes to couple information-storage units. In order to advance the stored "1" to the right, two pulse drives occur in sequence. First, all odd-numbered vertical legs are driven upwards. The diodes prevent information flow to the left. Only the storage location storing a "1" will switch. For the state shown in Fig. 14, l_1, and l_2 will switch. The next pulse resets the diodes. The final state is shown in Fig. 14(c). The stored "1" has moved to the right. The next advance is caused by a pulse drive applied to all the even-numbered vertical legs, followed by a diode reset drive. We have described the digital-delay unit only briefly because we intend to illustrate the possibilities of the synthesis approach rather than to describe a practical device.

The magnetic-diode element may also be used to couple the output leg of a gate to an input leg of another gate. It is possible to construct fairly complicated logical machines in which the information is propagated entirely within the magnetic medium.

All-Core Networks

Networks built entirely of simple cores and copper windings exist which are equivalent to any of the multiple-aperture devices which have been described. A brief introduction to the subject is given here.

When magnetic elements are combined in a network to form a multiple-aperture device, nodal constraints are imposed on the flux levels in the elements. At a node

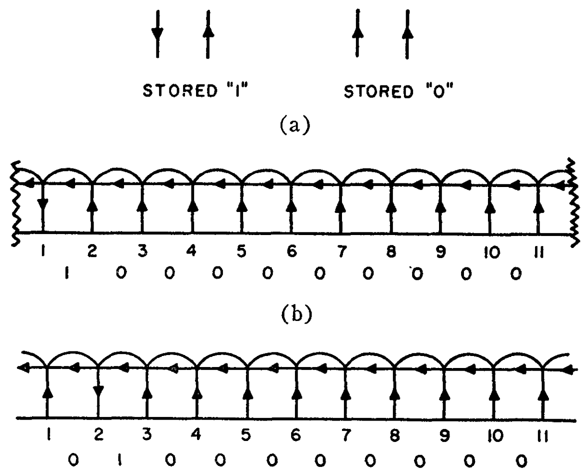

Fig. 14—Digital-delay element.

$$\sum \phi = 0$$

and

$$\sum \frac{d\phi}{dt} = 0.$$

If windings on several different cores are connected in series to form a short-circuited loop.

$$\sum e = 0$$

for the series loop. If there are no other impedances, all the voltages in the loop are induced voltages

$$e = N \frac{d\phi}{dt} \cdot$$

The flux changes which take place in the cores coupled by the series loop obey the following equation

$$\sum N \frac{d\phi}{dt} = 0.$$

This constraint is similar to the nodal constraint of magnetic networks. Following this procedure, a core circuit equivalent to any multiple-aperture device can be found. The relative advantages of the two classes of circuitry will be discussed in a subsequent paper.

Conclusions

We have described an elementary magnetic element. This can be used as a building block for any multiple-aperture device. We have also presented a terminal variable relationship of the element, and introduced a nonlinear electrical equivalent circuit which may be used to analyze the operation of a multiple-aperture device. Three synthesis techniques have been given for obtaining a multiple-aperture device to generate any combinational logical function. Such devices may be coupled by conventional-core logic circuitry.

The possibility of coupling logical gates entirely within the magnetic medium has been discussed briefly.

A simple example of a magnetic "diode" unit was used to demonstrate that square loop materials can be used in interconnection circuitry. If this procedure is followed, many logical operations may be performed on the input formation while the information is kept continuously within the magnetic material.

All-core networks may be derived which are equivalent to the multiple-aperture devices. The networks which result have many advantages over their multihole counterparts. These networks will be discussed in a future publication.

Future Prospects

Coupling of logical gate devices within the magnetic medium has many attractions.

1) Compatibility—the physical input quantities are of the same magnetic nature as the physical outputs. Direct coupling permits scaling down physical dimensions to reduce the power consumption.
2) Resistance to noise—the magnetic elements are natural integrating devices. In a noisy environment they will not respond to large but short-lived noise impulses.
3) Reliability—the reliability of magnetic materials is seldom questioned. The circuits described here contain no electrical components except for a clock pulse source and drive windings.

Future effort should be devoted to developing simple, flexible magnetic-interconnection circuitry suitable for coupling the various types of logical gates.

Relative Merits of General and Special Purpose Computers for Information Retrieval

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Introduction

INCREASING attention to automatic information processing is being given by all sections of our technology, commerce, and military operations. One of its more important aspects is the use of computing machines for storage and subsequent retrieval of information by request.

There have been two simultaneous patterns evolving in the last decade. One group has borrowed the equipment used for standard accounting and engineering calculations and has demonstrated the practicability of automatic information retrieval (IR) using such equipment. A second group has concentrated on designing special equipment for use solely for mechanized information retrieval.

We are at present in a transition period and it seems appropriate at this time to review the progress made using each of the two approaches and perhaps to introduce some constructive cross-fertilization. For the most part, this field, like many new and exciting disciplines, has produced much controversy, strong prejudices, and a tendency to place personal viewpoint above impartial analysis. Let us hope this "feudal" period is over.

Information Retrieval on General Purpose Computers

Excluding military systems, there have been approximately eighteen information retrieval systems programmed and debugged for general purpose (GP) computers. Some of these were written primarily for purposes of exploration and others have been actually made operational. From a review of this activity, we are now able to draw a number of generalizations regarding the performance of general purpose computers in the information retrieval area.

1) The high-speed computer has proven satisfactory for both exploration and operation. Intermediate speed machines have been satisfactory only for exploration, for operation of simple searching schemes or use with small collections.
2) The files of information to be stored were maintained on magnetic tape (one exception employed magnetic disk storage).
3) The full gamut of available machines has been used for information retrieval and it appears that no currently available logical design is markedly superior to any other. Information retrieval systems tend to take many forms. For each IR system formulation and for each machine design, there will be special programming techniques required.
4) A remarkable variety of document storage formats and retrieval schemes has emerged. With the general purpose computers, it appears that the searching system designer is relatively free to build using the classification system best suited to his needs. Indexing schemes as simple as Dewey Decimal and as complex as those required for

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