A Time-Sharing Analog Computer*

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I. Introduction

THE transient behavior of physical systems is often studied by the use of electronic analog computers. If the system considered is characterized by a continuous distribution of properties, the describing system equations are of the partial differential class. An analogous set of equations, soluble on the analog computer, can often be formed by the application of finite difference approximations. For example, a physical system, originally space and time dependent, can sometimes be sectionalized into a number of space segments and then described by a set of ordinary differential and/or algebraic equations. Such sectionalization ordinarily results in a number of equation sets of similar form.

Most often the computational approach to the sectionalized problem is to associate with each section a block of analog equipment. Each section block is usually composed of identical analog computer components. The total system is then simulated by cascading the section blocks. For multisection systems, as are required for rapid transients, equipment requirements increase as n, the number of sections, increases. As a result, some problems cannot be accommodated by the analog computer facility. Further, the large number of potentiometers resulting from the sectionalized cascade solution increases problem setup time and the probability of operator error in the potentiometer-set-phase of setup.

A time-sharing analog solution, described in this paper, replaces the cascade of similar circuits by a single circuit whose components are time-shared. In conjunction with the actual computing elements of the time-shared circuit are circuits to provide time delay and timing functions. This sharing permits a reduction in equipment requirements permitting a smaller investment in computing equipment for a given problem size or increased problem capacity over that available without time-sharing.

II. Description and Method of Operation

A. A Typical Problem and Method of Solution

The description and method of operation of a time-sharing analog computer designed to solve a typical set of pressurized water, forced convection reactor core heat transfer equations follows. The machine to be described illustrates the principal features of time-sharing and the solution of the sectionalized reactor core equations may be considered a typical application.

The set of differential-difference equations to be solved is given below and is shown, along with a sketch of the model, in Fig. 1. Coolant flow is assumed constant for the analysis:[1]

$$\frac{dT_{m_k}(t)}{dt} = \alpha_1 \bar{q}_k(t) - \alpha_2'[T_{m_k}(t) - T_{w_k}(t)] \tag{1}$$

$$\frac{dT_{w_k}(t)}{dt} = \alpha_3'[T_{m_k}(t) - T_{w_k}(t)] - \alpha_4'[T_{o_k}(t) - T_{i_k}(t)] \tag{2}$$

$$T_{w_k}(t) = \frac{T_{o_k}(t) + T_{i_k}(t)}{2} \tag{3}$$

$$T_{o_k}(t) = T_{i_{k+1}}(t). \tag{4}$$

The forcing functions for the kth section are the inlet coolant temperature $T_{i_k}(t)$ and the heat flux $\bar{q}_k(t)$. The output coolant temperature is $T_{o_k}(t)$, and the average metal and coolant temperatures are $T_{m_k}(t)$ and $T_{w_k}(t)$, respectively.

The block diagram of Fig. 2 illustrates the conventional, cascaded method of solution. Each of the n sections is composed of the same computing elements. Fig. 3 indicates, in block diagram, the solution of the equation set by time-sharing. The substitution of a single time-shared circuit for the tandem string of circuits is evident by comparing these two diagrams.

Fig. 4 shows a four-section analog circuit diagram for a time-sharing machine to solve the set under consideration. This analog circuit can be considered as a combination of two circuits, *i.e.*, an equation solving section and an auxiliary or service section. The equation solving section consists of integrators A and B, summer D, and the gain potentiometers with settings α_1, α_2', α_3', α_4'. Integrator A solves (1) for $T_{m_k}(t)$ given the heat flux and the film drop. Eq. (2) is solved by integrator B for $T_{w_k}(t)$ by integrating the film drop and the coolant temperature rise across the kth section. Summer D produces the outlet coolant temperature $T_{o_k}(t)$ by solving (3). The auxiliary or service circuit, peculiar to this time-sharing machine, includes six special devices. The devices and their functions are as follows.

1) Delay circuits D_A, D_B, D_C, and D_D receive, store, and discharge voltages at times determined by control signals. The delay circuits can be classified into two types by considering the nature of the signals upon which they operate. First are those

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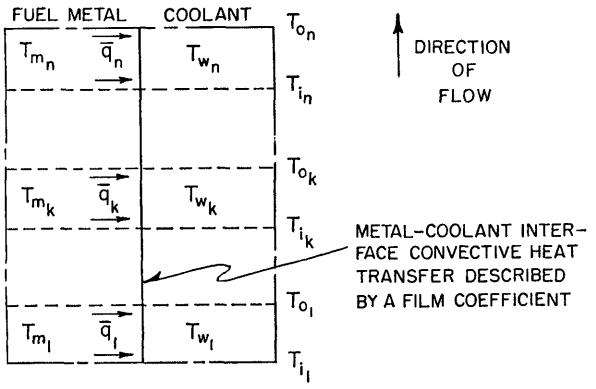
[1] See Appendix for a list of symbols.



$$\frac{dT_{m_k}(t)}{dt} = \alpha_1 \bar{q}_k(t) - \alpha_2'\left[T_{m_k}(t) - T_{w_k}(t)\right]$$

$$\frac{dT_{w_k}(t)}{dt} = \alpha_3'\left[T_{m_k}(t) - T_{w_k}(t)\right] - \alpha_4'\left[T_{o_k}(t) - T_{i_k}(t)\right]$$

$$T_{w_k}(t) = \frac{T_{o_k}(t) + T_{i_k}(t)}{2}$$

$$T_{o_k}(t) = T_{i_{k+1}}(t)$$

Fig. 1—Reactor core heat transfer equations and model sketch.

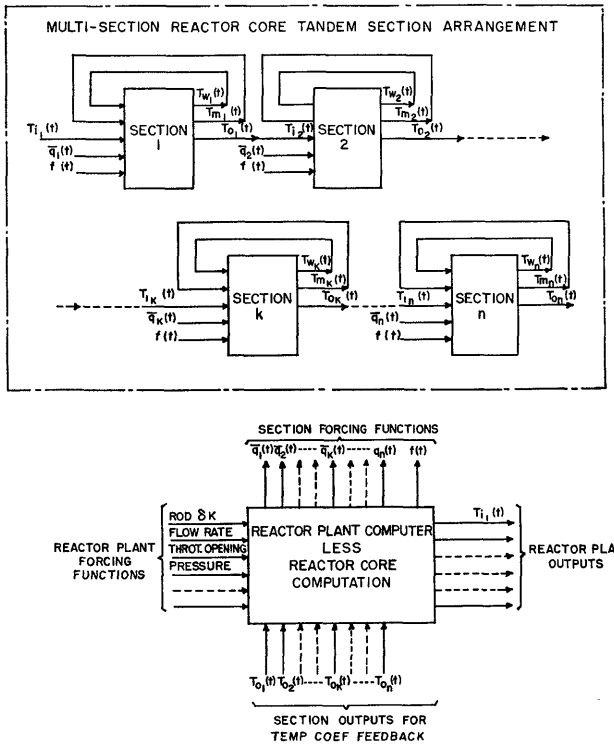


Fig. 2—Reactor plant simulator with multisection reactor core tandem section computer.

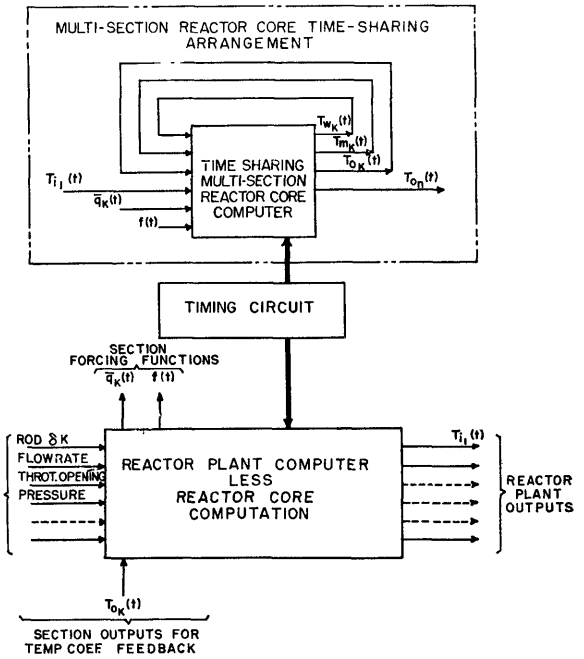


Fig. 3—Reactor plant simulator with multisection reactor core time-sharing computer.

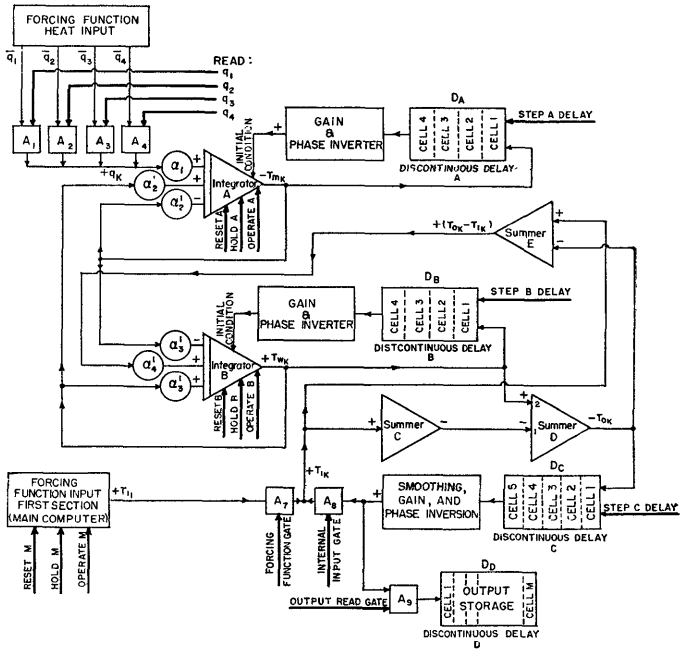


Fig. 4—Time-sharing computer for the solution of a sectionalized heat transfer problem-reactor core.

Circuit model for: open loop, constant flow, non-uniform heat flux situation (four section model).

$$\frac{dT_{mk}}{dt} = a_1\bar{q}_k - a_2'(T_{mk} - T_{wk})$$

$$\frac{dT_{wk}}{dt} = a_3'(T_{mk} - T_{wk}) - a_4'(T_{ok} - T_{ik})$$

$$T_{ok} = 2T_{wk} - T_{ik}$$

$$T_{ok} = T_{ik+1}$$

which delay initial condition voltages, *e.g.*, D_A, D_B. These signals are discrete in nature and the necessary delay may be discontinuous, *i.e.*, discrete sampling, storage, and discharge. Second are those which delay continuous voltages, *e.g.*, D_C, D_D. This second type is extremely difficult to realize economically, particularly when the time delays are long. For this reason all of the delays designed for this prototype computer are of the first type. The continuous signal delays are approximated by smoothing operations performed on the discontinuous delays.

2) The integrator operation control circuit changes the operational state of integrators (Reset, Hold, Operate) in response to command signals from a timing circuit.
3) A heat input circuit provides the kth section heat forcing function when the kth section equations are being determined by the equation solving circuit.
4) Smoothing, gain, and phase inverting circuits perform the functions their names imply.
5) Gates A_1, A_2, A_3, A_4, A_7, A_8, and A_9 control the flow of signals.
6) A timing circuit controls the sequence of operations of the auxiliary devices and the main and time-sharing computer. Command signals from the timing circuit are shown as heavy lines in Fig. 4.

Prior to the initiation of operation of the time-sharing computer, steady-state calculations are performed to obtain the initial conditions for all n sections. These initial conditions are denoted by $T_{m_k}(o)$ and $T_{w_k}(o)$. The voltage analogs of these temperatures are stored in discontinuous delay circuits D_A and D_B, respectively. These circuits consist of four tandem cells denoted by C_1 through C_4. The number of cells making up delays D_A and D_B does not necessarily equal the number of sections being simulated. The requirement is that the number of cells and the stepping rate yield a time delay of $n\tau_R+(n-1)\tau_s$ where n is the number of sections, τ_s the sampling time, and τ_R the reset time. For the subsequent discussion delay D_C is assumed to consist of five cells permitting five samples in each sampling interval τ_s, *i.e.*, $p=5$. The time delay employed is τ_s for the first sample and $\tau_R+(p-2)\tau_s/p$ for the four subsequent samples. If a continuous delay were to be used a delay of $\tau_s+\tau_R$ would be employed.

The heat input forcing function circuit (shown in the upper left of Fig. 4) computes $\bar{q}_1$, $\bar{q}_2$, $\bar{q}_3$, and $\bar{q}_4$, and these variables appear at the inputs of gates A_1 through A_4, respectively. The outputs of these gates are multiplied to form the $\bar{q}_k$ input line.

Two additional engineering considerations remain. A sampling period is chosen to establish the rate of computation as controlled by the timing circuit. The choice of a sampling period is governed by the speed of the transient to be encountered, the degree of reactivity feedback via the temperature coefficient, the desired accuracy, the allowable machine running time, and other considerations. The sampling period is denoted by τ_s. The second consideration is the evaluation of the hot leg transport time τ_{d_h}. This time fixes the number of tandem cells required in delay circuit D_D (output storage, D_D, could also be a continuous type delay, *e.g.*, tape, if economic considerations permit). With τ_{d_h} established, the timing circuits are adjusted to provide such a delay.

The operation of the time-sharing analog computer proceeds as follows. The computer integrators are set to Reset, installing initial conditions $T_{m_1}(o)$ and $T_{w_1}(o)$ at the outputs of integrators A and B. With gates A_1 and A_7 open and all others closed, the main and time-sharing computers are set to Operate condition. The circuit remains in Operate for τ_s seconds during which time the forcing function $T_{i_1}(t)$ flows into the computer. Since gate A_1 is open, the heat flux presented to the circuit is $\bar{q}_1$. The output of summer D is, consequently, the analog behavior of $T_{o_1}(t)$ for the period τ_s, *i.e.*, the output water temperature transient of the first section of the four-section model during the sampling period τ_s. This output temperature transient is to become the input forcing function for section two of the model during the subsequent operational period, and so provision is made to store discrete values of $T_{o_1}(t)$. Such storage is accomplished by stepping the discontinuous delay circuit D_C at intervals during the initial τ_s seconds. Such a stepping action is caused to take place every $\tau_s/4$ seconds by the timing circuit. The result of this action is the storage of five samples of $T_{o_1}(t)$ in delay circuit D_C at the end of τ_s seconds. These five voltage analogs denoted by $T_{o_1}(o)$, $T_{o_1}(1)$, $T_{o_1}(2)$, $T_{o_1}(3)$, and $T_{o_1}(4)$ appear in cells C_5, C_4, C_3, C_2, and C_1 of D_C, respectively. At the end of τ_s seconds the main computer (external to the time-sharing computer) and the time-sharing computer are set to the Hold condition. Shortly thereafter, the initial condition delay circuits D_A and D_B are stepped placing conditions $T_{m_2}(o)$ and $T_{w_2}(o)$ at the outputs of integrators A and B. Stepping delays D_A and D_B also causes the state of integrators A and B (at a time τ_s after the beginning of the transient) to be stored in C_1 of D_A and D_B. These analog voltages are the initial conditions required for the second complete cycle of computation. They displace, in the delay circuits, the "initial" initial conditions. The notation employed for these conditions is $T_{m_k}(4)$ and $T_{w_k}(4)$ where the parenthetical number denotes the state of the variable after a time $4\ \tau_s/4$ seconds. Then, with gates A_2 and A_8 open and all others closed, the time-sharing computer is placed in Reset and shortly thereafter in the Operate condition.

The input forcing function for the second section is

now the output of the first section as previously computed. This signal is introduced by stepping the D_C delay. Such stepping causes the discrete analog voltages to pass out of the delay, through the smoothing, gain, and phase inverting circuit, and into the computational circuit via gate A_8. This same stepping of D_C causes the output transient of the second section to pass into the delay D_C for storage and future use in the next cycle of computation. Again, the output transient is sampled at five points $\tau_s/4$ seconds apart in time. The output transient from the third section is obtained during the third τ_s interval of time by the same sequential process employed in solving the section two response, and similarly for section four.

At the end of the fourth τ_s second interval the contents of delay circuit D_C are five voltages representing samples of the outlet water temperature transient during the initial sampling period of the input water temperature forcing function. At this time, with the time-sharing and main computer in the Hold condition, the initial condition delays D_A and D_B are stepped placing $T_{m_1}(4)$ and $T_{w_1}(4)$ upon integrators A and B. Further, gate A_8 is closed and A_7 opened permitting the second τ_s interval of the inlet coolant temperature forcing function to drive the first section computation when the computers are set to Operate. Gate A_1 is opened and the time-sharing computer is set to Reset. Both computers are now placed in Operate and the second cycle of computation begins. The four section computations proceed as previously described. During the first τ_s seconds of the second complete cycle gate A_9 is open. This open gate permits the output transient from the first cycle to pass into the output storage delay circuit D_D as the first section response to the second sampling interval displaces this information in storage device D_C.

As the computation proceeds in a cyclic fashion the output storage D_D becomes filled with samples of the desired output coolant temperature transient. Each analog sample, spaced $\tau_s/4$ seconds apart in time, is stored in sequential order in the D_D device. The earliest (time-wise) voltage appears in the highest order cell and the latest voltage sample in the lowest order cell, *i.e.*, the input cell number (C_1). As soon as sufficient τ_s second intervals have elapsed so that the sum of the intervals totals the hot leg transport delay τ_{d_h}, the output storage delay begins to discharge the sampled output transient. This output information is sent out in spurts, four section computation times apart. Each data spurt consists of five voltage samples spaced $\tau_s/4$ apart in time. Such discrete data may be smoothed to convert to a continuous analog form.

B. Feedback Considerations

Time-sharing techniques must include provision for feedback signals such as the temperature feedback loop signal in the simulation of a reactor plant with a nonzero temperature coefficient of reactivity. The effect to be simulated can be described as

$$\partial[\delta k_{TC}(t)] = f\left\{\sum_{k=1}^{n} K_{TC_k}[\partial T_{w_k}(t)]\right\}. \tag{5}$$

Or if the temperature coefficient, K_{TC_k}, is assumed spatially constant

$$\partial[\delta k_{TC}(t)] = f[K_T \partial T_{\text{ave}}(t)] \tag{6}$$

where

$$T_{\text{ave}}(t) = \frac{1}{n}\sum_{k=1}^{n} T_{w_k}(t). \tag{7}$$

An exact summation process, as required by (5) or (7), is not possible with time-sharing techniques. This inherent limitation is so because the instantaneous behavior of the average water temperature in all n sections is known only during the computation of the final or nth section, and then only if all previous $T_{w_k}(t)$ transients are stored.

The circuit next described approximates $T_{\text{ave}}(t)$ as given by (7). The method proposed is the repeated correction of the average existing at the start of any one complete cycle by the use of the section data as it becomes available. Listed below are equations which describe such a method.

T_{ave} at the start of a four-section cycle is

$$T_{\text{ave}}(o) = \frac{1}{4}\sum_{k=1}^{4} T_{w_k}(o)$$

during the first section computation

$$T_{\text{ave}}(t) = \frac{1}{4}\sum_{1}^{4} T_{w_k}(o) + \frac{1}{4}[T_{w_1}(t) - T_{w_1}(o)];$$

during the second section

$$T_{\text{ave}}(t) = \frac{1}{4}\sum_{1}^{4} T_{w_k}(o) + \frac{1}{4}[T_{w_1}(4) - T_{w_1}(o)] + \frac{1}{4}[T_{w_2}(t) - T_{w_2}(o)];$$

and the third section

$$T_{\text{ave}} = \frac{1}{4}\sum_{1}^{4} T_{w_k}(o) + \frac{1}{4}[T_{w_1}(4) - T_{w_1}(o)] + \frac{1}{4}[T_{w_2}(4) - T_{w_2}(o)] + \frac{1}{4}[T_{w_3}(t) - T_{w_3}(o)]$$

and finally, during the fourth section computation the average becomes

$$T_{\text{ave}}(t) = \frac{1}{4}\sum_{1}^{4} T_{w_k}(o) + \frac{1}{4}[T_{w_1}(4) - T_{w_1}(o)] + \frac{1}{4}[T_{w_2}(4) - T_{w_2}(o)] + \frac{1}{4}[T_{w_3}(4) - T_{w_3}(o)] + \frac{1}{4}[T_{w_4}(t) - T_{w_4}(o)].$$

At the end of the first complete cycle of computation the T_{ave} signal is

$$T_{\text{ave}}(4) = \frac{1}{4}\sum_{k=1}^{4} T_{w_k}(4)$$

and so, during the next cycle, the identical process can be repeated.

A circuit to accomplish this task is shown in Fig. 5. The expressions, indicated in terms of temperature, are the analogs of the voltages which, of course, actually occur. The state of the circuit is that which would exist at the start of the first section computation of the first cycle.

The operation of the circuit proceeds as follows. Prior to time zero,

$$\frac{1}{4}\sum_{k=1}^{4} T_{w_k}(o)$$

is stored on capacitor C_1. Relay T_{ave} is de-energized and $T_{w_1}(t) = T_{w_1}(o)$ so that the output of summer P is also

$$\frac{1}{4}\sum_{1}^{4} T_{w_k}(o).$$

The analog voltage of this term is applied to capacitor C_2 through the NC_x contact on relay T_{ave}. The inputs of summer Q are $+T_{w_1}(t)$ and $-T_{w_1}(o)$ which are obtained from the output of integrator B and the gain and phase inverter following delay D_B, respectively. Integrator B and delay D_B are shown in Fig. 4. During the first section computation (computers set to Operate) $T_{w_1}(t)$ begins to differ from $T_{w_1}(o)$. This difference is computed by summer Q and added to the original summation stored on C_1 by summer P after being attenuated by $1/n$ by the input potentiometer shown. This new voltage is applied to capacitor C_2.

At the end of the first section computation, relay T_{ave} is energized and maintained up during the second section period. Now capacitor C_2 "remembers" the initial voltage and the new sum consisting of

$$\frac{1}{n}\sum_{1}^{4} T_{w_k}(o) + \frac{1}{4}[T_{w_1}(4) - T_{w_1}(o)] + \frac{1}{4}[T_{w_2}(t) - T_{w_2}(o)]$$

is applied to capacitor C_2 through the NO_x contact. During this period, the inputs to summer Q are $T_{w_2}(t)$ and $T_{w_2}(o)$. Relay T_{ave} is thus alternately de-energized and energized until all four sections have been computed. At the end of four periods capacitor C_2 has the analog of

$$\frac{1}{4}\sum_{k=1}^{4} T_{w_k} \tag{4}$$

stored upon it. Summer R corrects the stored signals for attenuation and dc shift suffered in passing through the cathode-follower read-out circuit. The succeeding cycles proceed as the first.

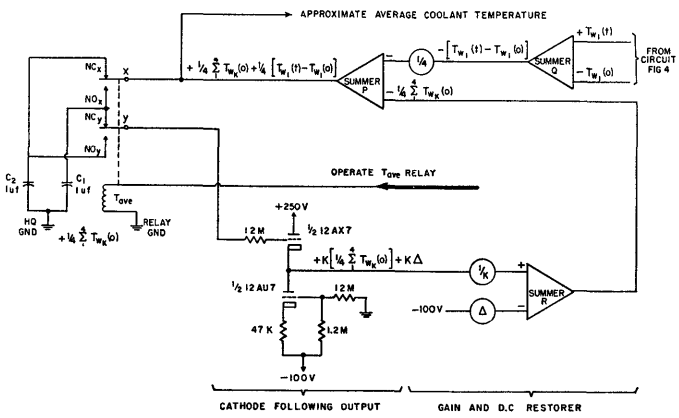


Fig. 5—Summation circuit to approximate the average coolant temperature.

C. Time and Space Dependent Forcing Functions

Provisions for forcing functions which are both time and space dependent require another novel time-sharing circuit. The heat flux input to the reactor core is a typical example.

By finite differencing techniques the kth section heat flux input can be approximated by

$$\bar{q}_k(t) = m_k \bar{q}_T(t),$$

where m_k is constant. Several system variables cause time variations in the reactor core—heat flux, $[\bar{q}_T(t)]$, *e.g.*, changes in rod position, coolant temperature, and pressure. If the sampling period of the time-sharing computer is chosen so that the core heat flux, $\bar{q}_T(t)$, changes appreciably during the period, provision must be made to include such variations in the computation.

Fig. 6 is a circuit diagram of a heat flux circuit which provides both a space and time variant forcing function. During the first sampling period relay Q is inoperative permitting the $\bar{q}_T(t)$ signal to flow to the input bus of the m_k scaling potentiometers and to the input of discontinuous delay D_Q (this delay could also be of the continuous type, *e.g.*, magnetic tape). While the $\bar{q}_T$ signal flows, the D_Q delay is stepped causing five (arbitrary number) samples to be stored within the delay. Potentiometer m_1 scales $\bar{q}_T(t)$ yielding $\bar{q}_1(t)$. During this time, rotary switch R_Q is in position 1. Thus, $\bar{q}_1(t)$ appears at the output of the heat flux circuit. At the start of the second section computation relay Q is operated and switch R_Q is stepped to position 2 by pulsing the step R_Q lead. During the second interval delay D_Q is stepped periodically causing the initial $\bar{q}_Q(t)$ signal to reappear on the potentiometer input bus as well as at the input of the delay. Smoothing and gain are applied to the discontinuous signal as indicated. During this period $\bar{q}_2(t)$ appears as the output of the flux circuit. This sequence is continued until all n sections have been computed. At the completion of the computational cycle rotary switch R_Q is set to position 1 by pulsing the home R_Q lead which actuates the release magnet. Relay Q is released and the circuit is ready for the second sampling period. This cir-

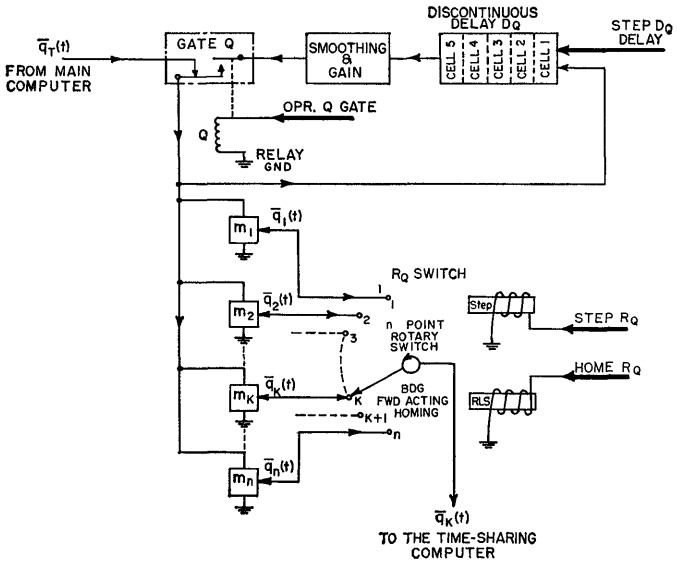


Fig. 6—Heat flux forcing function circuit for a time-sharing computer solving the reactor core equations.

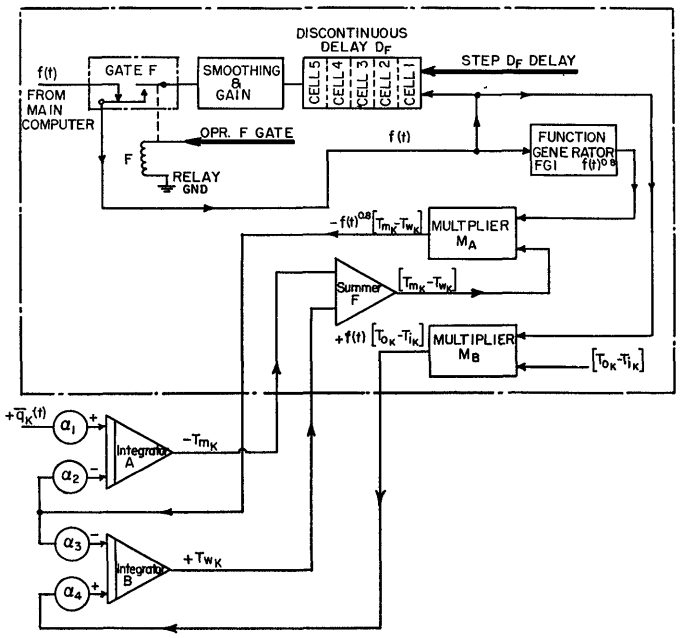


Fig. 7—Time variant flow rate forcing function circuit for a time-sharing computer solving the reactor core equations.

cuit performs the functions of gates A_1 through A_4 of Fig. 4.

D. Time Dependent Forcing Functions

Another class of forcing functions which must be handled by time-sharing are those which are time dependent only. An example of this class is the coolant flow rate through the reactor core. For nonconstant flow (1) and (2) are amended to read:

$$\frac{dT_{m_k}(t)}{dt} = \alpha_1 \bar{q}_k(t) - \alpha_2 f(t)^{0.8}[T_{m_k}(t) - T_{w_k}(t)], \quad (8)$$

$$\frac{dT_{w_k}(t)}{dt} = \alpha_3 f(t)^{0.8}[T_{m_k}(t) - T_{w_k}(t)] - \alpha_4 f(t)[T_{0_k}(t) - T_{i_k}(t)]. \quad (9)$$

Clearly those terms in (8) and (9) with coefficients α_2, α_3, and α_4 are dependent upon flow rate. Fig. 7 is a circuit designed to include the effects of variable flow upon the reactor core analog simulation. The circuit is shown as it would appear when augmenting the time-sharing simulator illustrated in Fig. 4. Only integrators A and B of Fig. 4 are indicated and all other components are omitted for simplicity. The variable flow portion is set off by the heavy broken line in Fig. 7. At the start of the transient run relay F is de-energized allowing the flow signal $f(t)$ to pass into the computer as a continuous function. During the initial sampling period, delay D_F is stepped causing discrete samples of $f(t)$ to be stored in the delay (D_F could be a continuous delay, *e.g.*, tape). The sample $f(t)$ also passes to multiplier M_B, and the function generator FG1 and hence to multiplier M_A. The outputs of these multipliers, M_A and M_B, are the desired functions

$$f(t)^{0.8}[T_{m_k}(t) - T_{w_k}(t)]$$

and

$$f(t)[T_{o_k}(t) - T_{i_k}(t)],$$

respectively. At the end of the section 1 computational period, relay F is energized by applying voltage to the Operate F gate lead. During the section 2 and succeeding section computation periods the discontinuous delay D_F is stepped periodically causing the initial $f(t)$ sample to pass out of the delay, through the smoothing and gain circuit, and into the computing circuit. Thus, the sample is reused in each section period. At the conclusion of the complete n-section computing cycle, relay F is de-energized and the circuit is prepared to receive the second $f(t)$ sample from the main computer.

III. Pilot Model

In order to determine the workability and accuracy of the time-sharing computing method a pilot model was designed and constructed with sufficient capacity to solve a four-section reactor core heat transfer problem with constant coolant flow and uniform axial heat flux.

The necessary delay circuits for the pilot model were designed by an extension of an invention attributed to Janssen[2] and later demonstrated by Philbrick.[3] A block diagram of a delay circuit is shown in Fig. 8. Buffer amplifiers B_1, B_2, etc., have the following properties:

1) very high input impedance,
2) very low output impedance,
3) amplification close to unity, and
4) high available output power.

[2] J. M. L. Janssen, "Discontinuous low-frequency delay line with continuously variable delay," *Nature*, vol. 169, p. 148; January, 1952.
[3] "A Palimpset on the Electronic Analog Art," ed. by H. M. Paynter, G. A. Philbrick Researches, Inc., Boston, Mass., p. 163; 1955.

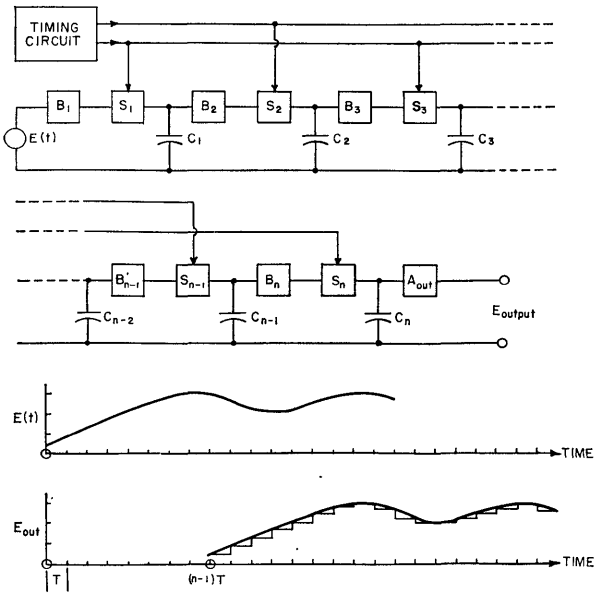


Fig. 8—Block diagram of a discontinuous delay line with continuous variable delay (after J. M. L. Janssen, Royal Dutch/Shell Laboratory, Delft, Netherlands, October 25, 1951).

These devices were obtained by the design of an extra-linear cathode follower. Switches S_1, S_2, etc. have characteristics as follows:

1) very low forward impedance,
2) very high reverse impedance, and
3) controllable by external command signals.

The switches for the delay circuits of the pilot model were designed for two different applications of the delays:

1) The short time delay circuits, *e.g.*, the recycled forcing function delays (delay D_C of Fig. 4), required bilateral electronic switches patterned after the work of Philbrick.[3]
2) The long time delay circuits, *e.g.*, the initial condition delays (D_A and D_B of Fig. 4), were designed with fast-acting relay contact switches.

Capacitors C_1, C_2, etc., are extremely low-leakage components. Output amplifier, A_{out}, has:

1) adjustable gain,
2) very high input impedance, and
3) low output impedance.

This component was obtained by cascading a buffer amplifier and a conventional analog computer dc amplifier. This arrangement permitted the required smoothing operation and the gain adjustment to be performed within the output device.

To begin the explanation of the delay circuit it is assumed that all switches are open and all capacitors initially uncharged. At time zero all odd number switches are closed for a sufficient time to cause capacitor C_1 to charge to $E(o)$. At time T all even number switches operate causing C_2 to assume voltage $E(o)$. The odd switches are then closed at time $2T$ allowing $E(2T)$ to charge C_1 and $E(o)$ to pass to C_3. At time $3T$ even switches are closed moving $E(2T)$ to C_2 and $E(o)$ to C_4. The process of alternately closing the odd and even number switches is continued with closures every T seconds. Eventually, after $(n-1)T$ seconds, voltage $E(o)$ appears on C_n and hence becomes the first output sample. Following this voltage, every $2T$ seconds, are $E(2T)$, $E(4T)$, $E(6T)$, etc. Thus a delay of $(n-1)T$ is achieved. Since T, the switching period, can be controlled, the objective is achieved.

The timing circuit of the pilot model was synchronized with a master clock. Clock pulses were used to drive bistable multivibrators which performed desired frequency divisions. The resulting subharmonics of the clock pulse train were directed to a logic circuit which generated the necessary control pulses to execute the desired sequential switching plan. The control pulses, after receiving power amplification, actuated relays whose contacts formed a switching network. The signals from the network controlled the operation of the component devices which made up the time-sharing computer.

IV. Test Results and Conclusions

In order to evaluate the performance and accuracy of the pilot model a series of tests were run in which the reactor core heat transfer equations were simulated with zero heat input and constant flow, *i.e.*, a simple transport delay problem described by:

$$\frac{dT_{w_k}}{dt} = \frac{2n}{\tau_{do}} T_{i_k} - \frac{2n}{\tau_{do}} T_{w_k}, \tag{10}$$

$$T_{o_k} = 2T_{w_k} - T_{i_k}, \tag{11}$$

$$T_{i_k} = T_{o_{k-1}}. \tag{12}$$

The forcing function was a cosine shaped increase in the inlet coolant temperature. The results of these experiments indicated:

1) Conventional and time-sharing circuits are compatible and reproducible results are obtainable. Switching transients, relay contact "races," and switching synchronism problems are evident but they can be overcome by proper circuit engineering.
2) Simulation accuracy is a function of the sampling interval employed in the delay circuits and the method of signal smoothing employed. Fig. 9 shows a typical input-output trace. The circuit was forced by a 0.785 rad/second cosine rise in inlet coolant temperature. Delay D_C of Fig. 4 was smoothed by a $1/(\tau_c s+1)$ filter in which the optimum τ_c was found to be 0.03 second. The maximum per cent departure from the ideal delayed transient (also shown in Fig. 9) is 3.1 per cent occurring 3.6 seconds from the start of the transient.
3) The accuracy of the simulation of systems in which feedback signals dependent upon instan-

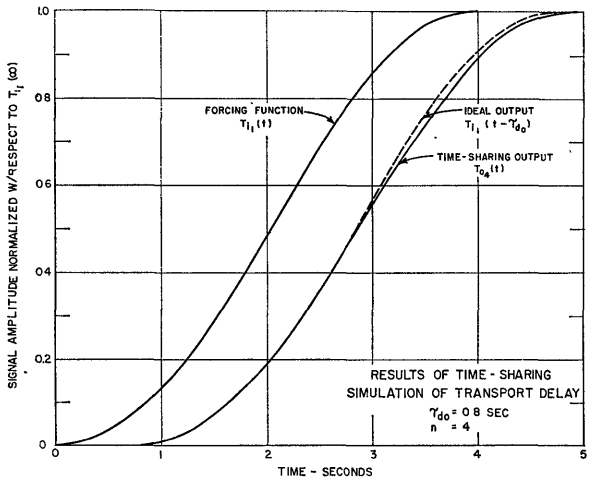


Fig. 9—Results of a time-sharing simulation of transport delay.

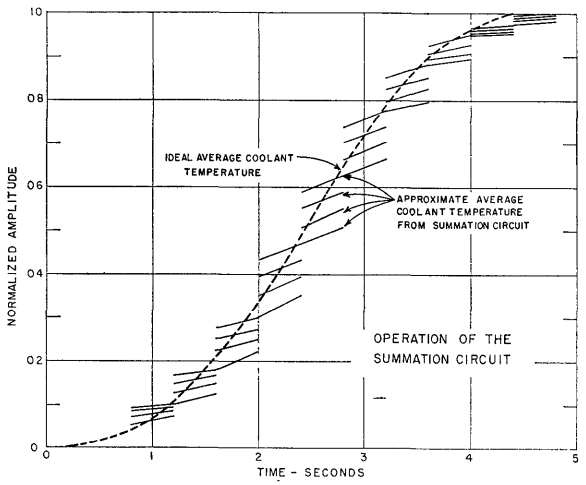


Fig. 10—Operation of the summation circuit.

taneous spatial averages, is limited by the inherent inability of the time-sharing computer to correctly obtain such averages. The operation of the circuits designed to obtain the approximate average coolant temperature was, however, successful. Fig. 10 illustrates the results of approximating the spatial average by employing the circuitry previously described. In this figure each τ_s segment of the input forcing function produces four output traces since the average water temperature is continuously corrected as new data become available from the four sections in turn. The nature of the approximation is seen by comparing the summation circuit output traces, shown as solid lines in Fig. 10, with the ideal average temperature shown as a dashed line.

V. Cost and Equipment Requirements

In order to compare the approximate cost and equipment requirements of time-sharing computation with conventional analog computation a calculation of these requirements for a large but typical problem was performed. The problem considered was the simulation of the heat transfer phenomena of a reactor core coupled to a heat exchanger within a pressurized, forced convection system. The simulator was designed with sufficient capacity to provide the following:

1) variable coolant flow,
2) nonuniform axial heat flux,
3) temperature coefficient of reactivity feedback,
4) variable steam throttle opening, and
5) steam temperature feedback in the heat exchanger.

The most important results of the calculation are shown in the three graphs of Fig. 11. Fig. 11 (a) compares the cost of time-sharing solutions to conventional cascade solutions as a function of the number of sections.

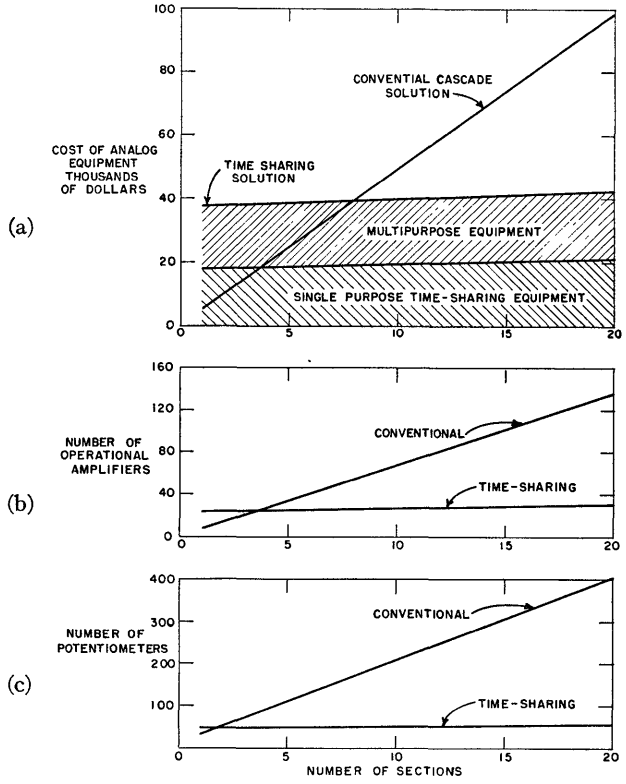


Fig. 11—Cost and equipment comparisons.

Time-sharing costs are divided into two parts. The first, shown cross-hatched in Fig. 11(a), represents the cost of that equipment which is peculiar to time-sharing and which could not readily be used in non-time-shared applications. The second component cost is that of multipurpose equipment, *e.g.*, amplifiers, potentiometers, multipliers, etc., which, of course, could be used for non-time-shared problems. Fig. 11(b) and 11(c) shows the amplifier and potentiometer requirements as a function of the number of sections simulated.

The ratio of the machine running time required to

solve a sectionalized problem by time-sharing to the running time by the conventional cascade method is given by:

$$\frac{\text{time-sharing running time}}{\text{conventional running time}} = n\,\frac{(\tau_s + \tau_R)}{\tau_s}\,.$$

VI. Conclusions

The results of this study indicate that a time-sharing analog computer for the solution of differential-difference equations is realizable and is economically attractive in certain circumstances. If the number and size of multisection problems to be computed are large, the equipment conservation possible with time-sharing can conceivably outweigh the accuracy and running time penalties.

The three phases of this study, *viz.*, design, development, and optimization, yielded more specific conclusions. The design of a system to solve the reactor core and boiler heat transfer multisection equations revealed that considerable savings in operational amplifiers and potentiometers would be enjoyed when the number of sections simulated exceeded three. First cost of the auxiliary equipment required for the time-sharing solution of these equations is estimated to be equivalent to the first cost of a sufficient amount of conventional analog equipment to solve a four-section problem. Programming and set-up time would be markedly reduced by time-sharing particularly if a large number of physical parameters and analog scaling factors were common to many sections. Such a savings would tend to offset the increase in running time required by time-sharing. Design considerations further revealed the upper bound on the accuracy obtainable under time-sharing to be the accuracy achieved by the conventional cascade analog solution. This accuracy can be approached as

1) the sampling interval, τ_s, approaches zero,
2) the number of samples, p, obtained for the forcing function delays approaches infinity, and
3) the highest frequency components of the input forcing functions approach zero.

The development phase of this study produced working models of all of the circuits essential to the time-sharing system. These units were successfully integrated with conventional analog computing equipment and test problems were run. The electronic and relay circuits proved reliable and the total system yielded reproducible results. The delay and timing circuit designs, as conceived for the four-section pilot model, can be readily extended to handle additional sections.

Much additional attention can be given to the optimization of the time-sharing system. The effect of the variation in computing parameters, *e.g.*, τ_s, upon accuracy might profitably be studied. Newly available analog devices, such as magnetic tape loop transport delays, could provide improvements in computational accuracy and thus merit investigation.

Appendix

List of Symbols

Symbol	*Description*	*Units*
α_1	Constant in heat transfer equations	ft² °F/Btu
α_2', α_3', α_4'	Constant in heat transfer equations	1/sec
σk_{TC}	Reactivity due to temperature effects	reactivity
K_T	Over-all temperature coefficient of reactivity	reactivity/°F
K_{TC_k}	Temperature coefficient of reactivity for the kth section	reactivity/°F
$f(t)$	Ratio of instantaneous coolant flow rate to the time-zero flow rate	dimensionless
m_k	Ratio of kth section average heat flux to the total average heat flux	dimensionless
n	Number of axial sections	dimensionless
p	Number of samples obtained for delays during τ_s interval	dimensionless
$\bar{q}_k$	Spatially averaged heat flux in the kth section	Btu/second ft²
$\bar{q}_T$	Spatially averaged total heat flux	Btu/second ft²
t	Time	second
T	Switching period of discontinuous delay	second
τ_c	Smoothing circuit time constant	second
τ_{do}	Coolant transport time through reactor core coolant channel	second
τ_{dh}	Hot leg transport time, core to heat exchanger	second
τ_R	Time-sharing reset time	second
τ_s	Time-sharing sampling time	second
T_{ave}	Spatially averaged mean coolant temperature	°F
T_{i_k}	Mean coolant temperature at entrance to the kth section	°F
T_{m_k}	Spatially averaged metal temperature in kth section	°F
T_{o_k}	Mean coolant temperature at exit of the kth section	°F
T_{w_k}	Spatially averaged mean coolant temperature in kth section	°F