# ANALOG TIME DELAY SYSTEM

Charles D. Hofmann
Electronics Engineer
and
Harold L. Pike
Senior Electronics Engineer

Convair (Astronautics) Division
General Dynamics Corporation
San Diego, California

## Introduction

The Convair-Astronautics Time Delay System is being developed to make possible the delay of analog functions over a greater range than is possible with more conventional means. The system is designed to handle ten channels of analog data, delay each for the same time interval, and reproduce the functions within 0.1% of the original composition for all frequencies up to 100 cycles per second. The delay is required to be variable from 0.01 to 10 seconds, ±5 milliseconds. This paper is concerned with the system design and will not attempt to discuss applications.

In order to obtain the wide delay range required, a special magnetic tape system is employed. The delay is achieved by recording information on the tape with a recording head, and reading the information back at the prescribed time with a separate head. The tape travels at a uniform rate in a continuous loop. The delay is therefore directly related to the length of tape between the write and read heads. This is controlled by a servo system which continuously monitors this "delay" loop and compares it with a value preset directly in milliseconds. The high degree of accuracy is obtained by converting the analog input voltages to digital form and recording it. A single analog-to digital converter is used for this purpose with the various analog inputs being commutated to the converter. The read head retrieves the digital information from the tape after the desired delay. The information is then re-commutated to ten digital-to-analog converters. The use of separate digital-to-analog converters for each input-output channel eliminates the need for holding amplifiers and commutation of the analog output voltages. Correlation between input and output commutation and delay control is achieved through a central timing system. The overall flow of information is shown in Figure 1.

## Tape Transport

The tape transport is designed to use a 100 foot continuous loop, one inch magnetic tape. Information is recorded non-return to zero on the tape by a 14 channel recording head designed to handle a forty kilocycle repetition rate as the tape moves at 100 inches per second. At the prescribed time later, this information is retrieved by the read head as the tape continues in its loop path. Since a delay of from 0.01 to 10 seconds is required, the amount of tape between the recording and the reading heads must be variable from one to one thousand inches. This tape is loosely piled in the tape delay storage compartment. The tape is pushed over the recording head where air pressure assures contact with the head. This is necessary since, to achieve the minimum one inch loop, it is impractical to place the drive capstan between the recording and reading heads. If the delay loop exceeds four inches, the tape is picked up below the recording head by a vacuum capstan which helps maintain tension in the tape across the recording head. With a delay loop of less than four inches, the tape pulls free of the vacuum capstan and its own centrifugal force supplies the required tension. The tape, after passing the read head, moves through a compartment similiar to the delay storage compartment where all tape not used in the delay loop is stored. Vacuum is used to maintain tension in the tape wherever it is necessary. The principle features of the tape unit are shown in Figure 2.

## Timing

As shown in Figure 3, the heart of the timing system is a 960 kc crystal clock which generates the fundamental frequency used by the digitizer for bit selection. This frequency is divided by twelve to obtain an 80 kc rate used by the delay servo counter. Dividing again by two gives the fundamental 40 kc sampling rate. A ten bit shift register uses this rate for input and output commutation and channel identification.

## Delay Servo

The tape transport uses two three-phase synchronous motors, one to drive the write and vacuum capstans and the other to drive the read capstan. The first motor is driven directly from the 60 cycle three phase line while the read motor is driven by a variable frequency (three-phase) oscillator. The frequency of this oscillator is controlled by a voltage level corresponding to the output of a comparator. The recording head records the 40 kc clock on the tape and, at the same time, adds it into a counter. The read head subtracts this 40 kc signal out of the same counter so that the balance in the counter represents the difference between the counts recorded and the counts read. This balance is proportional to the delay in the system and and is continuously compared against a preset count representing the delay required, set directly in milliseconds. The output of the comparator then regulates the speed of the read motor as discussed. This system is shown in Figure 4.

## Analog-To-Digital Conversion

The analog-to-digital converter samples the input analog voltage and converts it to digital form using ten bits for amplitude representation plus one bit to indicate polarity (sign). To obtain the required accuracy, each channel of input information is sampled at a repetition rate of four thousand samples per second. Since a single digitizer is used for all ten channels of analog inputs, the overall sampling rate of the digitizer is forty thousand samples per second. A ten bit shift register driven by the forty kilocycle clock is used to activate diode bridge switches for sequential input commutation. The digitizer consists of eleven flip-flop operated bit switches which contribute current through calibrated resistors to a summing junction to which the input signal is also connected. The polarity of this summing junction is the normal carrier signal input to a "ring modulator". The signal input of the "ring modulator" is the 960 kc clock frequency. The output is a 960 kc signal which leads or lags the clock by 90 degrees depending on the polarity of the summing junction. By comparing the phase of the clock with the modulator output, the summing junction's polarity is determined.

The common "ripple-down" method of digitizing is used. Starting with the most significant bit, the bit switches are turned on sequentially by an eleven bit shift register driven by the 960 kilocycle clock. Each bit switch activates a zener diode regulated, negative voltage source which is summed through a calibrated resister to the summing junction. The current contributed by each bit is proportional to the significance of the bit. If the summing junction goes negative, the bit reset gates are activated so that when the next bit switch is turned on, the preceeding switch is turned off. In the event the input analog voltage is negative, the sign bit is activated which contributes a positive current to the summing junction of a magnitude equal to that contributed by a maximum input voltage. The effect of the negative input voltage and the sign bit is a current equal to a positive input which is the complement of the absolute value of the input signal. As a result, the digitizer will always handle a positive input voltage. When all ten bits have been sampled a "transfer" pulse is generated by the eleventh bit of the shift register. This pulse is "and" gated with each bit switch through eleven transfer gates so that each transfer gate corresponding to each "on" bit switch will pass the pulse. The output of each transfer gate is coupled to a symmetrically driven flip-flop which serves as a write head driver amplifier. The eleven channels of digital information are thus recorded in parallel on eleven of the fourteen channels of the tape. A change in direction of saturation of the tape corresponds to a "one" being recorded, while no change represents a "zero". Figure 5 is a block diagram of this system. Figure 6 is a time versus sequential operation chart of the system.

## Digital-To-Analog Conversion

This section, shown in Figure 7, includes fourteen read amplifiers, eleven of which receive the digital information from the tape; ten groups of eleven output commutation gates; a ten bit shift register; and ten digital-to-analog converters each consisting of eleven bit switches, gates, and a summing amplifier with a low pass filter. The outputs from

the eleven read amplifiers (pulse for a "one", no pulse for a "zero") are gated to the proper output switches by the 10 bit shift register. This shift register is started in the output channel No. 1 position by a pulse from the tape which indicates that input channel No. 1 is being read, and is then advanced by the recorded forty kilocycle clock as the other input channels are read. The output bit switches are flip-flops which control diode bridge output gates. These gates apply a standard reference voltage through a calibrated resistance to the summing junction of the output amplifier. The summation of all the contributions from the on gates reproduces the analog equivalent of the digital information received from the tape.

## Additional Features

The limits on the delay of 0.01 to 10 seconds have effectively been expanded by use of a "recirculate" provision, making it possible to transfer information from any output channel back to any input channel without cumulative errors. This is done by making available at a patch panel all bit control flip-flop outputs which may be gated directly back to the write head driver amplifiers so that they are re-recorded without any conversions in place of the usual input information. This enables a single channel of continuous information to be delayed up to 100 seconds by recirculating the information through all ten channels successively. Many variations are possible which make the recirculate feature a versatile instrument. This system is completely transistorized. Printed circuit boards are mounted in slide-out racks making it possible to check any circuit during operation. Major system check points have been brought out to a test jack panel enabling checkout with a minimum of effort.

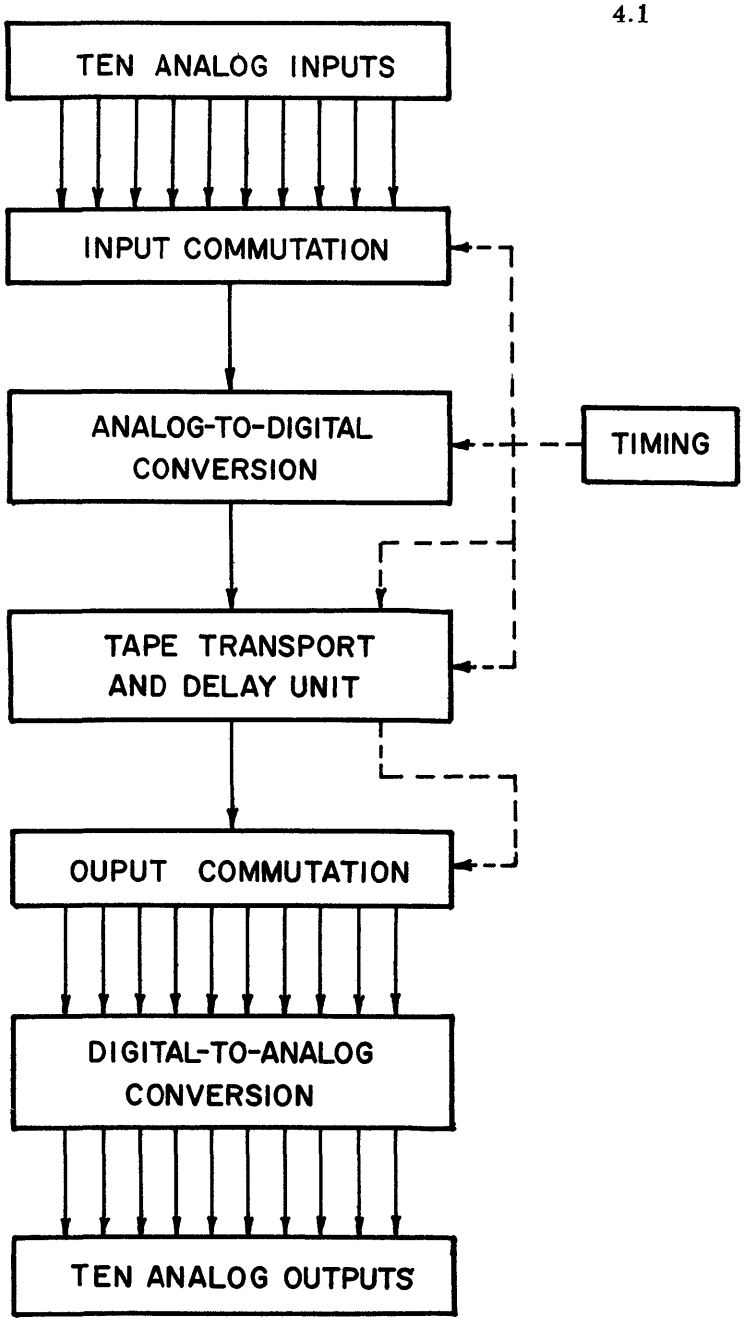


FIGURE 1
INFORMATION FLOW DIAGRAM

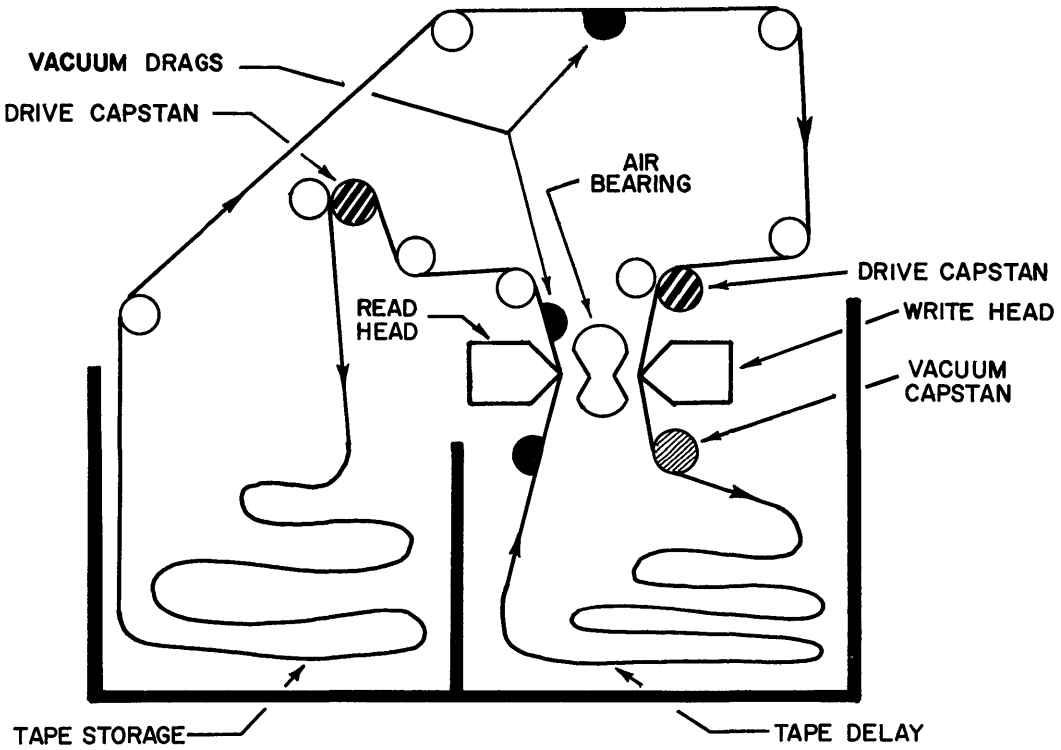


FIGURE 2
TAPE TRANSPORT

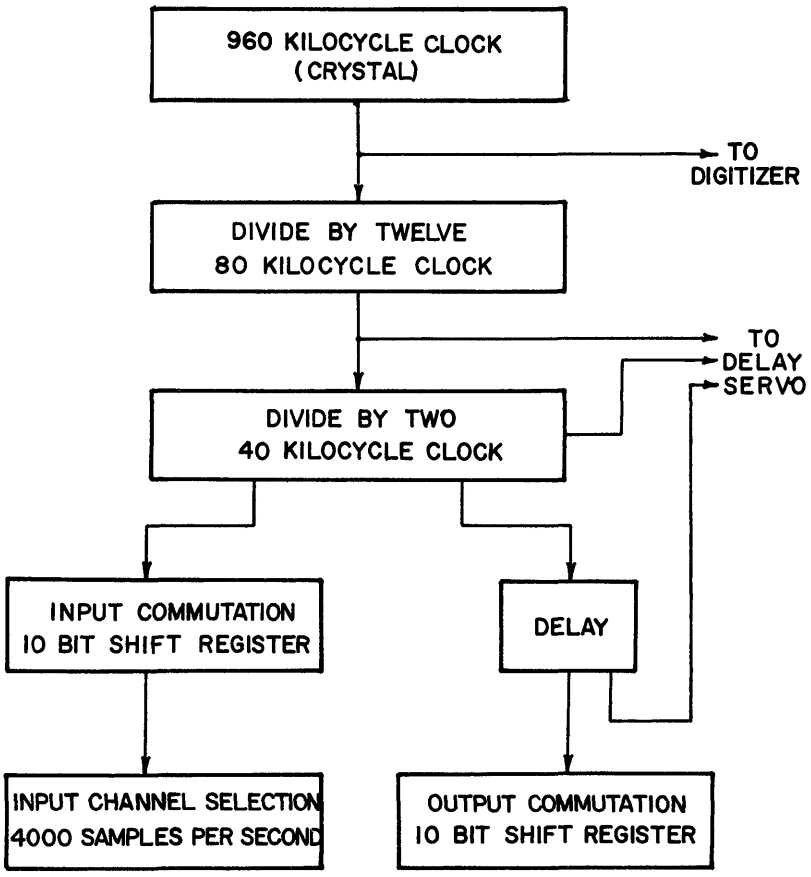


FIGURE 3
CENTRAL TIMING SYSTEM

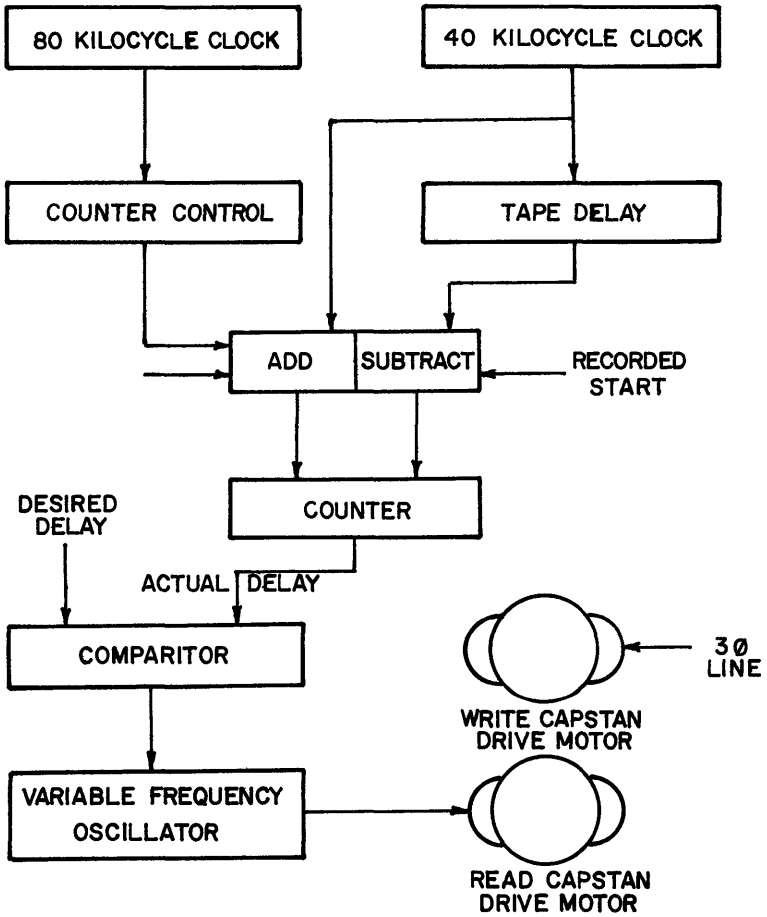


Figure 4
DELAY SERVO

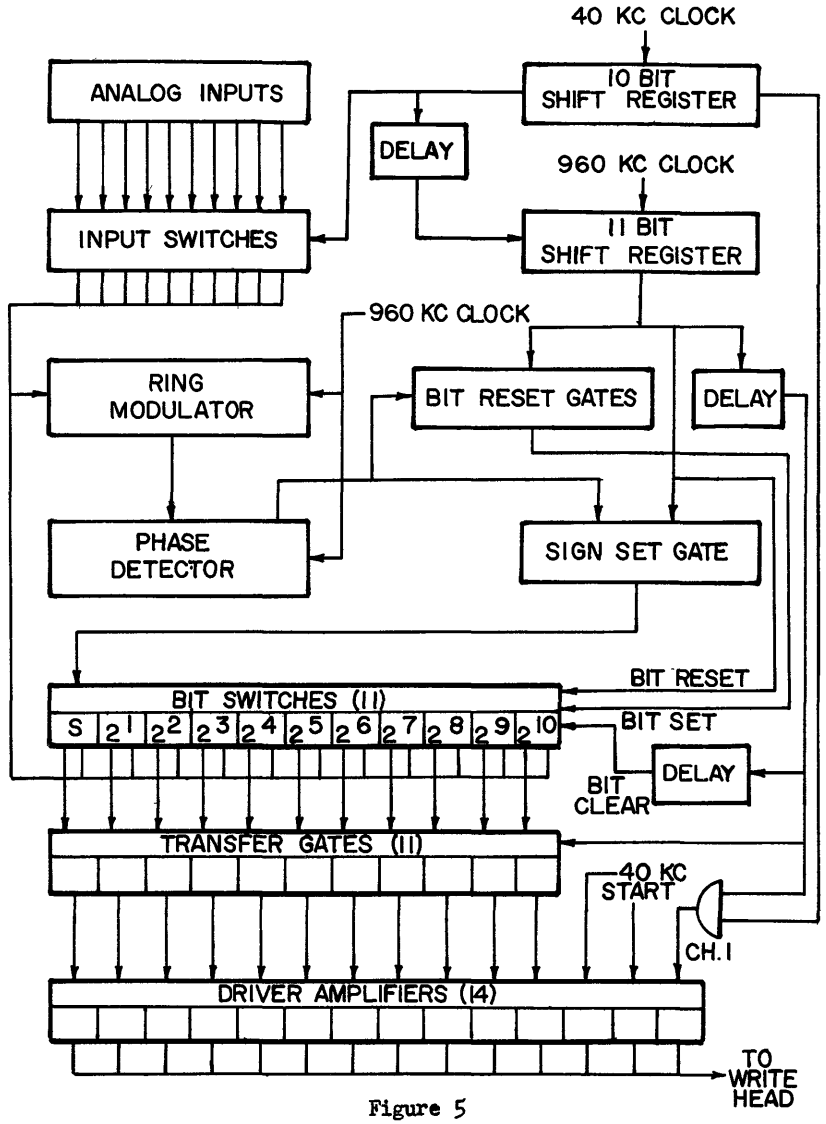


Figure 5
ANALOG TO DIGITAL CONVERSION

| CONTROL | TIME μSEC | OPERATION |
|---|---|---|
| INPUT COMMUTATION SHIFT REGISTER STEPS ON FORTY KILOCYCLE CLOCK | 0 | TURN OFF INPUT SWITCH FOR CHANNEL 10<br>TURN ON INPUT SWITCH FOR CHANNEL 1 |
| | 2 | SWITCHING TIME FOR INPUT COMMUTATION |
| 10 MICROSECOND DELAY OF FORTY KILOCYCLE CLOCK. | 4 | SWITCH. |
| | 6 | |
| | 8 | |
| DELAYED FORTY KILOCYCLE CLOCK STARTS | 10 | IF SUMMING JUNCTION NEG. TURN SIGN BIT ON. |
| ELEVEN BIT SHIFT REGISTER-POSITION 1 | | TURN ON BIT 1 IF SUM. JUNC. NEG. TURN OFF |
| 2 | 12 | 2 BIT 1 |
| 3 | | 3 2 |
| 4 | 14 | 4 3 |
| 5 | | 5 4 |
| 6 | 16 | 6 5 |
| 7 | | 7 6 |
| 8 | 18 | 8 7 |
| 9 | | 9 8 |
| 10 | 20 | 10 9 |
| 11 | | 10 |
| DELAYED ELEVENTH PULSE | 22 | OPEN TRANSFER GATES<br>TURN OFF THE ON BITS TRANSFERRING |
| | 24 | ALL ONES TO DRIVER AMPLIFIERS. |
| | 25 | |

FIGURE 6
TIME-OPERATIONAL SEQUENCE CHART FOR
DIGITIZING CHANNEL 1

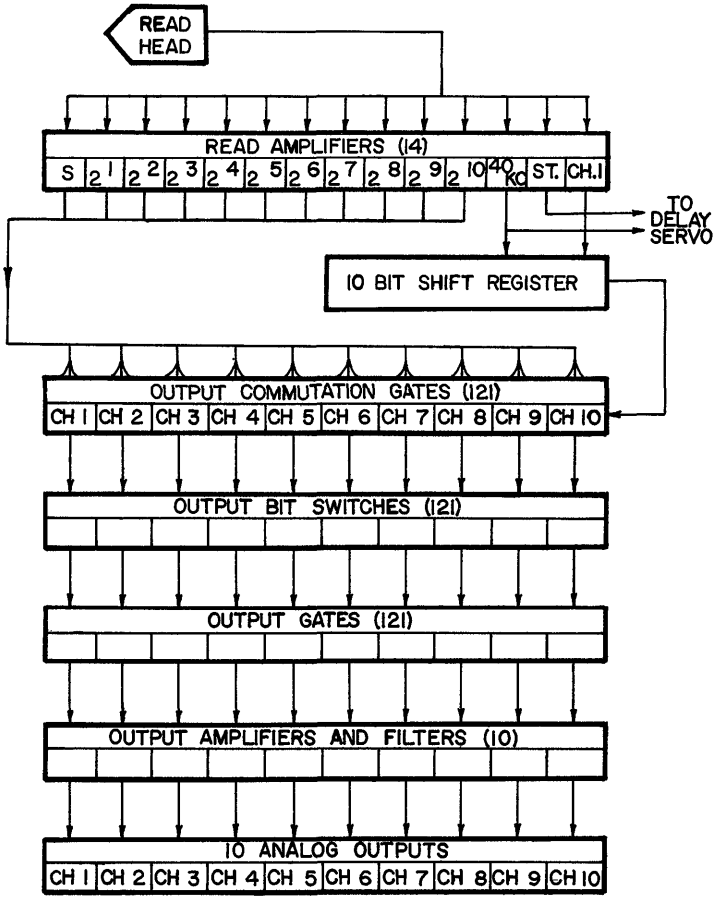


FIGURE 7
DIGITAL TO ANALOG CONVERTERS