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## Abstract

The design of a digital function generator based on incremental digital computer techniques is described which is capable of generating both mathematical functions and arbitrary functions. The mathematical functions are generated using parallel Digital Differential Analyzer methods. The arbitrary functions are obtained by generating interpolating curves through programmed numerical points. The mathematical functions can be generated with a high degree of accuracy and repeatability while the arbitrary functions can be generated to a high degree of repeatability but an accuracy limited by second order interpolation methods.

The interpolating equation generates a curve made up of a chain of parabolic segments passing through thirty-two numerical points which may be unequally spaced along the X axis. Both second order and first order interpolation may be performed.

Fourteen bit incremental Analog-to-Digital and Digital-to-Analog converters are included which enables the use of the DAFT system in conjunction with analog computer facilities. A 3 megacycle clock rate is used, enabling the transfer of information at 100,000 increments per second allowing for very high speed computation.

## Introduction

This paper describes the design for a set of incremental computer blocks. The basic blocks of this system are shown in Figure 1. The incremental inputs and outputs of a number of these blocks may be interconnected to solve a large class of research and development problems. The rate of transfer of information between such blocks is 100,000 increments per second which allows for very high speed computation. The operation of the blocks is numerical to allow for very high computational accuracy. This form of computer system should prove particularly useful for solving those complex problems in which present analog computers exhibit prohibitive total errors.

The Integrator, Variable Multiplier, Constant Multiplier and Servo Units are of the Digital Differential Analyzer type. The DAFT Unit is a Digital/Analog Function Table. The Analog-to-Digital and Digital-to-Analog Converter Units operate incrementally to convert between voltage information and digital information. These converters provide communication links between the incremental computer and either an analog computer or a process control system. The operation of these interconnected blocks is controlled by a central Control Unit. This Control Unit serves to enter problem parameters, monitor the operation of the system, and synchronize the system operation. This equipment can be used to generate many mathematical functions such as shown in Figure 2.

When a function cannot be expressed satisfactorily in an analytic form, the DAFT unit may be used to generate it as an arbitrary function as shown in Figure 3. The mathematical functions can be generated with a high degree of accuracy while the arbitrary functions can be generated to a high degree of repeatability but an accuracy limited by second order interpolation methods.

## DAFT Function Generator

#### General

One particular interconnection of incremental units (see Figure 3) will be given special attention in this report. This system of units accepts an input voltage, X, generates a function, f(X), from a numerical function storage and generates Z = f(X) as an output voltage. In this way an analog function generator is obtained with a very high degree of repeatability.



Fig. 3 Arbitrary Function Generator



Fig. 1 Incremental Computer Blocks



Fig. 2 Mathematical Function Generator

## Incremental Technique

It is characteristic of incremental computers to generate fewer dZ output increments than dX increments. If the X scale of the graph, Z = f(X), is divided into 16,384 dX increments and the Z scale is divided into 16,384 dZ increments, the Z function cannot generally extend over this full scale. Figure 4 indicates the range of Z for several types of functions.



Fig. 4 Incrementally Generated Curves

When the curve is Z = X, the curve can extend over 16,384 dZ's. The maximum excursions for other curves are given below:

% cycle sine curve ----10,420 dZ's
1 cycle sine curve ---- 5,210 dZ's
2 cycle sine curve ---- 2,605 dZ's
4 cycle sine curve ---- 1,302 dZ's
8 cycle sine curve ---- 651 dZ's

This does not mean that the output amplitude necessarily becomes reduced with higher frequency curves (the output amplitude can be scaled up at either the D to A converter or by an output amplifier), but that the resolution between output values becomes coarser.

The scaling of X at 16,384 dX's is consistent with the resolution of a high precision converter and is chosen to give a fine resolution for the output generation.

## Numerical Definition of Z = f(X) Curve

The curve to be defined\_is to be divided into 32  $\Delta X$  increments along the X scale. Each  $\Delta X_i$  will have  $(128)(N_i)$  of dX increments, where  $N_i$  is an integer from 1 to 16. The nominal value for  $N_i$  is 4 so that the nominal value of  $\Delta X_i$  is 512 dX's. Individual  $\Delta X_i$ 's may be onefourth the nominal or four times the nominal, but the sum of the 32  $N_i$ 's should be 128 so as to span the full scale of 16,384 dX's. The X scale may be visualized as divided by 129 grid lines with a spacing of 128 dX's between lines. The values of Z at any 31 of these grid lines may be used to define the curve provided that no more than 15 grid lines are skipped as a group. It is assumed that the first and last grid lines are always used to give 33 values of Z or 32  $\Delta X$ 's and 32  $\Delta Z$ 's.

The Z values are measured in units of dZ increments. The values used for Z and X must be chosen subject to some restrictions.

The first restriction is that  $\Delta Z_i / \Delta X_i$ =  $n_i / 128$ , where  $n_i$  is an integer from -128 to +127. This states that slope,  $\Delta Z_i / \Delta X_i$ , is restricted to one of 256 different values (since  $\Delta X_i = 128 N_i$ ,  $n_i = \Delta Z_i / N_i$ ).

The second restriction is that one of the X-Z points that is chosen be the origin. This requires that curves which do not pass through the origin be displaced vertically be the constant, f(0). This constant can be readily added back to the generated curve in the analog computer as well as in the incremental computer.

The third restriction is that the change of slope between  $\Delta X$  increments be such that  $n_{i + 1} - n_{i} = m_{i}$  where  $m_{i}$  is an integer from -128 to +127.

The fourth restriction is that  $|n_i - \frac{1}{2}m_i| < 128$  which may also be expressed as  $|\frac{3}{2}n_i - \frac{1}{2}n_i + \frac{1}{2}| < 128$ . This is necessary to limit the slope used in parabolic interpolation and will be mentioned later. Note that if the other restrictions are satisfied this restriction will be satisfied whenever  $|n_i| < 64$ .

#### Interpolation Method.

The interpolation formula to be used in the region  $X_i$ , is the following:

$$dZ = \begin{bmatrix} \Delta Z_{i} \\ \Delta X_{i} \end{bmatrix} + \begin{pmatrix} \Delta Z_{i+1} \\ \Delta X_{i+1} \end{bmatrix} - \frac{\Delta Z_{i}}{\Delta X_{i}} \begin{pmatrix} x - x_{i-1} \\ \Delta X_{i} \end{pmatrix} dX - y \begin{pmatrix} \Delta Z_{i+1} \\ \Delta X_{i+1} \end{bmatrix} - \frac{\Delta Z_{i}}{\Delta X_{i+1}} dX$$
or

$$dZ = \begin{bmatrix} n_{\underline{i}} \\ 128 \end{bmatrix} + \begin{pmatrix} m_{\underline{i}} \\ 128 \end{pmatrix} \begin{pmatrix} X - X_{\underline{i}-1} \\ 128N_{\underline{i}} \end{pmatrix} dX - \frac{1}{2} \begin{pmatrix} m_{\underline{i}} \\ 128 \end{pmatrix} dX.$$

Figure 5 shows the interpolation curves for Z in the intervals,  $\Delta X_1$  and  $\Delta X_2$ 



Fig. 5 Interpolation Curves

In general, the interpolation formula yields a curve that is a chain of parabolic sections. The parabola used in the increment  $\Delta X_{i}$  passes

through three points:

1) 
$$x_{i-1}, z_{i-1}$$
  
2)  $x_{i}, z_{i}$   
3)  $x_{i} + \Delta x_{i}, z_{i} + \frac{\Delta z_{i+1}}{\Delta x_{i+1}} \Delta x_{i}$ 

This linearly interpolated third point is much easier to use than  $(X_{i+1}, Z_{i+1})$  for the third point of the parabola.

The interpolation system is indicated by the block diagram in Figure 6. The dX increments, of which there are 128 N<sub>i</sub> as X varies through  $\Delta X_i$ , are scaled down in number by  $1/N_i$ to give 128 increments per  $\Delta X_i$ . The increments are scaled down further in number by 1/128 to give one increment per  $\Delta X_i$ . These i increments are summed in the i counter to control the selection of m<sub>i</sub> and N<sub>i</sub> from the storage.

As X varies through  $\Delta X_i$ ,  $m_i$  is added into the A register 128 times. The A register has 64 in it at the beginning of  $\Delta X_i$  (this is 1000000 in binary). After  $m_i$  has been added into the A register 128 times, the A register will have overflowed  $m_i$  times and again have 64 in it. The overflows of the A register are summed in the B register. At the beginning of each  $\Delta X_i$  increment, the B register contains the value,  $n_i$ , which is increased by  $m_i$  to  $n_i + 1$  at the end of the  $\Delta X_i$  increment. While X varies through the  $\Delta X_{i}$  increment,  $m_{i}$  is added into the C register 128  $N_{i}$  times. The C register operates much like the A register, beginning and ending with 64 in it, but overflowing  $(N_{i})(m_{i})$  times. These overflows are scaled down by - $\frac{1}{2}$  and summed with the overflows from the D register to obtain the dZ output increments.

While X varies through the  $\Delta X_{i}$  increment, the arying value in the B Register is added into the D register  $128N_{i}$  times. The value added from the B register into the D register corresponds to  $n_{i} + m_{i} (X-X_{i-1/128N_{i}}) dX$  from the interpolation formula. The output from the -½ scaler added into the D register corresponds to -½(m<sub>i</sub>) dX

from the interpolation formula. By taking the overflows for the sum of these terms from the 7-bit D register, we obtain a 1/128 factor or

$$dZ = \frac{1}{128} n_{i} + m_{i} \frac{X - X_{i-1}}{128N_{i}} dX - \frac{1}{128} \frac{1}{2} m_{i} dX$$

The DAFT Unit operates as a numerically drift-free interpolator which traces out a smooth curve through the  $Z_i$  points regardless of the number of cycles of the X input voltage. This curve will have a point by point uniformity for all cycles of X.

When linear interpolation is desired, the overflow signals from the C register may be used as the d Z output and the A, B and D registers not be used. The curve traced in this case will be a chain of straight line segments joining the  $Z_i$  points. The values of n will be taken from



Fig. 6 Interpolator Block Diagram



Fig. 7 Patchboard Storage Circuit

<i>?n /</i> , , , , , , , , , , , , , , , , , , ,			
m 2	Nź	m 19	Nig
771 3	N <sub>3</sub>	M 20	NZO
m.4	N4	m 21	NZI
<i>m</i> 5	N <sub>5</sub>	m 22	NZZ
me	NG	m 23	N23
m.7	Ny	M24	N24
me	Ng	m 25	Nes
m g	Ng	M 26	NZ6
mio	N/0	me7	N27
m <sub>11</sub>	N//	m 28	NEB
m12	N12	<i>™</i> -29	N 29
m_/3	Nız	m 30	Ngo
<i>m</i> .14	Niq	M31	N3,
M.15	NIS	<i>m32</i>	
m16	N16		
			<u>i</u> i i i i

Fig. 7a Function Patchboard Layout

116 4.2

storage rather than  ${\tt m}_{\underline{i}}$  . Only the first two restrictions on the X-Z points will apply in this case.

# Method of Operation

The design of the system is arranged for ease of operation and testing. To set the function generator system into operation, the function patchboard is inserted into the DAFT Unit and the Control Unit Reset button pressed. Pressing this button does the following:

- 1) Clears the X and Z counters in the converters to zero.
- Transfers the origin values of n and i from the patchboard into the B register and i counter of the interpolator.
- Sets 64 into the A, C and D registers and clears the Scalers of the interpolator.

When the Control Unit is switched into computation, the function generator system proceeds to generate the curve Z = f(X) from the origin to the current value of the X input voltage in 0.082 seconds or less. The function generator will then track on the variations in X until the Control Unit is switched out of computation. When the system is switched out of computation, the values of X and Z are locked on the last computed point of the curve. When computation is restarted, the generator will slew at the rate of 100,000 dX's per second to the current value of X.

To perform a quick test for errors in the operation of the generator, the push button to set the X input to zero may be pressed. The X and Z indicators should both slew to a zero reading when this button is pressed and back to the current (X,Z) point when this button is released.

To verify the operation of a new function patchboard, the manually controlled X input voltage may be used to obtain the  $(X_i, Z_i)$  read-

ings on the indicator lamps that are prescribed for the function. When the readings are incorrect, the patchboard can be corrected and the revised data verified directly.

# Circuits

All circuits are designed using germanium transistors and diodes. No tubes or mechanical choppers are used. All components are used at a conservative power and tolerance rating. The design goal is to achieve very reliable operation at low power consumption. The converter units use the circuits developed for the Packard Bell Computer Corporation MULTIVERTER equipment.

The circuits used for the DAFT interpolator are the circuits used in the Packard Bell Computer Corporation TRICE computer. These circuits consist of transistor flip flops, diode gates, and distributed delay line storage elements.

Figure 7 shows the gating circuit designed for the Patchboard Storage Unit. This circuit has the moderate speed requirement of obtaining a new set of values on its 12 output lines within five microseconds after the i counter changes. One of 32 diode-and-gates transmits a DC signal depending on the state of the i counter. This signal is sent through an emitter follower at an 8-volt level to a 12-contact common of the patchboard. The signal is connected or disconnected with patchboard jumper to twelve diode-Or-gates. The twelve Or-gate lines present the interpolator with the  $m_i$  and  $n_i$  values in parallel.

When the Reset Signal comes from the Control Unit, it is used to block the reading of  ${\rm m}_{\rm q}$  and

n, values and introduce the value for n at the

origin on the Or-gate lines. This signal is also used to transfer the value for i at the origin to the i counter flip flops.

## X Frequency Response and Accuracy

The DAFT Unit has a maximum operation rate of 100,000 dX increments per second. This rate is chosen to be compatible with the other units of the system. When the X scale is divided into 16,384 dX increments, the value of X for a sinusoidal input of frequency, f, is given by

 $X = (16, 384/2) \sin 2\pi ft$ 

and the maximum rate of change of X is

 $(dX/dt) = 16,384\pi f.$ 

Therefore, the system will track if the maximum full scale input frequency is

 $f = 100,000/16,384 \gamma = 1.95 \text{ cps.}$ 

When the tracking frequency of 1.95 cps is exceeded by a signal of, say, 3 cps, the Analogto-Digital Converter fails to follow closely the steep portions of the input curve. Figure 11 indicates the discrepancy that will occur in this case. The result is approximately a triangular wave with 5% amplitude reduction, a maximum error of 21% of full scale and a phase shift of  $20^{\circ}$ . The function generator continues to function properly but for the distorted input curve.

The described system units can be used at

higher frequencies by reducing the number of dX's per full scale of X. For example, the X input resistor of the Analog-to-Digital Converter can be changed to give 8,192 dX's per full scale of X and the sum of the N<sub>i</sub> values reduces to 64.

The maximum full scale input frequency can then be 3.9 cps. The number of dX's for full scale can be further reduced to 4096 and all  $32 N_{1}$ 

values restricted to 1's. This will accomodate a full scale input frequency of 7.8 cps.

In general, the following relationship exists between frequency and the number of dX's:

(number of dX's/full scale of X) =  $100,000/\pi f$ 

When the curve, Z = f(X), is characterized as a sine curve of C cycles, '

(number of dZ's/full scale of Z) =  $(1/\pi C)$  (number of dX's/full scale of X)

Therefore,

(number of dZ's/full scale of Z)

 $= 100,000/\pi^2$  Cf = 10,132/Cf

Where the output is expressed as a binary number with p binary stages used, the formula may be written as

2<sup>p</sup> = 10,132/Cf

This last equation essentially defines the frequency-accuracy product of the DAFT function generator system.

As an example, if the input frequency is 3 cps and the Z = f(X) curve resembles 2 cycles of a sine curve, the generator can be set up to give an output curve that is smooth to one part in 2<sup>10</sup>. No. of dX's = 100,000/ $\pi$  (3)  $\cong$  10,496 = (82)(128)

$$\sum N_i = 82$$
  
No. of dZ's = 10,496/ $\pi$  (2)  $\cong 2^{10}$   
for C = 2 cycles and f = 3 cps

For another example, if the input frequency is 30 cps and the Z = f(X) curve resembles one cycle of a sine curve, the generator can be set up to give an output curve that is smooth to one part in 2<sup>8</sup>. Only eight  $\Delta X$  increments may be used for this input frequency.

No. of dX's = 100,000/
$$\pi$$
 (30)  $\cong$  1024 = 8(128)  
 $\sum N_i = 8$ 

No. of dZ's =  $1024/\pi(1) \cong 2^8$ 

for C, = 1 cycle and f = 30 cps

In order to obtain more  $\Delta X_{i}$  increments for high frequency inputs, the DAFT Unit will have one other scaling arrangement:

- The 1/128 Scaler will be changed to a 1/16 Scaler
- 2) The B register will be shortened to 4 bits plus sign.
- 3) The number of dX's/ $\Delta X_i = (N_i)(16)$
- 4) n; will be an integer from -16 to +15
- 5) m, will be an integer from -16 to +15
- 6)  $|n_i \frac{1}{2}m_i| < 16$

The last example may then have all 32  $\,$  X increments used

No. of dX's = 100,000/ $\pi(30) \cong 1024 = 64(16)$   $\sum N_i = 64$ No. of dZ's = 1024/ $\pi(1) \cong 2^8$ for C = 1 cycle and f = 30 cps

# Summary

The set of units described provide a flexible, high performance system with which arbitrary functions and mathematical functions can be obtained at high speed and high accuracy. The arbitrary functions are set up in numerical form on a patchboard and generated with first or second order interpolation. The mathematical functions are generated in their analytic form with interconnected Digital Differential Analyzer units. The performance of the system in generating both types of functions is approximated by the formula

$$2^{p} = 10,132/Cf$$

where

- p = number of binary bits precision
   (including sign) in the output,
- C = The complexity of the function measured in terms of the number of sine curve cycles it contains,
- f = the full amplitude input frequency
   of the independent variable input.

The independent variable may be followed to a precision of one part in 16,384 and the

output variable may be generated up to a precision of one part in 10,000. The system operates at the rate of 100,000 cps so that in the worst case, the delay between a variation in the input and a corresponding variation in the output will be much less than 50 microseconds.

Another type of function not treated explicitly in the body of this report is that of generating an analytic function of time such as

 $Z = \sin 2\pi ft$ 

This function can be generated with a performance formula of

 $2^{p} = 100,000/ f$ ,

where p is the number of bits precision (including sign) in the output. The value of p is limited to 14 or less by the output converter. For f of 64 cps the sine can be generated to 8 bits plus sign and for f of 200 cps the sine can be generated to 6 bits plus sign. These curves can be generated for an unlimited number of cycles without amplitude drift.



Fig. 8 Slope - Limited Tracking Curve