COMMUNICATIONS WITHIN A POLYMORPHIC INTELLECTRONIC SYSTEM

George P. West, Ralph J. Koerner
Intellectronics Laboratories, Ramo-Wooldridge
Canoga Park, California

Summary

A multiple-computer system, employing several computers of intermediate capacity, provides many system advantages over conventional large-scale computing systems. A multi-computer system requires effective communication of data and control signals between modules of the system. This paper briefly describes the RW-400 Data Processing Central, a new polymorphic data processing system. The communications problems associated with such a system are discussed, and a high-speed electronic switch employing multiple-aperture magnetic cores to provide system communication is described. The utilization of this high-speed switch in providing efficient data communication, as well as effective control of the system modules, is explained.

With increased automation of large-scale data processing applications, the trend has been to larger memories, higher clock rates, and increasingly complex arithmetic units. This approach is not entirely satisfactory, particularly from cost and reliability standpoints. A multiple-computer approach employing several computers of intermediate capacity provides many system advantages. A novel organization of more or less conventional computational elements, communicating in a common format by means of a high-speed electronic switching network, provides a data processing system which can assume many different forms. Such a polymorphic system can be more nearly tailored to the requirements of a particular application, since storage capacity and arithmetic capability can be adjusted independently, in relatively small increments to match the requirements at hand. Furthermore, changing operational requirements can be matched by expanding the system economically, without obsolescence of existing equipment or programs, merely by adding additional computers or memory devices. Finally, the system can be programmed to adjust its own performance to meet rapidly changing operational requirements by shifting computational capacity from one assignment to another.

The RW-400 system is a multiple-computer system of this type, capable of simultaneously processing multiple tasks with extremely short time requirements for the completion of each task. The Computer Modules of the RW-400 system employ a powerful two-address order code providing three optional forms of each arithmetic instruction. These options may be utilized to specify the contents of the accumulator as one of the operands, providing in effect a two-plus address structure. A magnetic core memory of 1024-word capacity, and 10-microsecond memory cycle, is provided with each Computer. Control and synchronization of computations is exercised by a generalized program interrupt feature. Each Computer is capable of recognizing one or more external interrupt conditions to force a branch in the computer program. Each Computer is provided with a masking register which can be loaded by the computer program to specify which of the 13 possible external interrupt conditions, as well as which of the internal interrupt conditions, will be effective at any instant of time.

The system employs novel magnetic core buffer memories (Buffer Modules) to augment the memory provided with each Computer Module. The Buffer Modules make possible rapid, efficient transferral of data and programs within the system. Each Buffer Module is capable of independently executing a stored program which permits it to gather data from magnetic tapes, drums, or the system input-output buffers. Similarly, the Buffer Module can distribute results under the control of its own stored program. The Buffer Module may also be used to augment the memory of any of the Computer Modules; in this mode, operands taken from the Buffer memory may be utilized by the Computer Module almost as rapidly as operands from the Computer's internal memory.

The system employs magnetic tapes, magnetic drums, printers, plotters, and input-output buffers as independent modules. All of these modules communicate with one another by means of a high-speed electronic switch, similar in many respects to a telephone exchange. Figure 1 illustrates a typical system configuration. The Central Switching Exchange can be tailored to the needs of the system, and may easily be expanded to accommodate system growth. The remainder of the paper discusses the design objectives for an adequate central switch, and develops a switch design which fulfills these design objectives.

The data switch must provide multiple paths so that each Computer can communicate without delay or interference. Control of the switch points must be rapid (less than 100 microseconds) and convenient so that Computer time is not wasted in manipulating the switch. The switch must test for a busy condition before making the connection, to prevent interference with communications in progress. The switch should be reliable, providing alternate paths for communication so that failure of a cross-point does not disable the system. The switch should be modular to provide for system growth. Since new problems must be checked out while the system is in normal operation, a means of restricting the accessibility of modules must be incorporated in the design. For example, in checking out a program that involves a Computer, a Buffer and two Tape Modules, it is necessary to restrict the switching capability so that the Computer and Buffer can control connections only between the modules being code-checked. This feature

prevents the new program from interfering with normal system operation.

The RW-400 data switch employs transfluxors (double-aperture cores) as the switching element. The principle of operation is analogous to that of a transformer connection which can be disabled by saturating the iron to prevent the flux linkage of normal transformer action. Some of the desirable properties of the transfluxor switching element are extreme reliability, small size, low cost, low power consumption, connection memory, ease of control, and bilateral signal flow characteristics. Figure 2 is a diagram of a transfluxor crossbar switch.[1] In this array, the transfluxors are selected by coincident currents.

Assume a "connection" to be made and signal flow to be taking place between Signal Input 2 (S_2) and Signal Output 3 (O_3) through core 10. Signal flow consists of a train of alternately positive and negative pulses of current along S_2 which are inductively coupled by core 10 to O_3; O_3 in turn is attached to the load.

To "disconnect" or open the path between S_2 and O_3, a blocking pulse of current is introduced along blocking line B_3. This blocking pulse blocks all possible signal paths for O_3, specifically cores 9, 10, 11, and 12.

To establish a new connection, between S_3 and O_3 for example, core 11 must be unblocked. This unblocking is accomplished by passing coincident unblock currents through lines UB_3 and B_3.

A transfluxor plane is provided for each signal line required between the computation modules. The RW-400 switch provides separate line groups employing 18 lines for communication in each direction. Consequently, the RW-400 switch employs 36 transfluxor planes. Control of the switch is obtained by providing an input commutator which samples each of the active input lines in turn. The commutator position controls one axis of the coincident-current selection, while the other axis is specified by a Command Output instruction from the Computer or Buffer being sampled by the commutator. An additional transfluxor plane is provided to record the status of each cross-point. In this way, it is possible to test the additional plane to determine whether the connection requested is available or busy. If the device requested is busy, the connection request is rejected without interfering with the communication already in progress. This basic switch configuration meets all of the design objectives except two, which are discussed below.

Control of the switch is rapid. Since the commutator speed depends upon the number of connection requests which must be serviced, the service time for a switch instruction will vary. Average service time is estimated to be about 50 microseconds. The switch tests for a busy condition before making a connection. Magnetic switching elements promise high reliability. Alternate paths are available by employing Buffer Modules in the transfer. The switch is modular in the sense that all circuits for a given set of input or output lines are packaged on a single 19-inch insert card. A cabinet with power supplies and all the transfluxor planes forms the basic switch. As additional modules are required in the system, line circuits are added as required. Line circuits constitute about one-half of the cost of the switch.

One of the design requirements which is not met by this simple design is the ability to restrict the setting of some of the cross-points. This design requirement to inhibit certain connections could be met by adding another transfluxor plane in which allowed cross-points would be recorded by blocking or unblocking the transfluxor corresponding to the cross-point. The memory plane would then be tested to see if the connection is allowed, in the same way that a test for a busy circuit is made.

The other design requirement which is not met is harder to rectify with this simple design. Control of the cross-points of the switch in this design is not particularly convenient, since the addresses used in the switching commands must correspond to the physical location on the switch matrix of the module selected. A design which would permit the programmer the use of arbitrary tags in his program, for the modules he intends to use, would be much more useful. When the program is complete, the tags used by the programmer could be entered in a memory in the switch before the program is executed. In this way, the switch could properly interpret the tags and select the desired module. In other words, a system of symbolic addressing for the switch would be much more convenient than an absolute addressing scheme. A very rapid table look-up operation is necessary to interpret the symbolic addresses within the switch.

A transfluxor memory device, called an Interrogation Module, which performs this table look-up very rapidly, has been developed by Ralph Koerner of Ramo-Wooldridge. The transfluxor memory employs two cores to store each bit position, one for each of the two possible states of the bit. The bits of the words which constitute the table are entered in parallel along one axis of the memory plane, while word positions along the other axis of the plane are designated by a read-in signal. Figure 3 illustrates the principle of operation of a three-bit Interrogation Module. The normal or clear position would have all cores unblocked. Words are entered into the memory in such a way that a logical "one" unblocks the "one" core and blocks the "zero" core of the pair of cores associated with the bit position, while a logical "zero" blocks the "one" core and unblocks the "zero" core. If, now, the complement of a number is used to interrogate the memory along the vertical lines threading all word positions, all of the output lines will have signals coupled to them by the transfluxors except that line corresponding to the memory position which stores the word exactly matching the word at the input of the interrogation unit. For that word only, the input signals will all traverse blocked cores, since the stored word and the interrogating word are complements. This Interrogation Module can be incorporated in the design of the switch to provide symbolic addressing; but even more important, it greatly simplifies the problem of interrupt communication within the system.

Interrupt communication is necessary to coordinate, synchronize, and control the operations of the individual Computers to provide the best

overall performance. The interrupt feature is a means of forcing a branch in the computer program by the use of an external electric signal such as is generated by depressing a push-button. In the RW-400 system, most interrupt signals originate from Computer or Buffer Modules; however, other devices such as the input-output buffers, provide signals which can be utilized as interrupt signals. When interrupted, a Computer must determine the meaning of the interrupt signal and its source. Some information as to intent or source of the interrupt can be conveyed by the bit position in which the Computer receives the interrupt. Unless a directed system of interrupts is employed, the bit assignments are rapidly used up specifying which Computer or Buffer should respond to the signal.

As an additional means of coordinating system actions, a digital clock is provided which can be read by any Computer or Buffer. The clock is more useful when it generates an interrupt signal at the end of a prescribed interval of time, directing it to the appropriate Computer or Buffer. The directed interrupt is an important system requirement.

Figure 4 illustrates a switch design which employs an Interrogation Module to control the simple data switch described earlier. The commutator samples the input lines in turn, routing the address tag specified by the Command Output instructions to the Interrogation Module. In general, the commutator position determines the selection along one axis, while the output of the Interrogation Module determines the selection along the other axis. The Interrogation Module is provided with additional word positions which are used to route interrupt signals to specified Computers. Note that the digital clock is sampled along with the Computers and Buffers at the input to the switch. By placing a time value in one of the interrupt words of the Interrogation Module, an interrupt is generated when the digital clock value equals the pre-stored time. In this way, Computer interrupts can be generated at specific time intervals. In normal system operation, Buffer Modules read or write the tape or drum records so that Computers usually accept data from Buffer Modules or deliver data to Buffers. For this reason, it is convenient to permit a Buffer to connect itself to a Computer if the Computer connection is not busy. When the Buffer stops its self-instruction program, interrupting the Computer, the Computer can use the results immediately without loss of time manipulating the switch. This type of connection is obtained by assigning either Computers or Buffers entry to both the x- and y-axis of the switch. The figure shows Buffers on both axes of the switch. If there are fewer Computers than Buffers in the system, the Computers would receive this double assignment so as to conserve the number of y-connections available to the system.

The Interrogation Module provides a ready means of restricting accessibility of certain cross-points of the switch. The word length is increased beyond that required for the selection address, and the extra bits are interrogated by the commutator position, while the selection address interrogates the rest of the word. Selection is inhibited unless the correct commutator code is stored in the memory of the Interrogation Module. Note that, by interrogation with "zero's" on both wires of a bit position, no signal is generated at the output, regardless of how the cores are set. In this way, it is possible to ignore certain fields of the interrogation word. If the commutator position interrogation occurs using an assigned bit for each commutator position, more than one device can be permitted to control a given switch selection. This is accomplished by setting into the commutator field of the Interrogation Module the proper bits for that selection word. In this way, identical switch address tags may be used concurrently in two different computer programs without confusion, since each will be assigned a different commutator bit by the Master Computer in setting up the assignment table. The bit will differentiate between the two Computers which are in simultaneous operation; thus, the switch can distinguish between the two identical address tags by determining which Computer is using the tag.

The use of the Interrogation Module in conjunction with the transfluxor switch provides a very convenient means of solving the difficult communication problem associated with data switching and interrupt control within a polymorphic computer system.

References

1. J.A. Rajchman and A.W. Lo. "The Transfluxor," Proceedings of the IRE (March 1956), pp. 321-332.

2. J.A. Rajchman and A.W. Lo. "The Transfluxor," Proceedings of the IRE (March 1956), pp. 321-332.

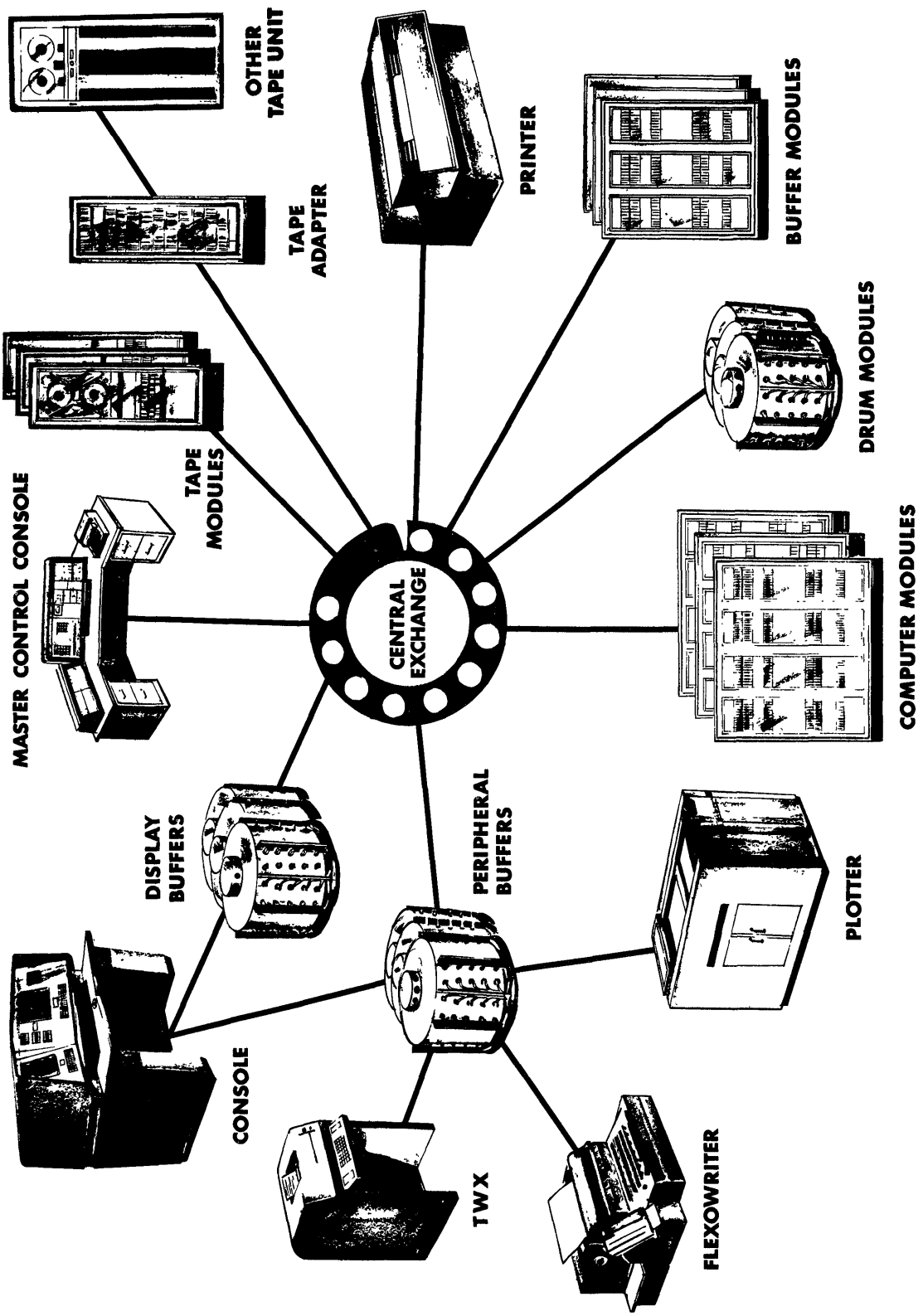

Figure 1
SYSTEM DIAGRAM

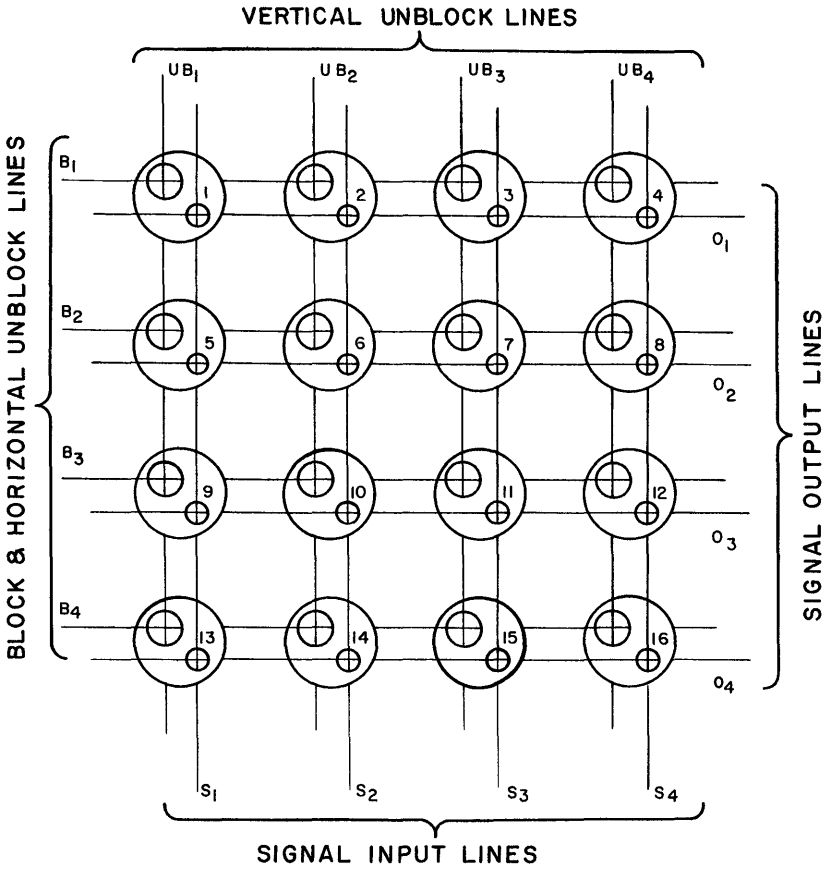

Figure 2
TRANSFLUXOR CORSSBAR SWITCH (SEE REFERENCE NO. 2)

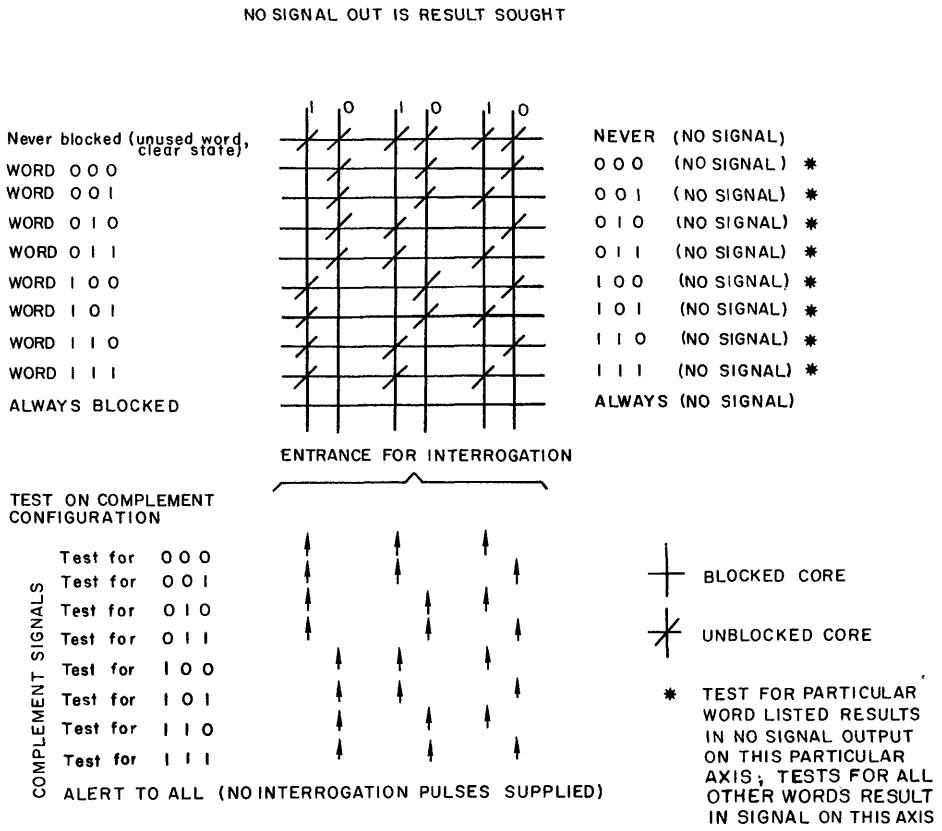

Figure 3
THREE-BIT INTERROGATION MEMORY

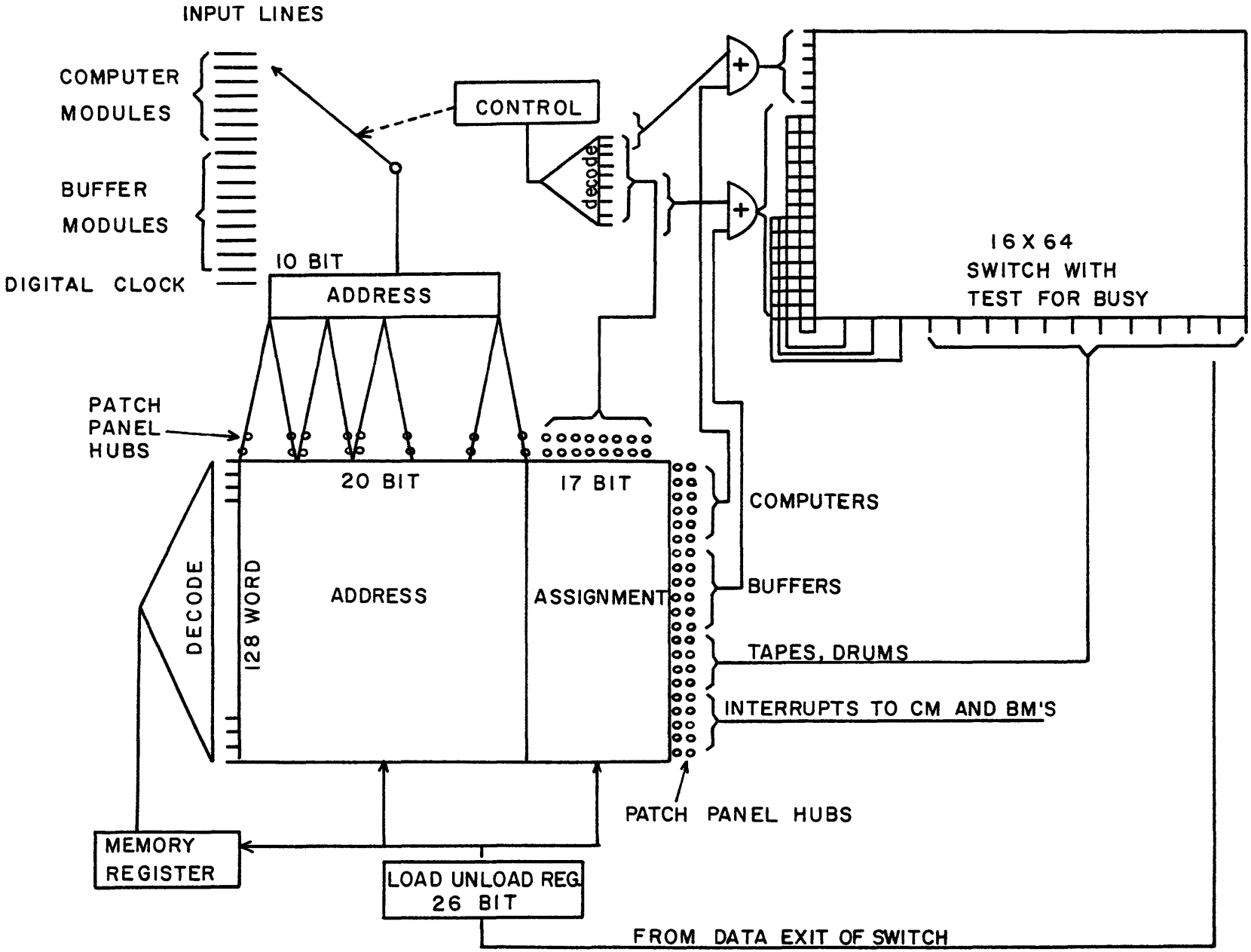

Figure 4
SWITCH DESIGN EMPLOYING INTERROGATION CONTROL