

FIXED, ASSOCIATIVE MEMORY USING EVAPORATED ORGANIC DIODE ARRAYS

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INTRODUCTION

The use of fixed or read-only memories to store permanent or semi-permanent data has been widely treated in the literature.¹ Associative or content-addressable memories, discussed more recently,² provide the important capability for rapid parallel searching and retrieval of stored information. A fixed, associative memory can be used in applications requiring storage of encyclopedic data which must be searched at very high speed. Large capacity stores such as library and other catalog search files, language translators and medical diagnostic tables, as well as small stores such as code converters, computer program memories and other real-time search files, may be of this type.

A magnetic realization of a fixed, content-addressed memory was discussed by Goldberg and Green³ in May 1961. An interrogation

routine to resolve multiple responses in this type of file was described by Frei and Goldberg⁴ in December 1961.

The work on which this paper is based began, first, with the realization that a symmetrical diode matrix exhibits the basic retrieval properties of an associative memory and, second, with the development of techniques to fabricate diode arrays by vacuum evaporation of organic films.⁵ One result of this investigation already published,⁶ was a very efficient algorithm for retrieval of multiple "matches" from a file of this type.

SYMMETRICAL DIODE MATRIX

Consider the diode array shown in Fig. 1. It is composed of w word lines (rows) and b pairs of bit lines (column pairs) and therefore stores w words, each b bits in length. At every row and column-pair intersection is a diode, one of whose terminals is connected to the word line. A "0" is stored by connecting the other terminal of the diode to the right column of the pair. Connecting the diode to the left column indicates

¹ An extensive bibliography on fixed memories can be found in the survey paper by D. M. Taub, "A Short Review of Read-Only Memories," Proc. IEE (British), vol. 110, No. 1, pp. 157-166, January 1963.

² A comprehensive bibliography on associative memories can be found in the survey article by A. Corneretto, "Associative Memories," Electronic Design, Vol. 11, No. 3, pp. 40-55, February 1, 1963. A set of three papers on associative memories is published in Proc. Pacific Computer Conference, Cal. Tech., Pasadena, Calif., pp. 96-130, March 15-16, 1963.

³ J. Goldberg and M. W. Green, "Large Files for Information Retrieval Based on Simultaneous Interrogation of All Items," Proc. Symposium on Large Capacity Memory Techniques for Computing Systems (book), edited by M. C. Yovits, published by Macmillan Co., N. Y., pp. 63-77, May 23-25, 1961.

⁴ E. H. Frei and J. Goldberg, "A Method for Resolving Multiple Responses in a Parallel Search File," IRE Trans. on Electronic Computers, Vol. EC-10, No. 4, pp. 718-722, December 1961.

⁵ A. Sussman, "Rectification in Evaporated Thin Films of Copper Phthalocyanine," Joint Symposium in Thin Films, Electrochemical Society, Pittsburgh, Pa., April 14-18, 1963.

⁶ M. H. Lewin, "Retrieval of Ordered Lists From a Content-Addressed Memory," RCA Review, Vol. XXIII, No. 2, pp. 215-229, June 1962.

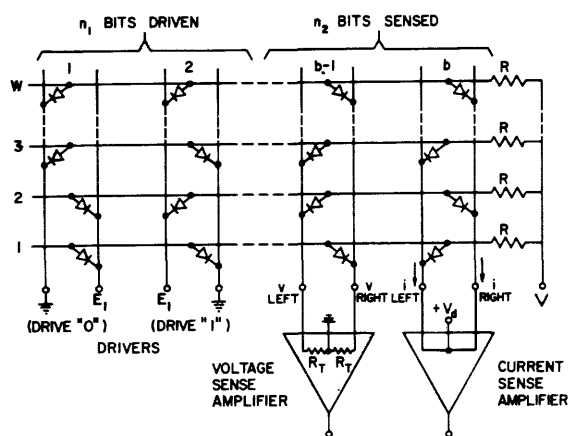


Figure 1. Diode Associative Array.

a "1" stored. Thus, the pattern of connections determines the information stored in the array. Every row is returned, through a resistor R , to a common voltage source V . For sufficiently large R and V , it sees a relatively constant current source looking into R . Each of the columns is terminated with either a driver or a sense amplifier. A given column-pair (bit) is driven with a "0" if the left column is grounded while the right column is connected to a voltage source E_1 . Alternatively, one drives a "1" by reversing these conditions. Thus, pairs of bit lines are always driven with complementary signals. The sense amplifiers may be either voltage or current amplifiers, both of which are illustrated in Fig. 1. R_T may be considered as the input impedance of a voltage amplifier. V_i , the voltage to which the input of a current amplifier is returned, is the maximum forward drop across a memory diode conducting a current V/R . A positive sensed voltage v or positive sensed current i indicates a "1" sense signal. No sensed voltage or current denotes a "0". To keep the discussion general, assume each sense signal is amplified by a separate sense amplifier (two per column-pair). Under some conditions a single sense amplifier per sensed digit may be adequate. A difference amplifier for each pair of sensed columns can also be used.

One can divide the matrix into two parts: n_1 bits driven (inputs) and n_2 bits sensed (outputs), where $n_1 + n_2 = b$. In Fig. 1 the left portion is driven while the right portion is sensed. (Note that every row is the output terminal of an n_1 -input diode AND gate.) As-

sume, for a given set of inputs, only one row develops a relatively positive ("1") voltage (i.e., it is selected). All other rows are clamped to ground (inhibited) and each of their currents V/R is steered to ground through at least one conducting diode connected to a grounded column wire. Those sensed columns which are coupled via diodes to the selected row will also be driven positive. Alternatively, one can say that the V/R current for the selected word is steered to split among those of its diodes which are connected to sensed columns. (Note that each sensed column is the output terminal of a diode OR gate. The number of inputs to the gate whose output terminal is the left (right) column is equal to the number of words which store a "1" ("0") in that bit position.) Thus, the pattern of sensed voltages or currents will correspond to the pattern of diode connections between the selected row and sensed columns. Such an arrangement can be used as a decoder-encoder combination or as a fixed memory. In the first case, one is translating from an n_1 -bit code to an n_2 -bit code. In the second case, the n_1 bits are the address of an n_2 -bit word stored. More generally, this array can be used as a content-addressed memory as is explained below.

The important property of such a matrix is the symmetry or reversability involved. For example, one can reverse input and output roles (i.e., drive the bits on the right side and sense those on the left side) to obtain an n_2 -bit to n_1 -bit decoder-encoder. In fact, any column-pair can be either driven or sensed—that is, serve as an input or an output. Thus, in the general case, any arbitrary number of bits, scattered in any manner among the b bit positions, can be driven while the remaining bits are sensed. The fact that this yields a content-addressable memory can be made clear with a simple example. Suppose one asks for retrieval of all words (assume there is only one, to begin with) which answer the following specification: "0" in the 1st place, "1" in the 4th place, "1" in the 8th place, etc. All of the column-pairs in the positions designated above are driven with polarities corresponding to the specified bits (tag bits or descriptors). All unspecified digit line pairs (i.e., the 2nd, 3rd, 5th, etc.) are sensed. Thus, sensing a pair of columns cor-

responds to a "don't care" or "0" specification for that bit. (The interrogation word for this case is 0001000100 . . .) Clearly, for the most general associative memory, each pair of bit lines must be terminated in a combination driver-sense amplifier which can be switched between "drive" and "sense" in accordance with the specification for that bit in the interrogation word. Circuits developed for this purpose will be described later.

When the drivers and sense amplifiers are set up corresponding to the interrogation word given, the selected word line assumes a relatively positive voltage while all others remain nearer to ground potential. The pattern of sensed voltages or currents corresponds to the pattern of diode connections for the selected word, so that all the other bits in the word answering the description given are read out simultaneously.

MULTIPLE-MATCH READOUT

More generally, more than one word is selected by a given specification and all must be read out in some ordered fashion. This problem is common to all physical realizations of associative memories. There are, broadly, two solutions to the problem. One involves incorporating in the memory array, appropriate circuits to allow for sequential activation and readout of selected words. The other involves manipulation of the interrogation word, outside of the array, in such a manner that all selected words are isolated and read out in sequence. This latter method has proven very well suited for use with the diode matrix. An algorithm has been developed⁶ which requires no modifications of the basic memory array and yet retrieves all selected words in less than two memory cycles per word. This is true, independent of the total number of words stored in the file and independent of the number of bits per word.

The interrogation algorithm relies on the fact that *two* columns per bit are available for sensing. If the memory is driven so that only unique selections occur, only one column per bit need be sensed, since the output signals of any column-pair will always be complementary (i.e., 0, 1 for a "0" stored; 1, 0 for a "1"

stored). The first use of sensing both columns of a bit is simply to detect when *no* word stored answers the description given. If there are no words selected, all rows are clamped to ground. Thus, a 0, 0 detected at *any* sensed column-pair gives this indication immediately. If a multiple-selection is made, as is usually the case, more than one row assumes a relatively positive voltage. If all words selected (isolated) have the same bit in a given position being sensed, the sense signals for that bit are similar to those detected for a unique selection of one of these words. One can say that the sense signals are "reinforced" or stronger in the multiple-selection case. More often, however, some of the words selected have a "1" stored in a particular sensed position, while the others have a "0" stored there. In this case, *both* columns of that bit are driven positive, or carry a positive sense current (i.e., 1, 1 detected), since each is coupled through at least one diode to a selected row. One can say that an "x" has been sensed in this case.

The ability to detect the above conditions, coupled with the fact that any bit can be either driven or sensed, allows one to efficiently retrieve all words selected. Combination driver-sense amplifiers, controlled by external logic inputs, are used. The interrogation routine is based on the fact that, as one converts sensed-"x" bits to driven bits, smaller sets of words are selected. In this manner, we have, with appropriate external logic, made successive interrogations converting sense amplifiers (sensing "x") to drivers and drivers to sense amplifiers so that all words originally selected are isolated and read out individually. The interrogation sequence is generated based on a set of rules by which the interrogation pattern for a given cycle depends on the pattern and the sensed results of the previous cycle. One effectively generates a "decision tree" in this manner.

This algorithm is described in detail in the paper⁶ referred to earlier. Included in the paper is a detailed flow chart for generating the interrogation sequence, a comparison of this routine with other published work dealing with the same problem, a complete per-digit logic design for mechanizing the routine and a proof that retrieval of m words always takes exactly $2m-1$ memory cycles, independent of the number of

words in the memory or the number of bits per word. Since the paper deals primarily with the logic of the routine, applicable to any physical realization which allows "column-pair sensing" and simultaneous activation of all selected word lines, no specific mention is made of fixed memories or diode matrices. (A cryogenic implementation is described only as an example.)

One point to note is that, while some physical realizations would require a word-driver per word to achieve simultaneous activation of all selected (or "matched") word lines, the diode array described above *automatically* furnishes this without the need of word-drivers. (I.e., every selected row develops a positive voltage which *directly* couples to sensed columns via its diode pattern.) This is a fundamental reason why the algorithm is particularly well-suited for a fixed memory configuration of the type discussed above.

EVAPORATED DIODE ARRAYS

A large diode matrix serving as a fixed, associative memory is economically feasible only if sizeable arrays of diodes can be fabricated at sufficiently low cost. A new technique for constructing integrated arrays of thin-film diodes has recently been described.⁵ It embodies vacuum evaporation of an organic semiconductor, copper phthalocyanine. Diodes fabricated by this technique were used experimentally to implement the associative memory concept considered here.

A multiple organic diode card is shown in Fig. 2. Each $4'' \times 4'' \times .020''$ board holds 128 diodes which are distributed around the outline of the dark phthalocyanine inner square. All diodes have a common cathode, connection to which is made at any corner of the card. (Diode polarities for all of the experiments described are the reverse of those given in Fig. 1.) The card shown can be used to store one 128-bit word, with the common cathode conductor being a row wire of the matrix. A set of n such cards, completely interconnected, comprises an n -word, 128-bit-per-word, memory. Two etched wires per diode form the anode connection, "fanning out" to the card edge. These allow connection of a given diode anode to both of its associated column wires. Information can be written in

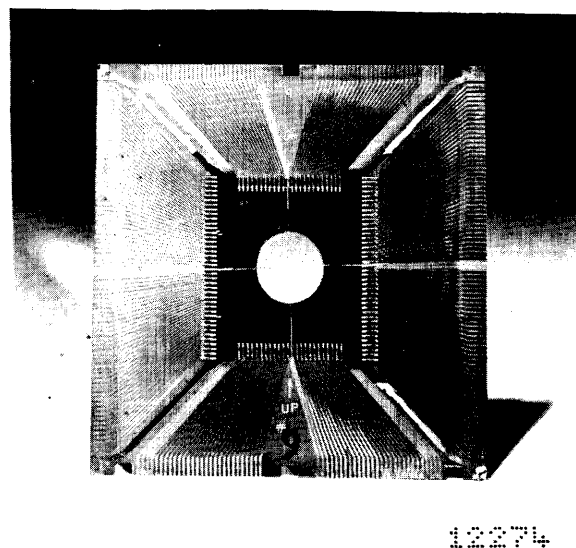


Figure 2. Evaporated Organic Diode Card.

by breaking the appropriate anode connections in any of a number of ways such as, for example, by punching a series of small holes in the card. The card pattern shown was chosen to allow a relatively small area for the evaporation of the diodes, in order to insure the desired uniformity of characteristics.

The static characteristic of a typical evaporated thin-film diode is shown in Fig. 3. With a diode area of 3.5 mm^2 , the voltage drop is approximately 1.5 volts at a forward current of 2 ma. Its rectification ratio is approximately 10^5 .

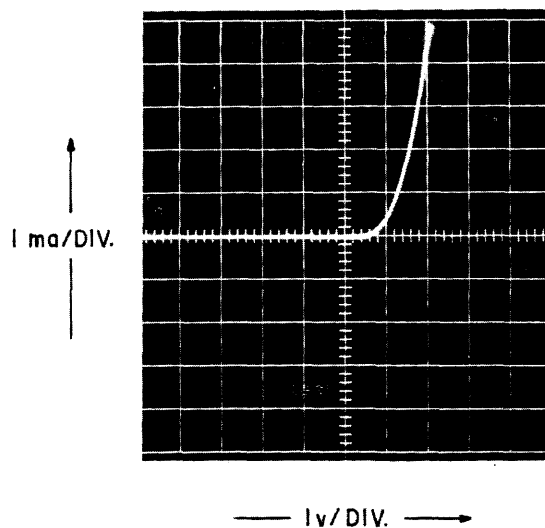


Figure 3. Copper Phthalocyanine Diode Characteristic.

Each diode consists of a three-layer sandwich, the middle layer being copper phthalocyanine and the outer layers being metal anode and cathode electrodes. Since the diode is such a thin element, its equivalent parallel plate or "case" capacity is large, being typically, for the area given above, approximately 50 pf.

EXPERIMENTS

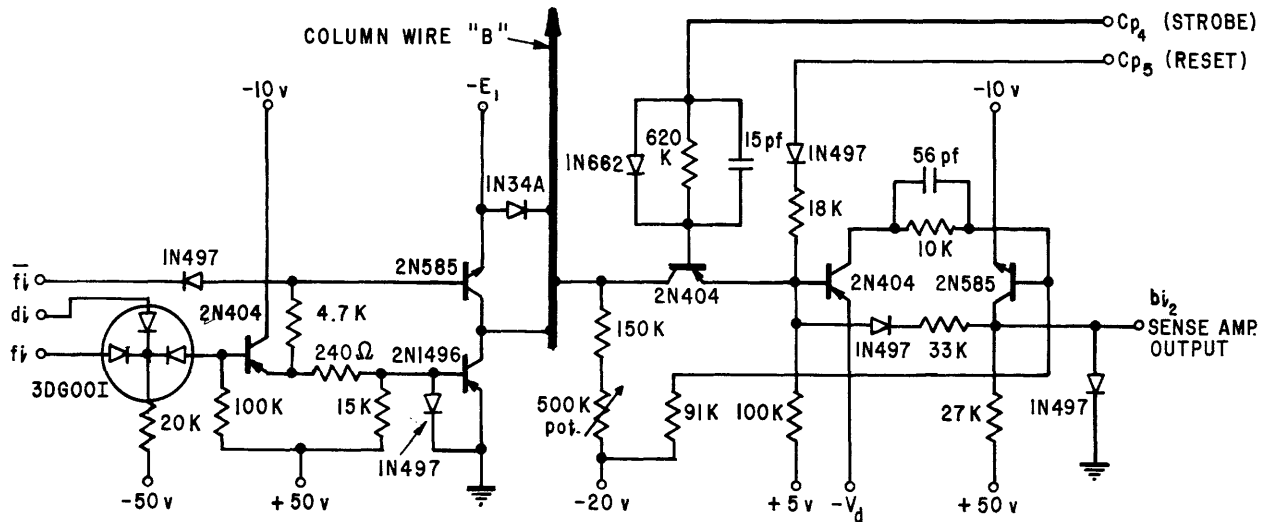
a) Peripheral Electronics

The circuit design of the peripheral electronics system which was constructed to exercise and test various embodiments of the diode associative memory was largely conventional (primarily using RCA 2N404 transistors). The apparatus consists of all the logic and the combination driver-sense amplifiers for implementing the search routine⁶ for a memory word length of 10 bits. Display of retrieved words, memory cycle count and driven or sensed states, for each bit, are included.

The requirement of a combination driver-sense amplifier controlled by external logic inputs, resulted in a somewhat novel design. A schematic diagram of the circuit is indicated in Fig. 4. When in the "drive" state, it can furnish the memory with up to 0.5 amps at ground potential. This would allow the circuit to drive a 1000 word (100 bit per word) diode associative array. It is also capable of detecting 10 μ a of signal current when in the "sense" state and strobed (CP_4 is the strobe pulse). The circuit will switch between "drive" and "sense", as demanded by the input signal f_i , in 0.5 microseconds. The function table shown in the figure relates the circuit state (drive or sense) to the logic input states. Two such circuits are required per column pair.

b) 500-Bit Diode Matrix

A small, conventional-diode array, constructed as a 50 word, 10 bit-per-word manually-alterable memory, served as initial experimental



DRIVER-SENSE AMPLIFIER FUNCTION TABLE, COLUMN "B"

f_i	$\bar{f}_i$	d_i	FUNCTION
0 v	-10 v	0 v	} SENSE DURING STROBE PULSE DRIVER PRESENTS A HIGH IMPEDANCE
0 v	-10 v	-10 v	
-10 v	0 v	0 v	DRIVE "0"
-10 v	0 v	-10 v	DRIVE "1"

NOTE :- COLUMN "A" DRIVER-SENSE AMPLIFIER IS IDENTICAL BUT WITH $\bar{d}_i$ REPLACING d_i . THIS PROVIDES THE REQUIRED COMPLEMENTARY DRIVE.

Figure 4. Driver-Sense Amplifier Circuit.

verification of the basic idea of a diode associative memory and of the electronic mechanization of the interrogation routine. Various patterns of information were written into the array by manually changing the pattern of diode connections.

A number of tests were made with this matrix. These include the lexicographic ordering of the entire memory contents and a large number of searches using a wide variety of input descriptor patterns. (Descriptors are inserted using a bank of toggle switches.) For each test series, the interrogation routine can be manually stopped along and monitored or can proceed automatically at a maximum rate of 100 kc (10 microsecond cycle time). The total number of cycles required for each retrieval was monitored by a counter and could be compared with the predicted count.

c) Organic Diode Array

Fig. 5 is a photograph of a stack of organic diode cards, each of the type shown in Fig. 2, which was successfully operated as a small test memory. Although each board contained 128 diodes, only 10 bits on each card were used for the tests because of the limited amount of peripheral electronics which was then available.

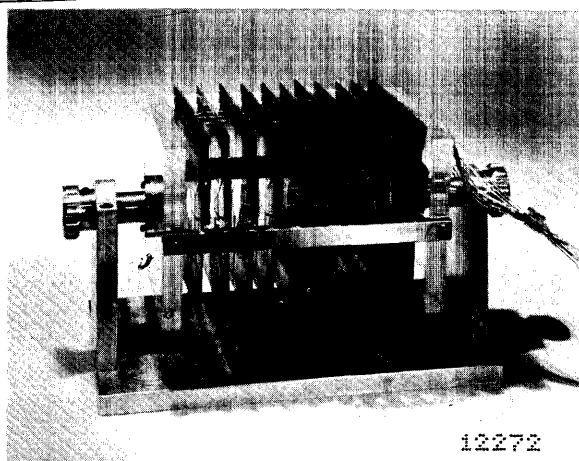


Figure 5. Organic Diode Test Memory Stack.

The diode cards are mounted in a metal frame with specially-designed "finger" connectors used for each card. Column wires running down the outside of the card stack are soldered to the finger connectors and provide the required card-to-card interconnection. The information stored is determined by the pattern of connections to these column wires. This allowed one to change the information stored without removing the cards and was convenient for the tests made.

Various search and retrieval tests were performed with the organic diode memory. In general, the experiments duplicated those performed with the conventional diode matrix. They demonstrated the feasibility of using thin-film organic diode arrays as digital elements.

CONCLUSIONS

The purpose of this paper has been to explain the associative properties of a symmetrical diode matrix, including the applicability of a very efficient interrogation algorithm to resolve multiple-matches, and to describe experiments which verify these concepts and which, in addition, utilize arrays of new thin-film diodes. Clearly, the physical realization of this type of diode matrix can be in many forms and may well involve other diode array fabrication technologies, including those now developing in the semiconductor industry.

ACKNOWLEDGEMENTS

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