DESIGN CONSIDERATIONS FOR A 25-NANOSECOND TUNNEL DIODE MEMORY

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INTRODUCTION

About two years ago a tunnel diode memory system was described which employed substantially different techniques than those previously used.[1] Although earlier systems had tended towards array arrangements that had the storage cells connected in parallel on one or more axes, the new system employed series connections along two axes. This new arrangement has several design and performance advantages compared to previous systems. The original paper described the basic approach and some of the earlier work which included the design of array cross sections and the associated driving and sensing circuits. Since that time one version of the system has been operational in two IBM 7030 systems,[2] and a 16-word, fully-populated, higher-speed laboratory model was built and reported.[3] The present paper describes the engineering considerations used in the design of a larger and faster memory employing the basic techniques.

The new memory system contains 64 words of 48 bits each, and test results from a partially-populated cross-sectional model indicate a complete READ/RESTORE or a CLEAR/WRITE cycle time of less then 25 nanoseconds. A fully-populated complete memory system is in the final stages of construction and assembly.

CELL OPERATION

The basic storage cell is simple, as shown in the dashed-line box in Fig. 1. It consists of a tunnel diode shunted by a series-connected load resistor and the secondary winding of a transformer. A biasing current is introduced to the tunnel diode

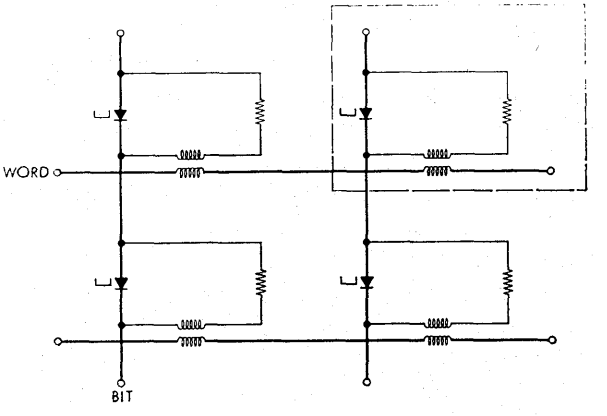


Figure 1. Array configuration.

storage cell along the bit axis. During the writing portion of a memory cycle, the biasing current can be increased by the addition of a bit current. The word driver introduces voltage excursions within the storage cell loop by means of the transformer. The normal bias current through the tunnel diode cell is such that the tunnel diode can be either in a high-voltage region or in a low-voltage region.

The cells are series-connected along two axes (Fig. 1) in order to form the basic memory array configuration. Figure 2 shows the load-line diagram for the basic storage cell. The current bias and the load resistor are such that the cell normally has two stable states. During the READ operation, if the cell has been storing a ONE, the voltage induced into the secondary winding of the cell transformer

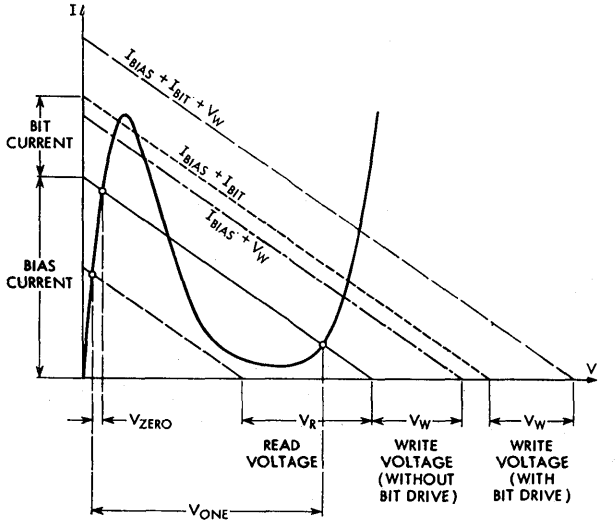


Figure 2. Tunnel diode load-line diagram.

shifts the load-line and clears the cell from the high-voltage state to the low-voltage state. The net voltage drop when the cell changes its operating point from the high-voltage to the low-voltage state is transmitted through the series connection of the diodes on the bit line to the end of the bit line, where it can be detected.

On the other hand, if the cell was storing a ZERO, it initially would be in the low-voltage state. The shifting of the load line in this case by the READ voltage, V_r, produces only a very small voltage as the ZERO response. At the conclusion of the READ cycle, all the cells associated with the particular word will have had their information read out and will be left in the low-voltage state.

ARRAY DESIGN CONSIDERATIONS

One of the key items in the design of the system is the cell transformer. The objectives are to achieve a low impedance when looking into the primary loops, and to have reasonable inductive coupling but a minimum of capacitive coupling from primary to the secondary loop. In the earliest work, etched circuit construction was tried but the state-of-the-art of fine-line etching and the difficulty of making good minature connections made the approach impractical at that time. The succeeding systems employed transformers with secondary windings made of wire. When the work on this new system was started, it was decided to again attempt to solve the various problems of the etched circuit transformer for the inherent advantages of reproducibility it offered.

The first step in the design process was to study electric field patterns of likely configurations using resistance paper analog techniques. From this work, reasonably accurate predictions of the transformer parameters such as mutual coupling and secondary self-inductance were made. This procedure permitted a quick review and optimization of different transformer patterns. A typical field plot used is shown in Fig. 3. As a result of this work, preliminary decisions were made as to the desired shape and dimensions of the transformer.

At this time different constructional methods and arrangements of the storage cell into arrays were considered from both a mechanical and electrical viewpoint. It was finally decided that an approach which had several cells on a module would simplify manufacturing problems and improve serviceability. Although it offered certain mechanical constraints, the SLT (Solid Logic Technology) type of module employed by IBM was chosen as a starting point for the design.

An alumina ceramic wafer about one-half-inch square serves as the main mechanical structure for the module. The ceremic wafer has 16 swaged pins on 0.125-inch centers for external connections plus 6 pins in the opposite direction to serve as mounting points for welding the tunnel diodes. One surface of the ceramic has 4 screened resistors and a solder-coated circuit pattern. A view of this subassembly is shown in Fig. 4. The transformers are contained in a separate multilayer etched copper wafer assembly that is slipped over the 16 pins and dip-soldered. The final assembly operation con-

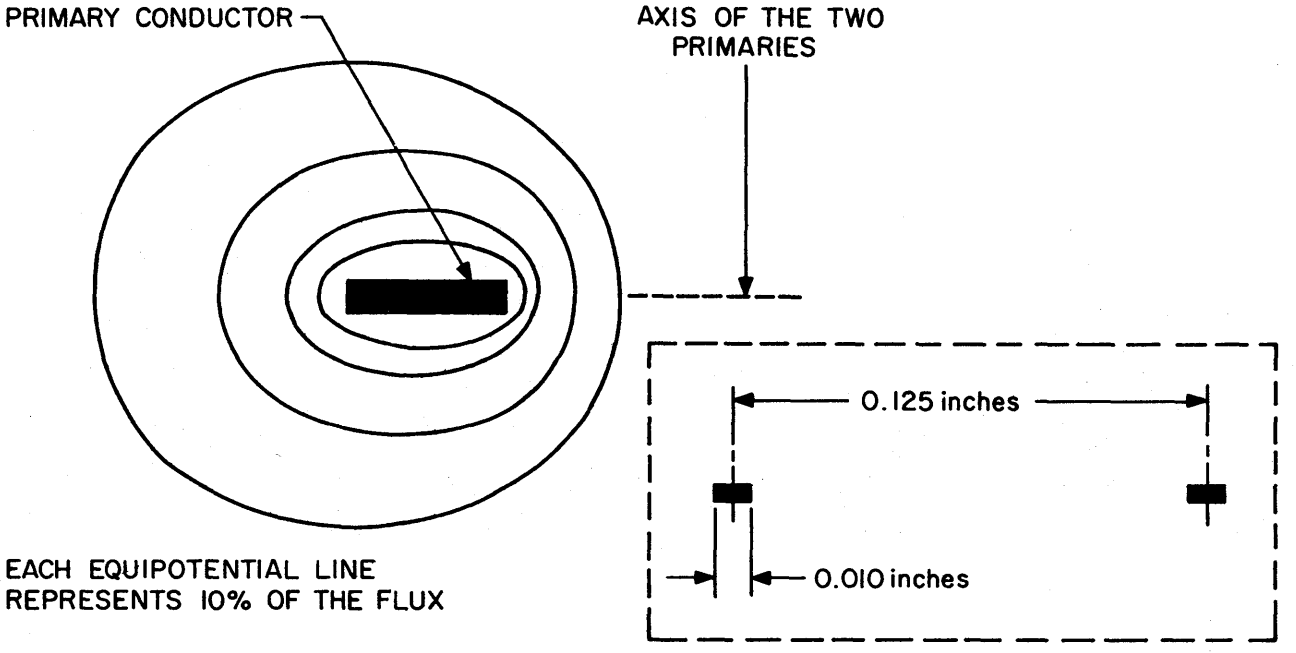


Figure 3. Magnetic field pattern around primary conductor.

sists of applying a ferrite powder coating in an organic binder on the primary side of the transformer wafer to increase the mutual coupling from primary to secondary. The assembled modules are shown in Fig. 5.

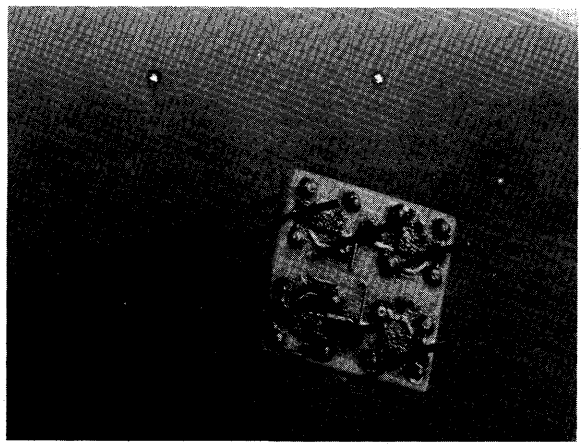
Early in the project, it was recognized that a large, accurately scaled mockup of the module assembly was needed for making electrical measurements. These measurements were needed to assist in the transformer design, and were also vital to the determination of the overall array parameters. The normal-size modules were so small that it was virtually impossible to make electrical measurements with any degree of accuracy of precision. Because both capacitance and inductance scale are directly proportional to linear dimensions, it was decided to make a module assembly 20 times normal size. One problem was to find a suitable dielectric material substitute for the ceramic substrate because large ceramic pieces were not available. The solution was found by loading an epxy resin mixture with titanium dioxide powder in a ratio of approximately 1:1 by weight to achieve a dielectric constant of 9.4. Analog field plots showed that thick copper wiring patterns could be simulated by using two thinner patterns appropriately spaced and connected in parallel. Figure 6 shows photographs of the large module and some of the transformer patterns.

The final transformer patterns are shown in Fig. 7. The solid squares are lands used for connecting points. To cancel capacitive coupling effects from the primary to the secondary wiring, each transformer uses two primary wires which are driven push-pull with respect to ground. The primary wires are routed in a manner to maximize the mutual coupling to the secondary wires, and the secondary wires are arranged in a mirror image configuration to match the land pattern to obtain uniform characteristics. Capacitance stub "fingers" are included to balance the capacitances between the primary lands and the secondary windings.

A cross section of a transformer wafer is shown in Fig. 8. To minimize the capacitance, the primary and the secondary wires are separated by Teflon® (registered trademark of E. I. Du Pont de Nemours and Co.). The outer layers are used as supports for a land pattern for soldering to the pins, and also to protect the transformer pattern. Through-hole plating techniques are used to connect the inner land patterns with the outer lands.

BIT-LINE CHARACTERISTICS

The bit line used in the tunnel diode memory consists essentially of a number of tunnel diodes connected in series. The inductance of the interconnections is the series inductance of the line, whereas the transformer and module capacitance is the major component of the shunt capacitance. However, the tunnel diodes add a nonlinear series



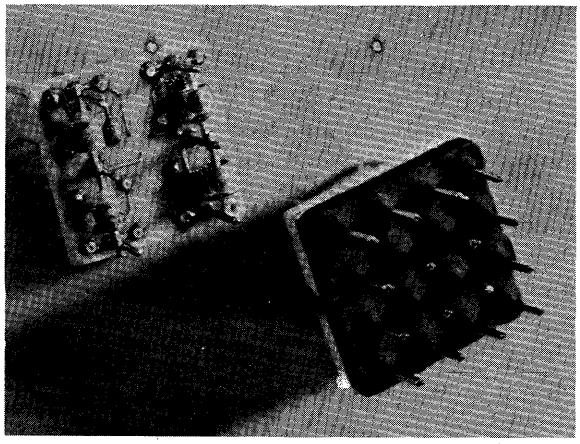


Figure 4. Array modules: (*a*) module with resistors and pins; (*b*) top and bottom views of array modules.

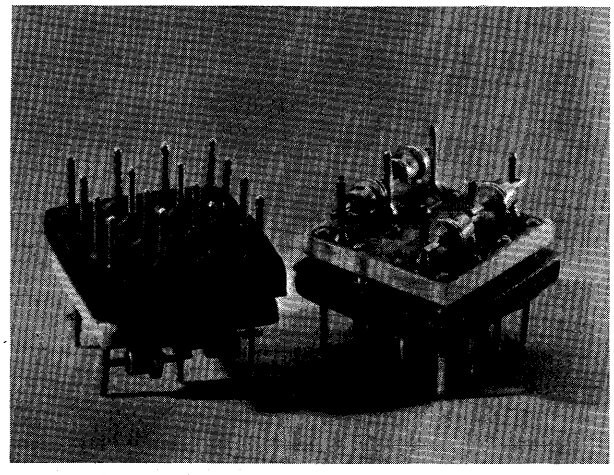
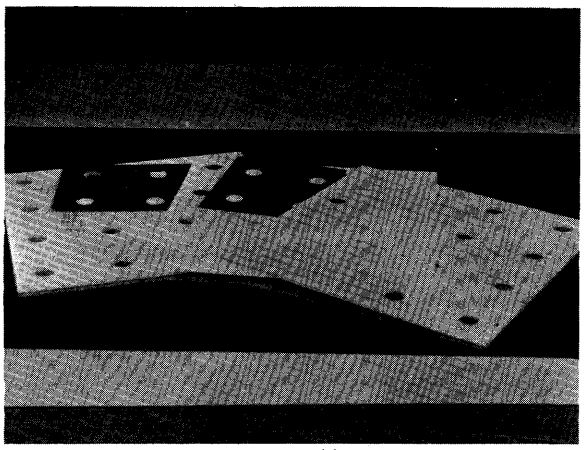


Figure 5. Assembled memory array modules.



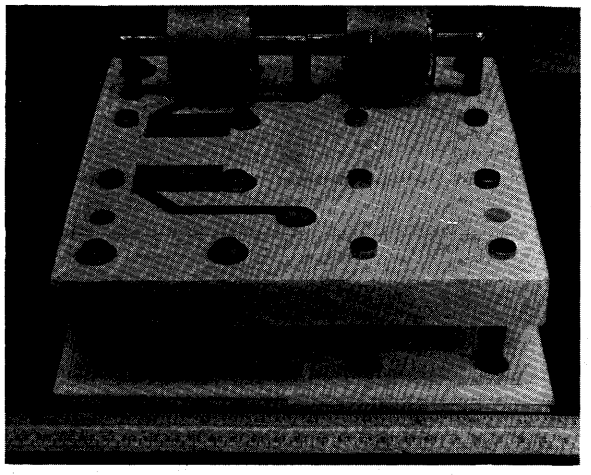


Figure 6. (*a*) Transformer wafer sheets, 20 times normal size; (*b*) memory module, 20 times normal size.

resistance component that predominantly affects the response of the line. An equivalent circuit for the line is shown in Fig. 9 where each section represents one bit of the line. L_S is the series inductance; C_d is the diode junction capacitance; R_d is the nonlinear diode resistance; and C_S is the total shunt capacitance. Because each of these parameters is very small and the current rise times desired are very fast, accurate measurements necessary to optimize the line design could not be made.

A program was written to calculate the response of the bit line that utilized this equivalent circuit and took the nonlinearities of the tunnel diode characteristics into account. By using this program, the

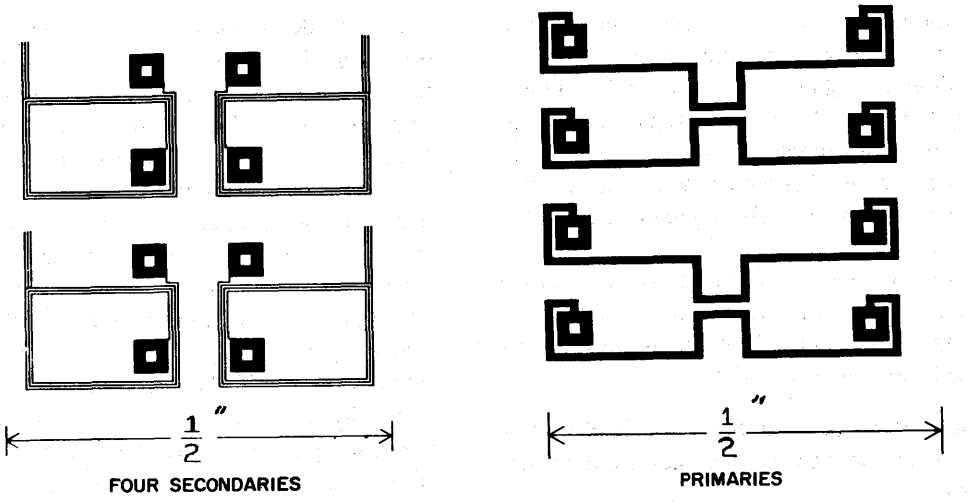


Figure 7. Transformer pattern.

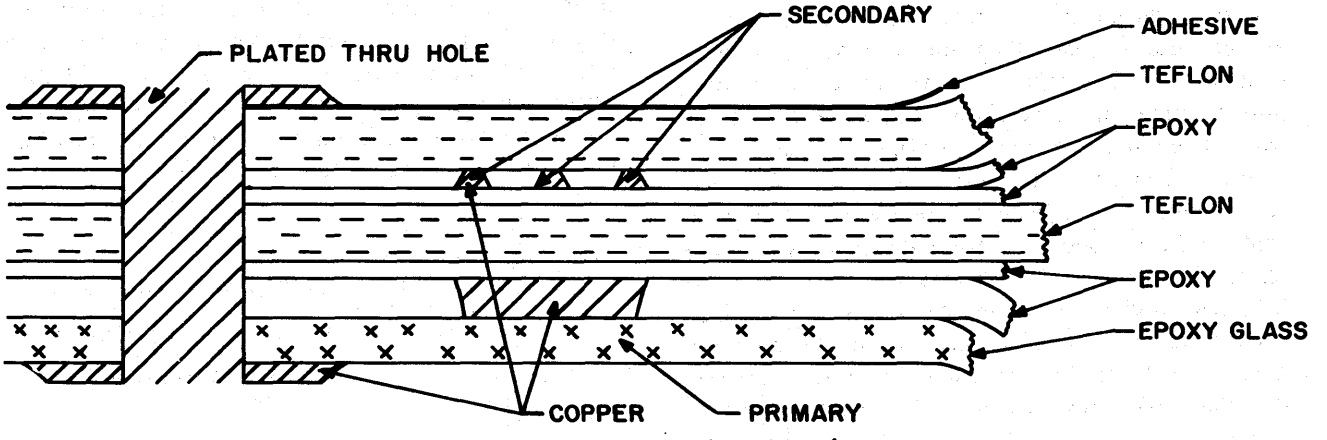


Figure 8. Transformer wafer cross section.

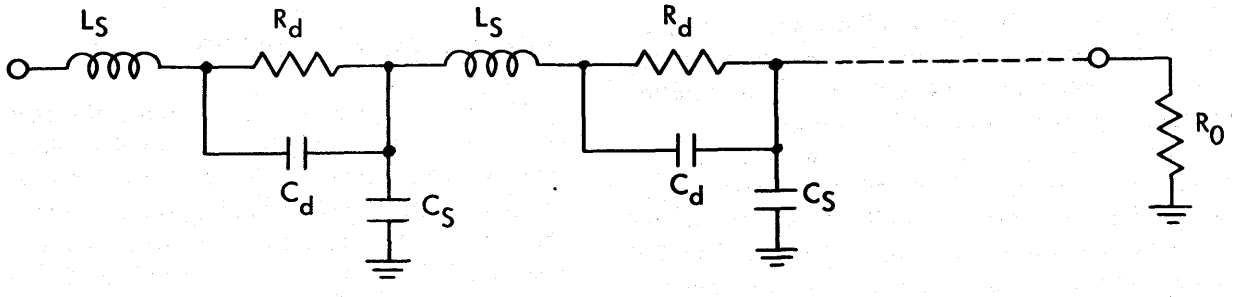


Figure 9. Bit-line equivalent circuit.

parameters of the line were varied to find their effect on the response and to find an optimum termination. The range of parameters used was determined by measurements of the 20-times module model. The results of the investigation led to the following conclusions:

- Increasing the series inductance of the line does not improve the response of the line; that is, in spite of the fact that the line becomes less lossy as the series inductance is increased, the sum of the rise time plus the delay time increases with increasing inductance.
- The parameters that most strongly affect the response of the line are the diode resistance, the shunt capacitance, and the termination resistance, in this order.

- The optimum termination resistance, chosen with the criterion of minimum rise time with negligible overshoot, is considerably below the $\sqrt{L/C}$ for the line. Reflections due to this lower terminating resistance tend to increase the bit drive current at the far end of the array and thereby compensate for the attenuation.
- Because of the nonlinearity of the diode resistance, the fastest response times are obtained when the bit drive is toward increased current in the diode.

Actual measurements verified these predictions but could not provide the accurate resolution obtained in calculations.

Two types of crosstalk were investigated. One was the inducement of a false sense signal on a bit line because of a switching tunnel diode on an adjacent bit line. The other type was accidental writing into a tunnel diode receiving full word current by way of mutual inductive coupling between transformer secondaries. The primary source of a false sense signal is the capacitance between cells on adjacent bit lines; these transformers are only 50 mils apart. The value of the capacitance predicted by the 20-times module (0.31 picofarad) is slightly high because no ground plane was used in the measurement. In order to find the worst case, it was assumed that the capacitance of eight cells are all lumped together at a point and that the voltage rises in one L/R time constant. Under these conditions, it is predicted that a maximum of 96 millivolts would be produced from the two adjacent bit lines. However, the actual noise should be much smaller and the detector rejection level is safely above 96 millivolts.

Calculations were made of the worst-case noise current induced by mutual inductive coupling between adjacent transformer coils. They showed that the peak induced current would be less than 2.5 percent of the diode peak current. This value is small enough to have a negligible effect on operating tolerances.

WORD LINE STUDY

The ferrite material on the primary winding of the transformer increases the characteristic impedance and delay of the line compared to a similar line without the ferrite. In addition, the ferrite increases the high-frequency losses and results in rise-time deterioration as the word pulse travels down the line. To maintain a reasonable variation in rise time, the word lines are split into 24-bit segments, with 2 segments being driven by the 2 output stages of a word-driver circuit.

A number of methods of maintaining independence of the secondary output current from primary current rise-time variations were investigated. These involved shorting the word line or inserting a rise-time pad in the output of the word-driver circuit. An investigation of the response of the transformer itself showed that secondary inductance and load resistance caused it to act as a reasonable rise-time pad to a fast word-drive pulse. Fig. 10 shows the method of drive presently employed. The line is terminated in its characteristic impedance, and the pulse is clamped at the driver to control the pulse amplitude. The transformer secondary circuit is used as a rise-time pad, with the result that a 20 percent change in the primary current rise time result in only a 10 percent change in the secondary output voltage amplitude.

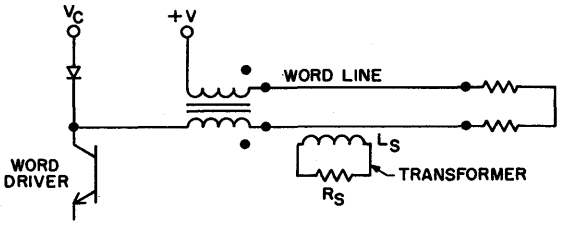


Figure 10. Word drive system.

ARRAY CHARACTERISTICS

The array is formed by mounting the memory cell modules on a pluggable card which contains the interconnection pattern. The card has etched wiring on the two outer surfaces and a ground plane inside the laminate In addition to the memory cell modules, the array card also contains all the word-driver circuits, word line termination networks, bit line termination networks, and miscellaneous power supply decoupling networks associated with the modules. Each card contains 8 words, 48 bits per word, of storage. An assembled array card is shown in Fig. 11.

One of the advantages of the series-type array is that the driving requirements are readily met with high-speed transistors. The array described utilizes a unidirectional current pulse of 88 milliamps into the word line and presents a load of

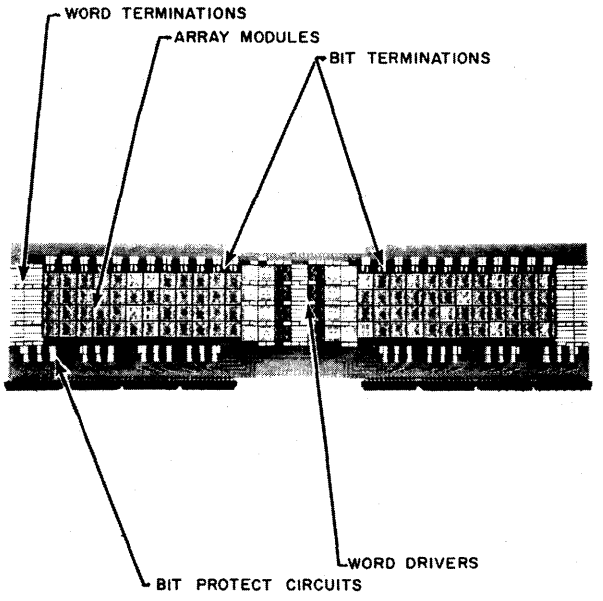


Figure 11. Array card layout.

136 ohms to the word driver. As previously explained, each word line is split into 24-bit segments, with a pair of segments driven by one word-driver circuit. The propagation delay from the word line input terminals to the far end of each line is about 3 nanoseconds. In contrast to the word line, the bit line is much more like a distributed RC-line than a conventional low-loss transmission line and, therefore, exhibits high phase and frequency distortion. To minimize delay, the bit line is broken into 8-bit segments, with a pair of segments handled by each information control (regeneration) circuit. The bit drive required is only 8.27 milliamps and is also a unidirectional pulse into a load impedance of about 50 ohms. Output signals for sensing are in the range of 300 to 400 millivolts, although the detector sensing level is usually set lower to save cycle time. The maximum quiescent power dissipated in a memory cell is 4.5 milliwatts which leads to an overall maximum standby power dissipation in the 64 by 48 array (exclusive of associated circuits) of about 14 watts.

CIRCUIT DESIGN

Information Control Circuit

Figure 12 shows the information control circuit diagram. The sense amplifier, detector, information control logic, bit-line bias current, and bit driver were included in this single circuit to shorten regeneration time and to simplify the circuitry.

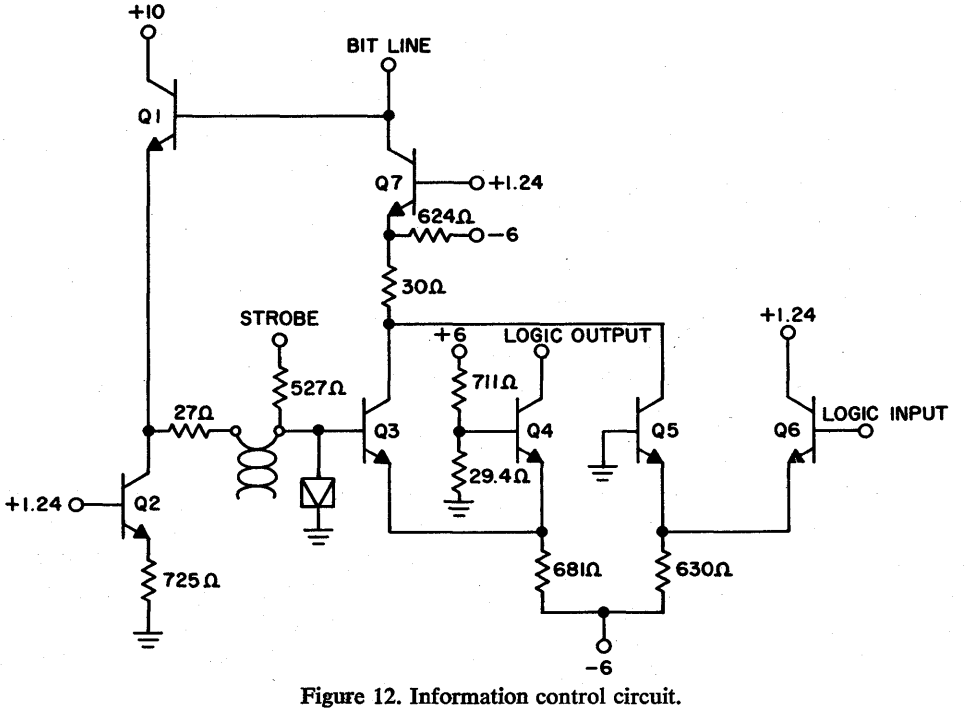


Figure 12. Information control circuit.

The operation of the circuit is as follows: The first transistor, Q_1, connected as an emitter follower, receives a sense signal at its base and drives a transmission line that is open-circuited at the far end.

This passes a pulse of a width of approximately 3 nanoseconds. If the strobe input is positive at this time, the tunnel diode switches on the first 200 millivolts of the signal. The detector diode remains in the high state as long as the strobe pulse is present. This drives the current switch ($Q_3 + Q_4$) that supplies the bit current pulse to the bit line. The bit drive may also be actuated by pulsing the logic input terminal negatively (Q_6). The bit-driver collector current increase of the output transistor rises in 2 nanoseconds or less, and the entire line assumes the full drive amplitude within 7 nanoseconds of bit-driver turn-on. No overshoot has been observed. In addition to furnishing the bit pulse, the output transistor also supplies the DC biasing current for the bit line. Throughput time of the ICC (Information Control Circuit) from sense-amplifier input to bit-driver turn-on is 2 to 3 nanoseconds. The total time elapsed from the resetting of the tunnel diode to its zero state until the restoration of that diode to its ONE state is 10 to 11 nanoseconds. During the write noise, the first transistor cuts off, thereby preventing the write noise from influencing the state of the tunnel diode detector.

WORD DRIVER

The word driver circuit is shown in Fig. 13. The operation of the circuit is as follows: The current switch formed by Q_1, Q_2, and Q_3 performs the logical AND function and provides regenerative feedback through C_1 to improve the rise time of the input pulse; Q_4 provides the necessary current gain to drive

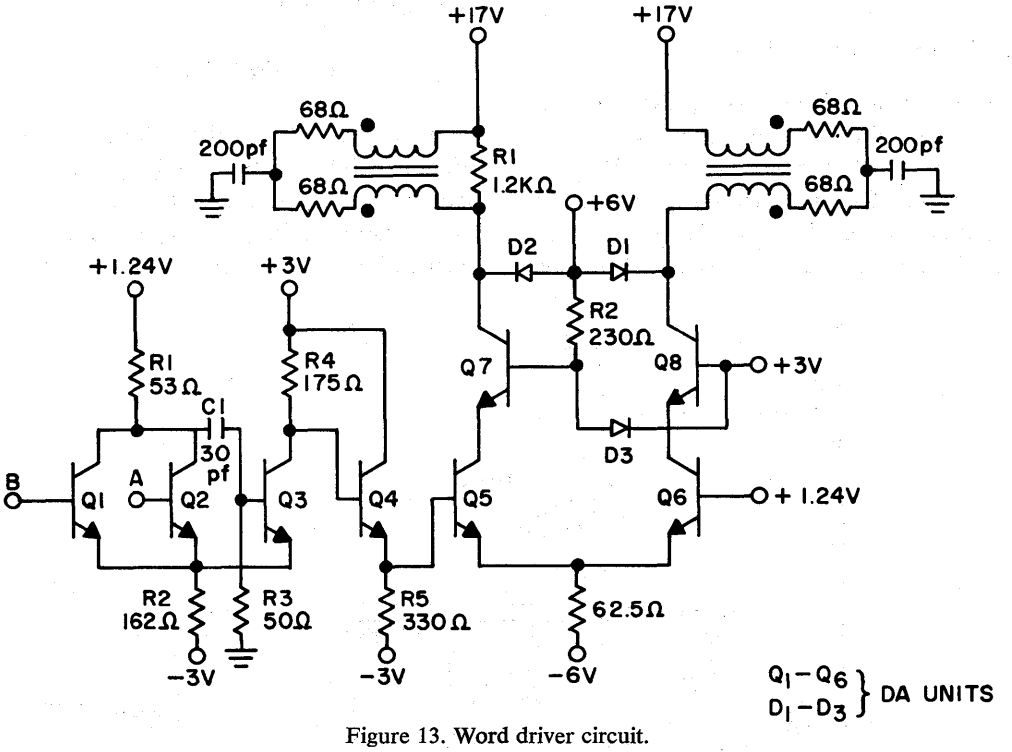
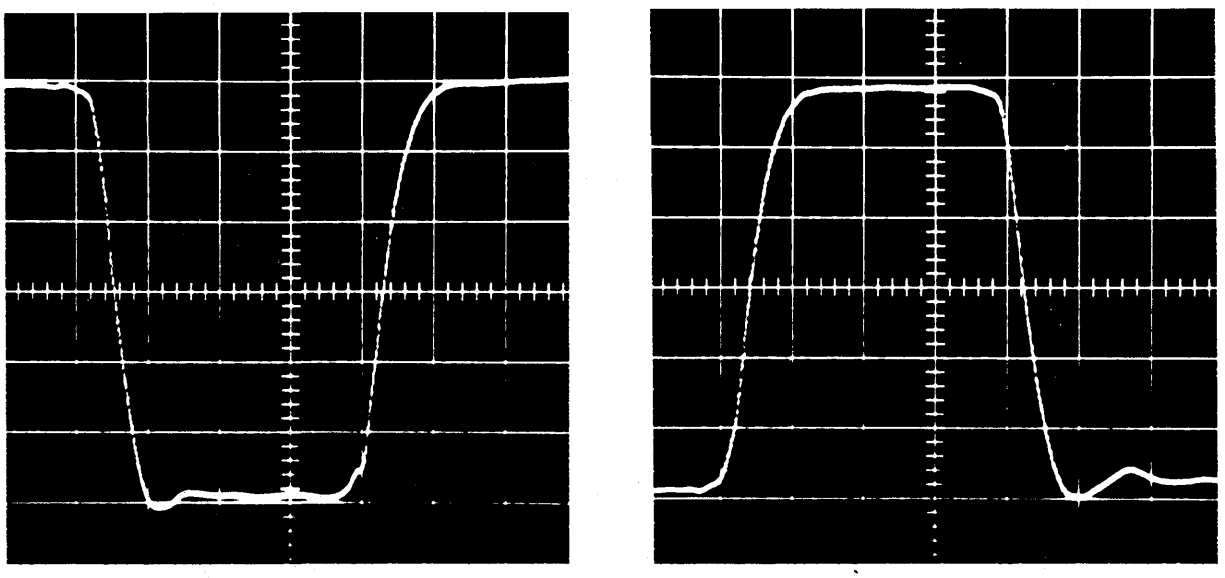


Figure 13. Word driver circuit.

the output stages. In this circuit, both outputs from the current switch are utilized to drive the word line in two segments. The output stage consists of the current switch formed by Q_5 and Q_6, which drives two 2N2369A ($Q_7 + Q_8$) transistors for increased voltage gain. The output levels are clamped by the diodes D_1 and D_2 to provide a well-controlled output level. The two wires of each word line segment are driven push-pull with respect to ground by a balun transformer. Because of the relatively light drive power requirements, high-speed current switch techniques can be used. It should be noted that half the drive is left ON all the time because only the changes in drive line current can activate the tunnel diode cells through the transformers.

The word driver produces an output pulse of 88 milliamps into a 136-ohm load. The current amplitude stays within a tolerance of ± 10 percent under worst-case conditions. The rise and fall times of the pulse are nominally 3 nanoseconds, 10 to 90 percent.

The worst-case tolerance on the write transition is within ±15 percent of nominal value and the read transition is at least as fast. The waveforms of the two outputs of the word driver are shown in Fig. 14.



a. In phase output.

b. Out of phase output.

(Horizontal = 5 ns/div and vertical = 2v/div. R_L = 136 ohms.)

Figure 14. Final word driver output waveforms.

OVERALL SYSTEM DESCRIPTION

In addition to the memory array and the associated driving and sensing circuits, the complete system includes a binary address register with decoding circuits, data input gating circuits, a data output register, and a clock with timing pulse distribution circuits. An address counter, comparing circuits, and manual data input switches permit exercising the memory system without using any external connections. Either the internal clock, or an external source of clock pulses may be used. The logic circuits are constructed of an advanced form of IBM solid logic technology, referred to as ACPX in papers presented previously.[4,5]

The system interwiring and voltage distribution is contained in 2 multiple-layer boards, each about 10 by 14 inches, mounted side by side. These boards have male pins protruding from them which serve as connecting points for external wiring and also receive the sockets mounted on the bottom of each circuit card. The memory array cards are about 18 inches long and plug into both board assemblies, bridging across the gap between them. Except for one narrower card, all the other circuit cards are about 3 inches wide and 5 inches high. About two-thirds of the volume is used by the memory array and the information control circuits; the remainder is used by the various logic circuits. A sketch of the layout is shown in Fig. 15. The card and board assemblies, blower system, power supplies, control panel, and I/O connection panel are contained in a cabinet.

Tests on a cross-sectional model containing 2 populated word lines and 4 populated bit lines indicated good operating margins with a cycle time in the range of 22 to 24 nanoseconds. Assembled array cards, shown in Fig. 11, have also been tested, with excellent operating margins verifying the validity of the cross-section test data. Fig. 16 shows the actual voltage waveforms from the cross-section model. At the time this is being written, the complete system is under construction; a photograph of the partially completed system is shown in Fig. 17.

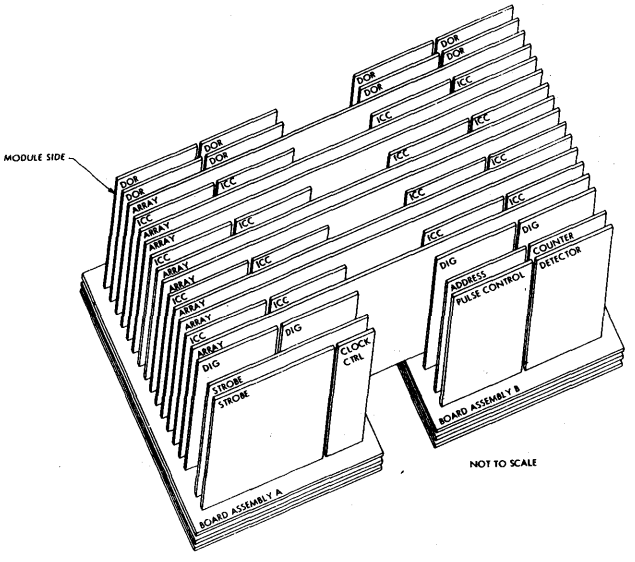


Figure 15. System layout sketch.

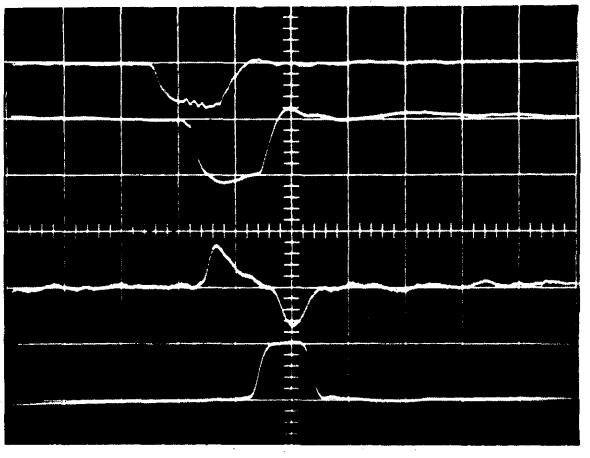


Figure 16. Cross-sectional model memory circuit timing waveforms (10ns/cm). The traces from top to bottom are as follows: (*1*) Input to word driver. (*2*) Driven end of word line. (*3*) Transformer output of the cell at the far end of the word line. (*4*) ICC output.

This represents the first complete memory system using any type of technology reported in this size and speed range.

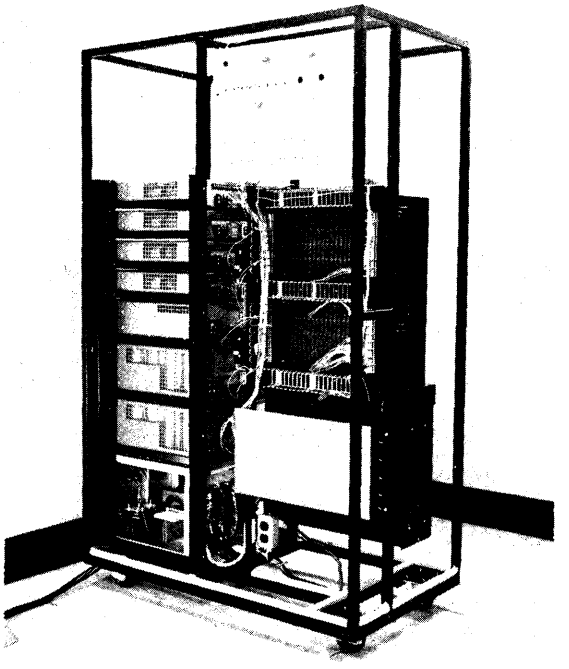


Figure 17. Partially assembled memory system.

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