A high-speed thin-film memory: Its design and development

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INTRODUCTION

Memories in today's high-performance systems are typically made up of memory modules of capacity comparable to the new memory to be described here. Cycle times are 500 nsec to 1 μsec with access times of 300 to 500 nsec. This paper presents the design of a thin-film main memory with a capacity of 8,192 words of 72 bits each. The cycle time of this memory is 120 nsec with an access time of 60 nsec. Thus, this memory design represents a 4-to-8-times improvement in main memory performance over the present state of the art.

The first section of the paper is a general description of the physical layout of the memory. The memory array is then discussed with particular emphasis on noise problems in the array. Finally, the memory circuits and packaging are described.

GENERAL SYSTEM DESCRIPTION

The memory layout is shown in Fig. 1. The approximate dimensions are 68″ high by 42″ deep by 7″ thick. The memory array consists of two 1,024-word by 288-bit assemblies which are driven and sensed in parallel. 72 of the 288 bits read in parallel are gated out. Each assembly contains 72 3″ × 3″ bit plates arranged in a back to back 6 × 6 configuration. The dimensions of each assembly are 20″ × 20″ × 4″. The drive and sense circuits and associated logic are packaged on cards mounted on multilayer boards which surround the array.

Array Design

The memory array is made up of copper bit plates on which the films are deposited, striplines of Mylar*

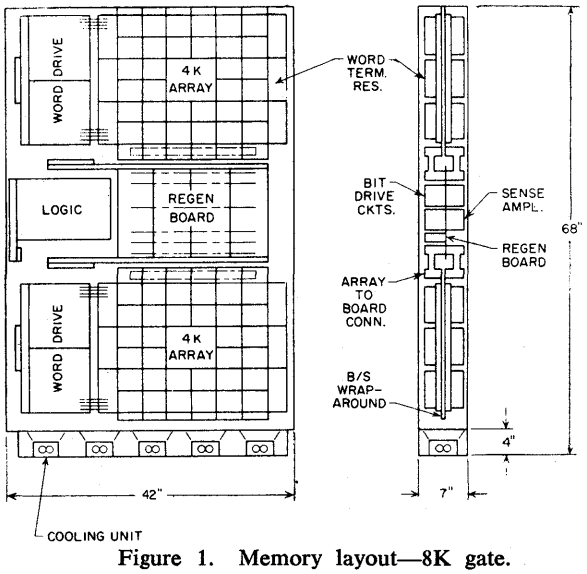

Figure 1. Memory layout—8K gate.

foils, and a ferrite keeper which partially closes the return flux path of the film memory elements around the striplines.

The thin-film elements utilized in this memory are 25 × 30 mil rectangles on 30 × 54 mil centers. The permalloy films are about 800 Å thick. They are switched in ~5 nsec by means of orthogonal drive fields produced by fast-rising current pulses in two sets of striplines. The word lines are closest to the film and are parallel to the easy axis of the film as shown in

*Mylar is a registered trademark of the E. I. du Pont de Nemours & Company.

Fig. 2. The bit lines are perpendicular to the word lines and separated from them by a thin dielectric foil. The sense line is parallel and coplanar with the bit line.

Registration of the striplines to the bit plates is achieved by mounting the striplines on rigid frames with appropriate mechanical registration fixtures. The line pattern is etched with the copper-Mylar laminate in tension, and a bit plate-stripline registration tolerance of ± 3 mils is maintained.

Array Noise Considerations

The signal energy from a thin-film memory array is low. In this memory the signal level is 4 millivolts, signal duration about 5 nsec, and the sense line impedance 50 ohms. At this signal level, array noise must be minimized if reliable memory operation is to be achieved. Noise results from unwanted energy coupling into the array at read time and at write time. The read noise results from capacitive coupling between the word line and the sense line. Since this noise is coincident with the signal, it directly affects memory operating margins. Write noise results primarily from coupling of energy from the bit line to the sense line. Since the sense system must recover from the write noise before the next read operation, the read-write cycle time is directly affected.

Read noise in an array in which all lines are terminated in their characteristic impedance is given by the following equation:

$$V_{rn} = \frac{C_{sw} Z_{ow} Z_{os}}{2} \times \frac{dIw}{dt}$$

where C_{sw} = the capacitance between word and sense lines,

Z_{ow} = the characteristic impedance of the word line,

Z_{os} = the characteristic impedance of the sense line, and

$\frac{dIw}{dt}$ = the rate of rise of the word line current.

This noise, unless canceled, is comparable to the signal level. First order cancellation is obtained by using a dummy sense line which runs between the bits on the bit plate. This is illustrated by Fig. 3. The outputs of the sense and dummy sense lines are sensed differentially using a balanced pulse transformer.

Since the bit and sense lines are closely spaced and long, the coupling between them gives rise to a large write noise (30 mv). The reactive component of write noise results from inductive and capacitive coupling between the bit and sense lines. This occurs during the rise and fall of the bit current. It determines the recovery time for the array and sense amplifier. The capacitively coupled noise from the bit line divides and is propagated in opposite directions on the sense line. Thus, the polarity of the capacitively coupled bit noise at the two ends of the sense line is the same. The inductive coupling, on the other hand, results in noise of opposite polarities at the ends of the sense line. Thus, on one end of a properly terminated sense line inductive and capacitive noise will add, while on the other end

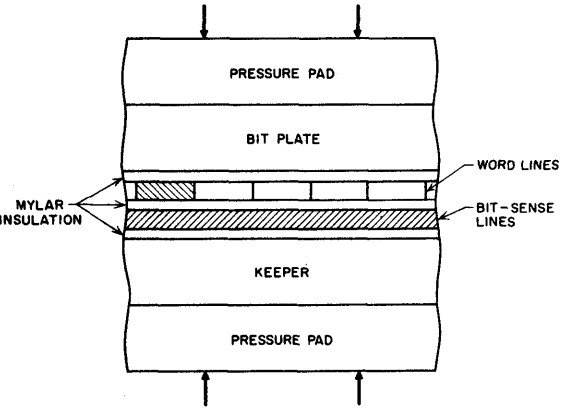

Figure 2. Array sandwich cross section.

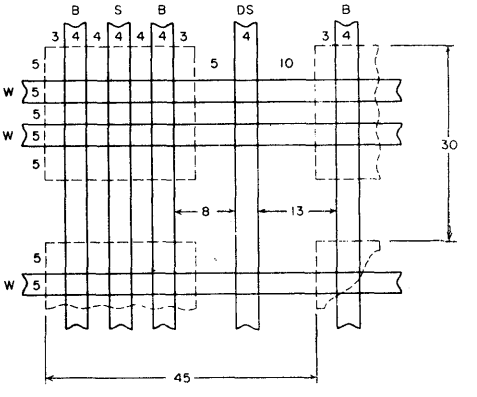

Figure 3. Array plan view—bit and line.

it will subtract. We take advantage of this directional coupling[1] by locating the sense amplifier and the bit driver at opposite ends of the array. The noise reduction thus gained may be as high as a factor of five. A second component of the bit noise is due to resistive coupling in the ground plane. This noise has approximately the same pulse shape as the bit pulse and is controlled by the magnitude of the ground impedance. An additional source of write noise is energy coupling to the sense line from the circulating ground plane currents. This noise is low in amplitude, but since the time constant for ground plane current spreading may be as

long as 500 nsec, this noise may be present during the read portion of the next cycle and so must be considered in the design of the sensing system.

Write noise may be controlled by a number of techniques. Directional coupling has already been described. In addition, several balancing techniques are available. A symmetrical arrangement of bit, sense and dummy sense lines may be employed in the bit sense lines to achieve first order cancellation of self-induced bit noise. This arrangement, however, is wasteful of bit current, and not effective in eliminating coupling between adjacent bit lines. Both self-induced and adjacent bit line noise can be canceled by driving and sensing two arrays in parallel. This arrangement, used in this memory, is illustrated in Fig. 4.

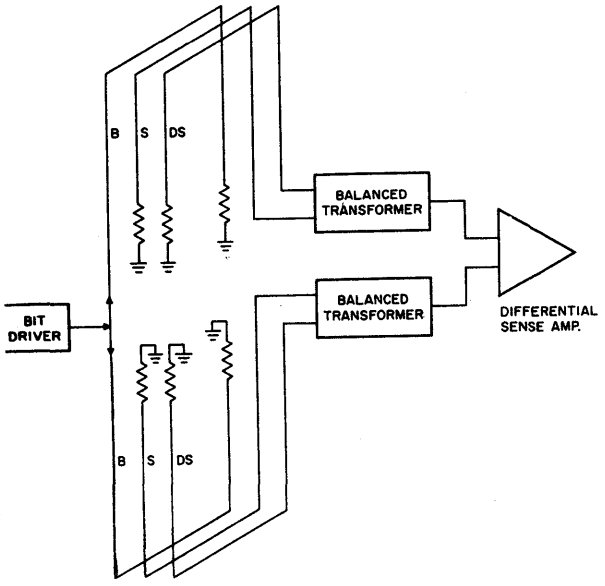

Figure 4. Bit-sense system.

Memory Circuits

The word selection system employs a transistor matrix (one transistor per word line). The nominal word current is 500 ma with a rise time of 7 nsec. The matrix transistors and word and gate drivers are packaged in a card-on-card approach similar to that employed in Solid Logic Technology (SLT).[2] All line impedances are controlled to provide line matching and prevent troublesome reflections. The word lines are terminated in approximately their characteristic impedance (i.e., 17 ohms). Interconnections between the array and circuit boards are made by means of coaxial cables.

The bit and sense circuits are packaged between the two halves on the array. The bit driver circuit provides 100-ma pulses into each of two parallel bit lines with a rise time of 7 nsec. These pulses are positive or negative depending on the information to be stored. The sense amplifier has a matched impedance input fed from a balanced pulse transformer. The output of the sense amplifier is gated into a tunnel diode detector, which feeds a data-register latch circuit. The sense amplifier, detector, data-register and bit driver are all packaged on the same board to minimize delay in the regeneration loop.

The films are vacuum deposited on a $3'' \times 3''$ highly polished copper substrate about 80 mils thick. The substrate is precoated with a micron or more of silicon monoxide to smooth the surface and improve the film properties. This deposition is made in the presence of a strong, uniform magnetic field and at a precisely controlled substrate temperature to produce the desired anisotropy in the films. An initial screening of the bit plates is done by checking magnetic properties using Kerr magneto-optic measurements prior to photoetching into the desired bit pattern. Typical properties are $H_c = 4$ oe, $H_k = 5$ oe, with skew and dispersion less than 2 degrees.

After etching, the bit plate is pulse tested under worst-case operating conditions. Each of the 4,128 bits on the plate is tested with a pulse pattern that corresponds to worst-case conditions, including information pattern, magnetic history, ground plane currents, trapped flux effects, disturb conditions, and marginal currents. Worst-case conditions involve simultaneous word and bit disturb, including disturb effects from adjacent lines, as well as those from lines directly over the bit. A bit plate is accepted only if all bits on the plate meet the minimum specifications for the bipolar one and zero signals.

The copper bit plate serves as the ground plane for the striplines. Interconnection of the bit plate ground planes is achieved with pressure connections around the bit plane periphery. To improve reliability of the ground system, the edges of the bit-plate are rhodium plated.

A metallic substrate, rather than glass or mica, was selected for this application for the following reasons:

1. Close proximity of the ground plane to the sense line reduces noise and permits higher-speed operation.
2. Lower line impedances reduce power requirements of drive circuits.
3. The ground plane reduces field spreading which permits closer spacing of the bits.
4. Metal substrate has more uniform temperature during film deposition resulting in more uniform film properties.

Disadvantages of the metal substrate, which include ground plane current and trapped flux effects,[3] are minimized by the keeper. The memory design includes etched discrete bits rather than a continuous magnetic film for these reasons:

1. Disturb effects (creep) are less severe with etched bits, permitting higher packing density.
2. A lower noise-balanced sense system with a dummy sense line running between the bits can be used.

Conclusion

This paper has described briefly the design of a large, high-speed film memory which represents a substantial speed improvement over the current state of the art in main memories. Key features and design choices highlighted here include the magnetic film element design, the metal ground plane substrate, the use of discrete bits, and the electrical design of the array to minimize noise effects.

Appendix

FILM MEMORY ARRAY PROPERTIES

Word lines

Z_o	=	17 Ω
length	=	24″
attenuation	=	<5%

Bit lines

Z_o	=	31 Ω
length	=	46″
attenuation	=	<5%

Sense lines

Z_o	=	60 Ω
length	=	46″
attenuation	=	25%

Signal = 4 mv (at the film)

Noise

Read Noise	≈	2.4 mv (uncanceled)
	≤	0.4 mv (canceled)
Bit noise	≈	65 mv (uncanceled)
	≤	30 mv (canceled)

REFERENCES

1. G. F. BLAND, "Directional Coupling and Its Use for Memory Noise Reduction, *"IBM Journal of Research and Development,* vol. 7, no. 3 (July 1963).
2. J. J. Corning et al, "Solid Logic Technology: Versatile, High-Performance Microelectronics," ibid, vol. 8, no. 2 (Apr. 1964).
3. V. T. Shahan, and C. J. Townsend, "Measurement of Trapped Flux and Ground Plane Current Effects," 1964 Intermag. Conference.