Engineering design of a mass random access plated wire memory

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INTRODUCTION

Among the newer memory elements, plated wire has been shown to be a serious contender for aerospace and central store applications.[1,2,3] This paper describes a memory development project, sponsored by the Rome Air Development Center, to extend the application of plated wire into the area of mass storage.

The basic memory module consists of 10^7 bits; the mechanical package can hold 10 modules. The potential speed is a 1-to-2-microsecond word rate. Preliminary system, stack, and circuit designs have been completed and a partially loaded model was fabricated and tested.

Memory organization

The memory under development has a capacity of 10^8 bits. This capacity is achieved by stacking ten 10^7 -bit modules into one unit. Figure 1 shows the arrangement and organization of such a memory Each module has its own set of driving circuits and sense amplifiers. This arrangement leads to a fast, random-access memory, readily realizable mechanically; it is justified from the viewpoint of modularity and cost because the electronic circuits are shared by a large number of bits. All modules share one set of auxiliary circuits, which include the address decoders, timing circuits, information registers, and power supplies.

The organization of the 10^7-bit memory module is shown in Figure 2. The memory plane contains 2048 word lines and 4608 plated wires. The word lines are spaced at 0.045-inch centers and the bit lines are spaced at 0.015-inch centers. This results in a storage density of approximately 1500 bits per square inch. The reason these spacings were selected will be discussed later.

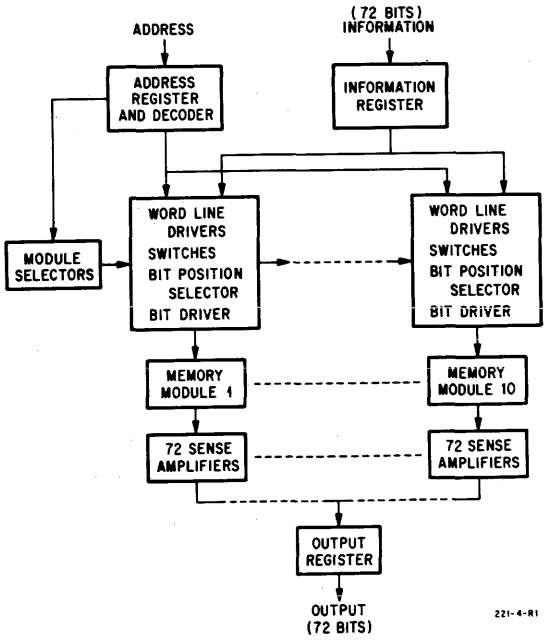

Figure 1 – Arrangement and organization of 10^8-bit memory

The plated wire used is a nondestructive readout (NDRO) element with equal word currents for reading and writing.[3] This property makes it unnecessary to have rewrite circuitry for each stored bit. A word line may be made many machine words in length; each time all the bits in such a word line are interrogated, only the bits belonging to the selected word are routed by a set of gates, called the bit-sense matrix, to the sense amplifiers. After interrogation, all the originally stored information at each bit location along the word line is left unchanged. Correspondingly, the same set of bit-sense matrix gates is employed to route the bit drivers to the proper bit lines of the memory. This feature is illustrated in Figure 3. This property is very

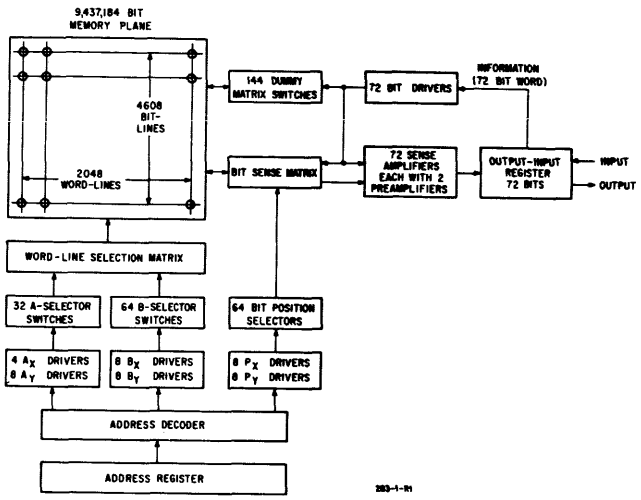

Figure 2 – Organization of 10^7-bit memory module

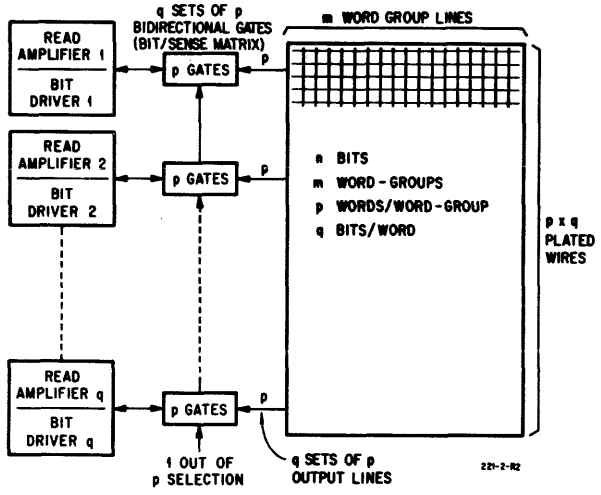

Figure 3 – Modified word-select memory organization

important because it allows a memory configuration to be chosen which leads to a minimal number of bit and word drivers and sense amplifiers.

The word-line matrix, bit-selection matrix, and selector switches are included physically in the memory stack; as a result, the number of connections between the memory-access circuitry and the module is reduced to a minimum.

Stack design

Two possible word-line constructions were considered. The first, called a half-turn line, consists of a single flat conductor over the plated wire, the wire being over a ground plane. The second type, a full-turn line, is a flat conductor wrapped around the wire, with the entire assembly mounted over a ground. The full-turn line provides a stronger and more confined field per unit of word current, thus giving less adjacent-word interaction and allowing lower word currents to be used. However, it presents significant mechanical problems in plane construction. Word lines must be etched double-length, and accurate registration between top and bottom conductors must be maintained.

Work has been published[4] which indicates that the placing of a magnetic keeper over the half-turn word line gives that configuration the advantages of the full-turn line, namely, low operating word current and low susceptibility to adjacent word interaction. Tests were performed to verify the theory; the results are shown in Figures 4 and 5 for full-turn and keepered half-turn word lines on 45-mil centers. In these figures, I_{wP} is the so-called "pop point" word current, representing a lower limit on word current; I_{wD} is the word current for destructive readout, and I_{wA} is the current flowing in the adjacent word line which will cause significant interaction in the bit under test. Based on these tests, it was decided to use a half-turn keepered word line, 33 mils wide, on 45-mil centers.

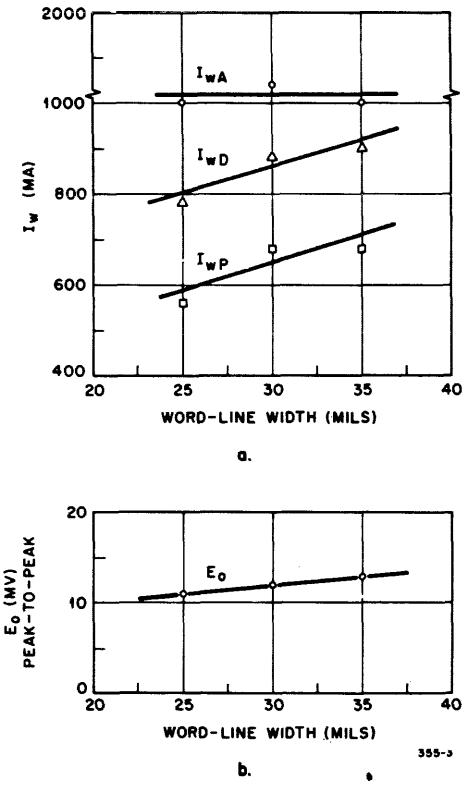

Figure 4 – Word current (a) and output (b) as functions of line width, for one-turn copper word lines

When an 8-foot sense line was contemplated, crosstalk between plated wires during a read operation was a major consideration. With a readout signal being

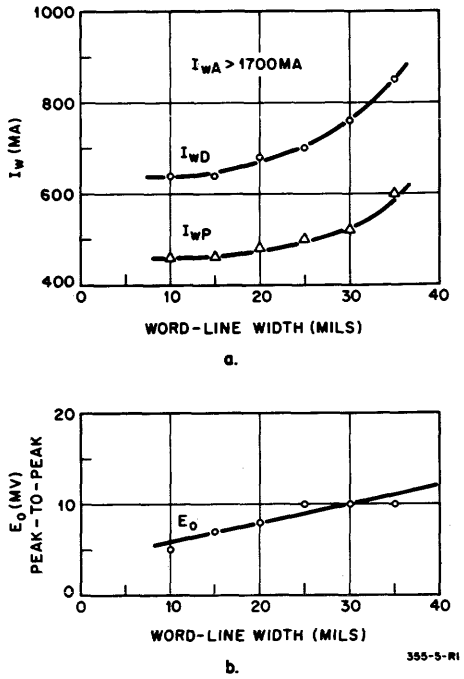

Figure 5—Word current (a) and output (b) as functions of line width, for half-turn copper word lines with mu-metal keepers

generated on all wires crossed by a word line, portions of the adjacent wire signals couple across to the wire being sensed. This crosstalk will either add to or subtract from the desired signal. Crosstalk signals have been broken into their forward and backward components, according to Feller et al.,[5] with appropriate modifications to conform to the fact that one end of the plated wire is grounded, while the other is properly terminated by the bit-sense matrix. It was found that for the word-current rise times anticipated, the peak of the crosstalk from adjacent wires could be more than 50 percent of the peak signal being sensed. However, the time integra of the crosstalk is zero to a first approximation. Therefore, it was decided to use an integrating sense amplifier for the memory to eliminate the effects of crosstalk.

Figure 6 shows a diagram of the plated wire selection scheme. Two dummy wires are associated with every 64 plated wires. Dummy line A is selected any time a plated wire from the 1-to-32 group is selected. Dummy line B is likewise selected at the same time as a wire from the 33-to-64 group. The dummy wires are used for noise cancellation. They are nonmagnetic wires and do not switch. The bit line selection scheme for a bit group is shown in Figure 6.

When information is written into the memory, bit current is driven down the selected wire and down a dummy wire in order to minimize the effect of a large bit-transient voltage in the differential sense amplifier, which would occur if current flowed only in the plated wire. When information is read from the memory, identical noise is coupled into the plated wire and the dummy by the word current and hence can be rejected by the differential sense amplifier.

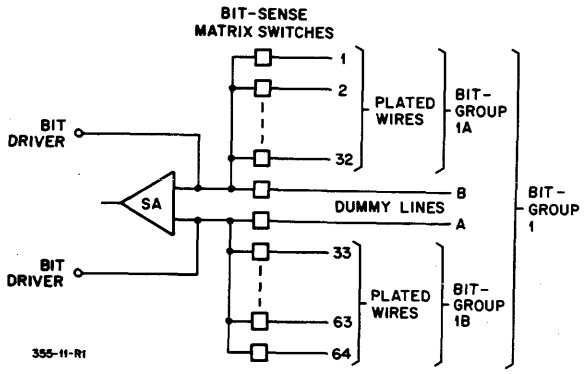

Figure 6—Plated-wire selection scheme

Because the dummy wire associated with bit-group 1A is selected when bit lines in group 1B are being interrogated, and vice-versa, a symmetrical situation is created which reduces the noise in the sense amplifier due to capacitance coupling of word line noise through the unselected bit-sense matrix switches. To explain further, if all the plated wires were connected to one differential input of the sense amplifier and only the dummy wire to the other differential input, noise coupled to the sense amplifier through the off-impedance of the bit-sense matrix switches would cause a noise imbalance. The symmetrical assignment of plated wires and dummy wires allows these off-impedance coupled noises to be in balance and to be rejected by the differential amplifier.

Stack construction

The 10^7 -bit module consists of two half-planes, one 4 feet 9 inches × 3 feet 2 inches, the other 4 feet 9 inches × 3 feet 9 inches, joined by a hinge along their 4-foot, 9-inch sides (see Figure 7). Forming the core of the plane is a 0.25-inch aluminum honeycomb structure, covered with a 5-mil aluminum skin which serves as a ground. Both surfaces of each plane are used. Tunnels to contain the plated wires are made in continuous lengths, 252 wires wide, as follows: A sandwich is formed by pressing 8-mil monel wires on 15-mil centers between an 8-mil sheet of Teflon and two outer 2-mil sheets of Kapton film. In the process, the wires become embedded in the Teflon. The material is then cut to the proper length and the monel wires pulled out. The tunnels

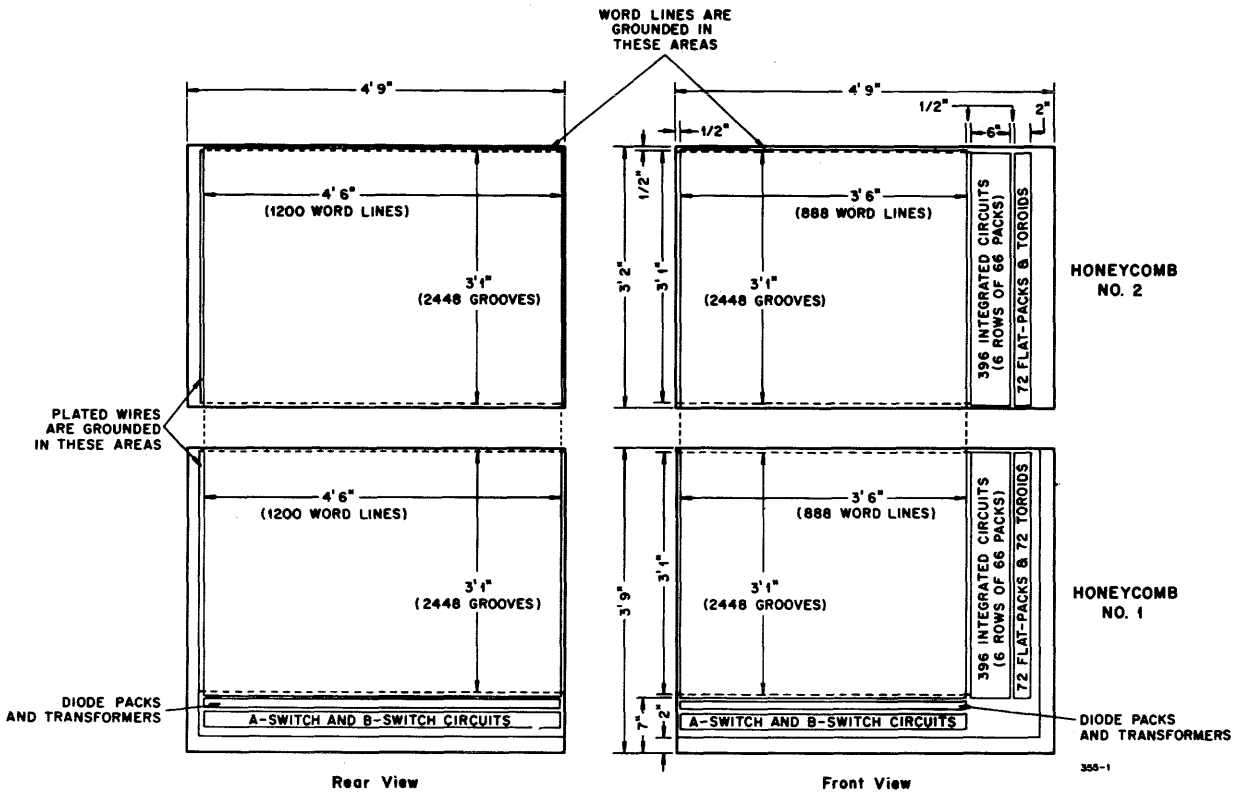

Figure 7 – 10^7-bit module layout

thus formed easily accommodate the 5-mil plated wires. Strips of this tunnel structure are bonded to the aluminum planes with their lengths parallel to the long edge of the plane. The word lines are fabricated as etched cables 120 lines wide of 1-ounce copper on a Kapton film base. They are bonded perpendicular to the tunnels and are continuous across the hinge connecting the two physical halves of the plane. Strips of magnetic keeper material 6 inches wide are bonded over the word lines parallel to them. Small gaps were left between adjacent strips so that noise could not propagate along the keeper for more than 6 inches in the bit direction. Plated wires are connected in series from the front to the back side of the plane and grounded at the far end. At the near end, the wires are terminated in boards containing the bit-sense matrix packages. Other boards, containing matrix diodes and transformers, mount on the plane and connect to the word lines.

Memory circuits

In general, the memory circuits used for this model are straightforward or have been described previously.[3] A description of several unique circuits follows.

Bit driver

The bit driver is shown in Figure 8. The phase-modulated-write method used in this memory system requires the writing of the complement information first, followed by the writing of true information during the writing of a bit. Therefore, if a 1 is to be written in a bit location, a 0 is written first, followed by the writing of the 1. Transistors Q1 and Q2 (see Figure 8) are pulsed sequentially on and off by the information generator in the memory exerciser during a write-1 instruction. This generates a negative and then a positive current in the secondary windings of the transformer. The sequence of pulsing Q1 and Q2 is reversed for a write-0 instruction.

With a nominal collector-supply voltage (V_{cc}) of + 12 volts, resistor R1 limits the current in the primary winding to 64 milliamperes. This allows the secondary to deliver 32 milliamperes to the plated wires and 32 milliamperes to the dummy wires. This arrangement of the bit current prevents the injection of a large, differential, bit-transient signal in the sense amplifier, thereby minimizing the recovery time. This arrangement of the bit driver allows a cycle time of a few microseconds. The transformer consists of two 6-turn bifilar windings located on

opposite sides of the core corresponding to the primary and secondary windings. These windings are intraconnected to produce the proper phase.

Use of a single supply and a single resistor to control the amplitude of both polarities of the bit current ensures their equality.

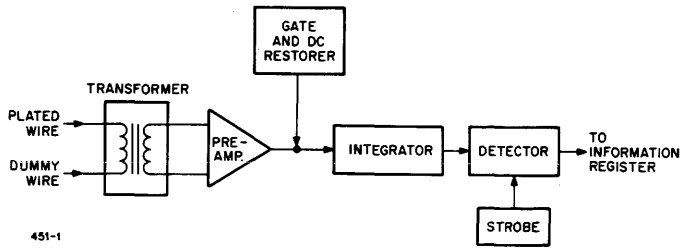

Figure 8 – Bit-driver design

Sense amplifier

An integrating sense amplifier is used for the memory. This detects the time integral of its input rather than its peak amplitude. Such an amplifying system has several advantages in a large memory, including the following:

a. Crosstalk from readout signals in adjacent wires is cancelled, since its time integral is zero. This benefit has been discussed above.
b. Word line noise coupled to the plated wire has, to a first order, a zero time integral. It, too, is cancelled out in the amplifier.
c. Dependence on the fall time of the word current is minimized. Since the area of the plated-wire readout signal is a function of word current amplitude but not of speed, use of an integrating sense amplifier relaxes the requirements on the word circuitry.
d. Approximately equal output areas result from readouts at all positions along the plated wire. A readout from the grounded end of the wire yields a single pulse, while transmission line behavior causes the readout from the other end of the wire to reach the sense amplifier as two like-polarity pulses of lower amplitude. If line attenuation is neglected, the total area of both readouts is the same, so that the integrating amplifier gives identical outputs.
e. Strobe timing is less critical with an integrating sense amplifier. A peak-detecting amplifier must have as narrow a strobe as possible to prevent its triggering on noise. With the signal delays along an 8-foot bit line, narrow strobing would be difficult. The integrator, however, holds its maximum output sufficiently long to permit a wide strobe and looser tolerances on its timing.

A block diagram of the sense amplifier is shown in Figure 9. The transformer input to the preamplifier is required to allow the proper d-c biasing of the preamplifier. It also provides common-mode noise rejection. The gate is a low-impedance shunt which is normally closed. This provides a d-c zero reference at the integrator output. During the interval when the wire signal is to be sensed, this gate is opened. The integrator then charges up, and the gate is closed. Next, the strobe is energized, and the detector provides an output pulse for one polarity of plated-wire signal and no pulse for the other polarity.

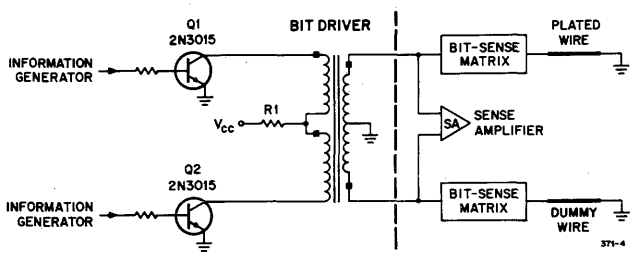

Figure 9 – Block diagram of sense amplifier

A complete schematic of the sense amplifier is shown in Figure 10. As can be seen, the major components are off-the-shelf integrated circuits. To achieve versatility, these circuits generally omit input biasing networks. Coupling capacitors must also be added. The transistor which serves as the gate is operated as a chopper in the inverted mode. This technique provides very low impedance to ground when the transistor is on and could not have been achieved with a standard integrated circuit. The strobe circuit, while available as an integrated circuit, was more readily built from discrete components.

A Texas Instruments SN 5510 serves as the preamplifier. It has a bandwidth of 40 megacycles, more than adequate for the purpose, and a voltage gain of about 80. Only one-half of its differential output is used. A feedback capacitor was added to the RCA CA-3002 linear amplifier to convert it to an integrator. The Fairchild μA 711 is a high-gain amplifier with strobe provisions. It has a very small linear range, about 3 millivolts at the input, and is thus useful as a pulse shaper. The bias adjustment is used to set the desired trigger level. When the signal input exceeds this level, the output follows the strobe pulse.

Tests of the sense amplifier indicate that it achieves all design goals.

Word circuitry

With the two-dimensional diode matrixing used to select word lines in previous memories,[3] half-selected

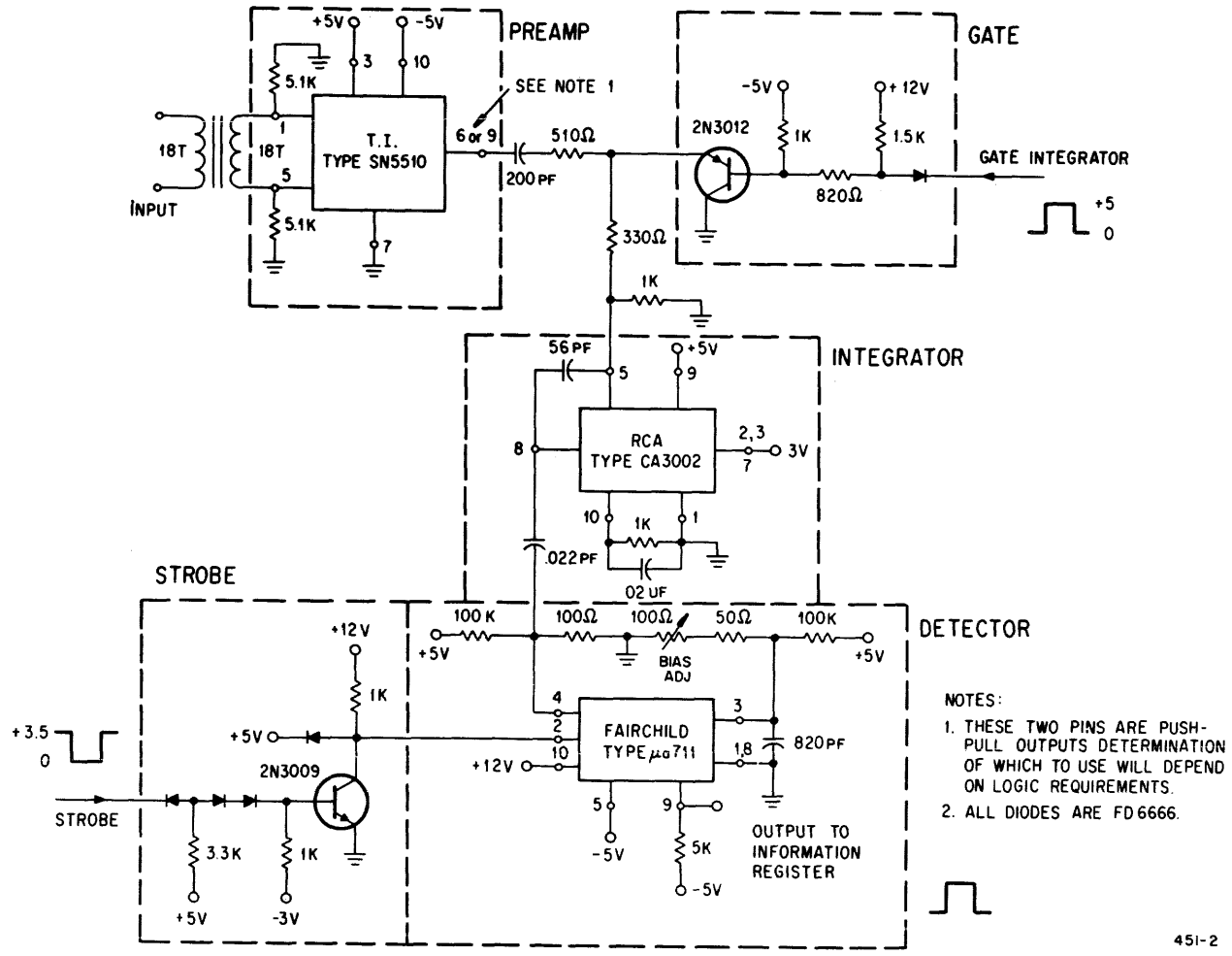

Figure 10—Sense amplifier, schematic diagram

lines were driven through a large voltage excursion by the B-switch. To drive the 0.016-microfarad capacitance of 32 six-foot lines in the present memory would have presented serious circuit difficulties; it might result in a limitation of cycle time and additional system noise. Therefore, a transformer-diode matrix was used instead, with one transformer and one diode per word line, as shown in Figure 11. Conventional diode matrixing is performed on the two ends of each transformer primary just as it had previously been done on the two ends of each word line. By permitting one end of the word lines to be at d-c ground, the transformer-diode matrix reduces system noise.

Memory model

The memory model constructed consists of a mechanically complete 10^7-bit stack. Word line and bit-sense-matrix circuits have been provided to address 32,768 four-bit words at the intersections of 512 word lines and 256 plated wires. These addressable locations were chosen at the four corners of the stack to provide limit conditions. Each addressable word line contains 64 four-bit words, with the remaining tunnels containing nonaddressable plated wires to give a worst-case loading condition of the word line. Two bits of each word are at the driven end of the word line, while the other two are at the grounded end. Similarly, each addressable plated wire passes under 256 addressable word lines at its grounded end and another 256 at its bit-sense-matrix end. Thus, the four corners of the stack are addressed and tested by the memory exerciser described below.

The model was tested at a 200-kilocycle-per-second word rate. The speed was limited by the recovery of a transformer in the circuit driving the bit-sense matrix. Since this limitation is not fundamental to the stack or system design, and since the development specifications call for only a 20-kilocycle-per-second word rate, this circuit was not redesigned.

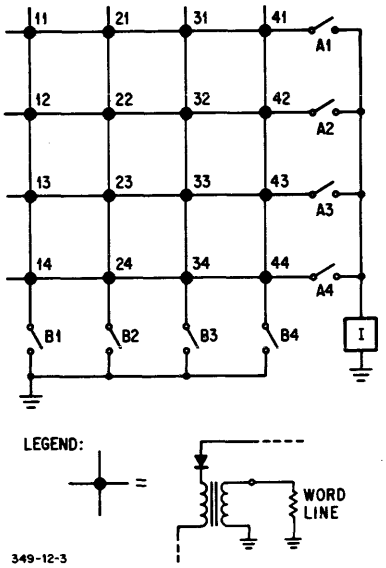

Figure 11 – Word-line selection matrix

Memory exerciser

Operation modes

The exerciser is capable of supplying various information patterns and modes of operation. These modes are write (W), read (R), write/read (W/R), write/read/subscan (W/R/SS). The W and R modes simply allow information to be written into or read from the memory. The W/R mode allows the exerciser to exercise each address (four bits) by writing information into the bit position and immediately reading it out a predetermined number of times. The W/R/SS mode permits the exerciser to write information into all bit positions once, until the memory is filled, and then allows the information to be consecutively read out a preset number of times.

The simplest information pattern that can be checked is all 1's or all 0's. Also, the information can be varied so that each bit contains the opposite information from the preceding bit, which will produce a 1-0 test pattern either down each word line, down each bit line (plated wire), or down both word and bit lines to produce a checkerboard pattern throughout the memory plane.

Worst-case test patterns

The memory exerciser is capable of generating several information patterns. These patterns have been designed with worst-case plated-wire tests in mind.

One test is designed to ensure the nondestructive readout property of the plated wire. This test is implemented by writing into the memory certain information patterns and then repeatedly reading the memory without rewriting. This test is also implemented in combination with other tests.

Another test is to check adjacent-bit disturb. The plated wire, being a continuous-storage medium, is susceptible to adjacent-bit-disturb phenomena. This is tested by writing 1's once into alternate bits in the memory and then writing 0's repeatedly into all other bits. The 1's are then read out and checked. This information is then complemented, the 0's read out and checked, and then the roles of the disturbing bits and test bits are reversed and the test procedure is repeated. An added feature of this test allows reading the test bits repeatedly while writing into the disturbing bits. This procedure then checks NDRO as well as adjacent-bit-disturb effects.

The plated wire is subject to disturbing due to adjacent-wire coupling. This effect is tested by writing into adjacent wires the same information as that stored in the bit under test. The information in the bit under test is then read out. Next, information opposite to that stored in the bit under test is written into the adjacent wires, and again the bit under test is read out. This last test is also used to check the diminution of the output signal from the test bit, as seen by the sense amplifier, by the information of opposite polarity stored in the adjacent wires feeding through the off-impedance of nonselected bit-sense-matrix switches.

CONCLUSIONS

Compatible system design, mechanical fabrication, and unique circuit designs of a mass random access plated wire store have been described. The system design fully utilizes the NDRO property of the plated wire and results in a low electronic component count. Ease of fabrication has been emphasized in the memory stack design. These factors, together with the low plated wire element cost, make an inexpensive mass plated wire store a distinct possibility.

ACKNOWLEDGMENT

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