The physical attributes and testing aspects of the symbol system

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INTRODUCTION

The major goals of the SYMBOL computer research project have been to provide a more effective man-machine interface and to reduce the total cost of a digital system to the user. The development of the multi-processing/multi-programming computer architecture with much of the executive system, memory management, and high-level language implemented in hardware is described in other related papers.[1,2,3] The SYMBOL project also has investigated low-cost construction techniques suitable for equipment to be used in commercial/industrial environments.

The packaging system utilized (See Figure 1) is a free-standing, self-contained unit with the electronics fabricated entirely on two-sided printed circuit (p.c.) boards. In addition to low-cost mechanical packaging, special low-cost test equipment has been developed. It utilizes the same mechanical packaging and allows very rapid and efficient testing of individual logic boards and of the full SYMBOL system. These techniques result in a significant savings in the amount of engineering manpower required for hardware prototype debugging.

PHYSICAL CHARACTERISTICS

One of the first problems attacked by the SYMBOL research project was the excessive cost and interconnection complexity of the mechanical packaging techniques commonly used for digital systems. The mechanical packaging system developed allows the use of free-standing, self-contained units requiring no special or raised floors and no special cooling, and using commercially-available power supplies. The SYMBOL computer shown in Figure 1 utilizes this packaging approach. The section above the table top contains all the logic and system interconnections for the CPU, I/O channels, memory controls and system executive controls.[2] The lower section contains all of the power supplies, power controls and the cooling components. In Figure 1B the section above the table top and in the foreground is the SYMBOL logic. The smaller enclosed section in the rear is a hand wired system maintenance unit.

The logic (upper section) is fabricated on large (12″ × 17″) two-sided printed circuit boards with plated-through holes. (See Figure 2). These logic cards contain all of the active logic components in the SYMBOL system and are easily removed and repaired. As shown diagramatically in Figure 3, the logic boards are mounted on one-half inch centers between a pair of two-sided printed circuit "motherboards."

Interconnections between logic cards are made on the motherboards with parallel lines for bus connections. The local buses which intraconnect Autonomous Functional Units (AFU's)[2] are physically identical to, and intermingled with, system buses which interconnect the AFU's (global signals). These printed circuit buses provide all required system interconnections. Every signal pin position has two associated buses. One bus connects to the pin while the second bus bypasses the pin. A signal on the connect bus and a signal on the bypass bus may "cross-over" between board positions (Figure 3). In addition, either or both buses may have continuity breaks to isolate groups of boards (Figure 5).

Due to practical limitations on motherboard size, the SYMBOL system has been implemented using five motherboard modules. Each motherboard module can interconnect thirty logic boards. In the SYMBOL system four modules are used for the computer logic and one module is partially used for the system maintenance unit. As mentioned above, all signals in the system are distributed on the printed circuit wires of the two-sided logic boards and motherboards. The only exceptions are cables to external peripheral devices and bulk

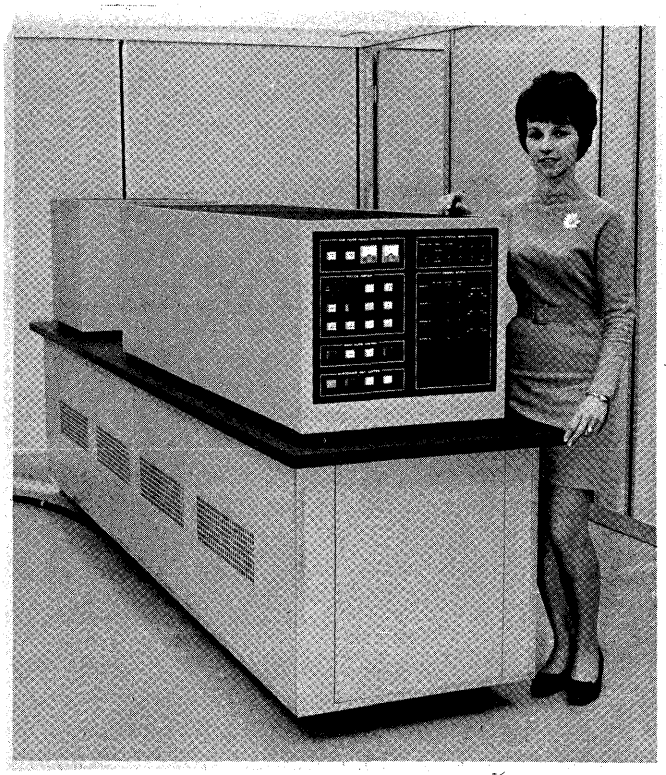

Figure 1a—SYMBOL main frame including power, cooling, logic and interconnects

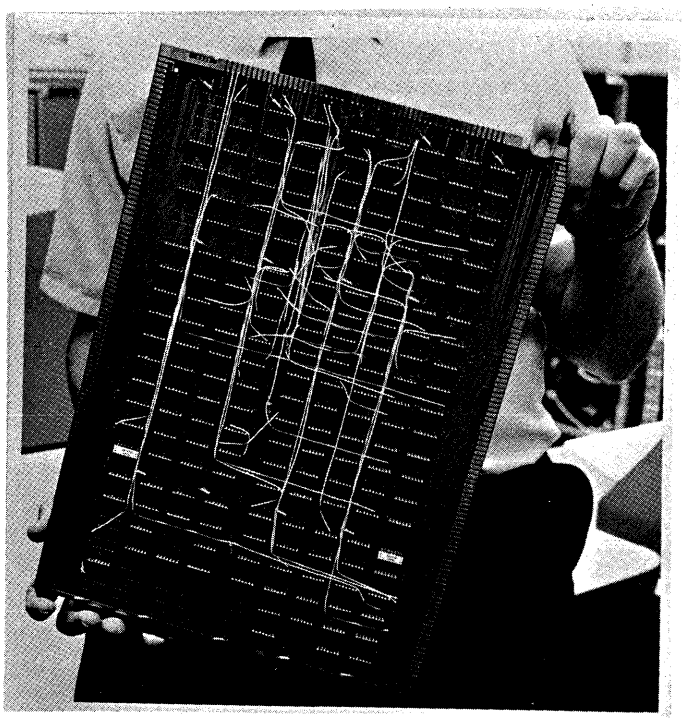

Figure 2—Typical 12″×17″ two-sided logic board with additions or changes in discrete wires

storage (Figure 4) wires which fix errors or implement design improvements (Figure 2), and the short jumper wires used to connect the motherboard modules (Figure 5).

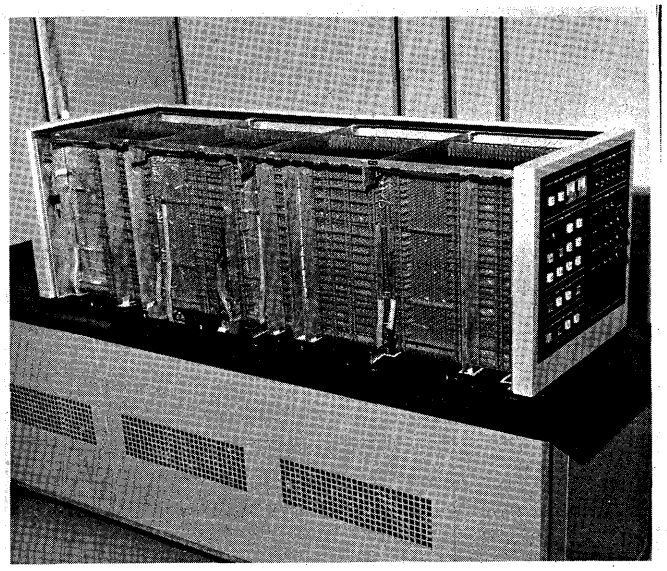

Figure 1b—SYMBOL main frame with covers removed

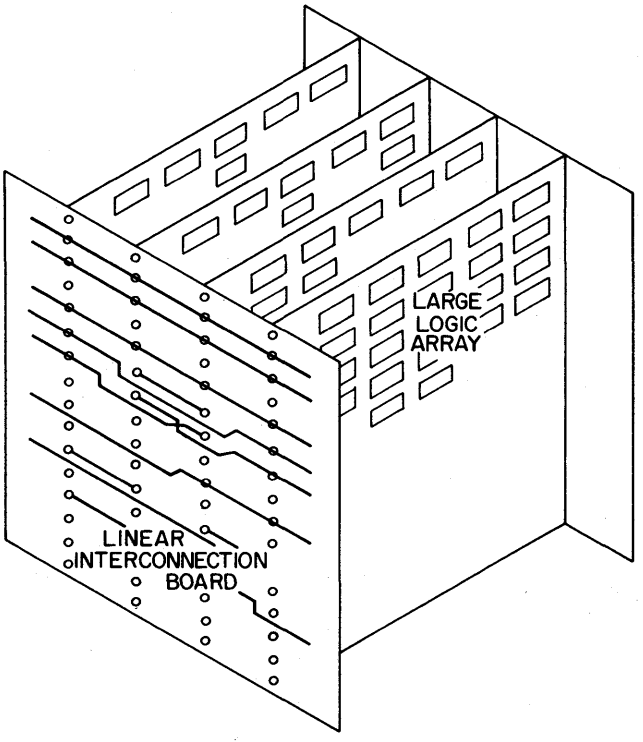

Figure 3—Conceptual physical organization of SYMBOL

As Figure 3 shows, connectors are required on two edges of the logic boards to provide signal paths to the motherboards. A cam-operated contact system was developed to allow zero contact-force insertion and removal of logic boards (from the top) and to provide high reliability, high pressure contact when engaged. The contacts themselves are soldered into the motherboards and, together with some molded plastic card guides, become a permanent physical part of the motherboard interconnection system (see Figure 6). To cam or uncam a board involves rotating two cam pairs using a cam key. No special board handles, locks, etc., are required.

In addition to logic board contacts on the inside of a motherboard, contacts may be provided on the outside of the motherboard at each board position. The connector positions on the outside of the motherboard allow lamp panel maintenance aids called wing panels (Figure 7) or printed circuit board cable connectors called paddleboards (Figure 4) to be connected to any board position in the system. In practice, only those positions specified before fabrication are used for external connection.

The signals interconnected by the motherboard system originate on the logic boards. Figure 2 shows a typical logic board. The 200 signal pins, a clock pin and a number of power pins on the two long sides connect to the motherboards. An additional fifty pins used for test points are available on the top of the board for monitoring during system operation and test. A typical logic board holds about 175 dual in-line packages; the maximum capacity is 220 packages. High packaging density has not been a major system goal. On the contrary, emphasis is placed on functional completeness and interconnection density on a board. An additional effort was made during prototype fabrication to guarantee some extra package positions on each board (at least ten percent) to allow implementation of logic functions "overlooked" and design improvements. Discrete wires are used to repair board fabrication errors and to implement additional logic. No degradation in performance has resulted and no special electrical considerations have been required. Surprisingly, not one board has had to be remade for the system. Discrete wire and component additions to the original boards have sufficed to bring the system to an operational state.

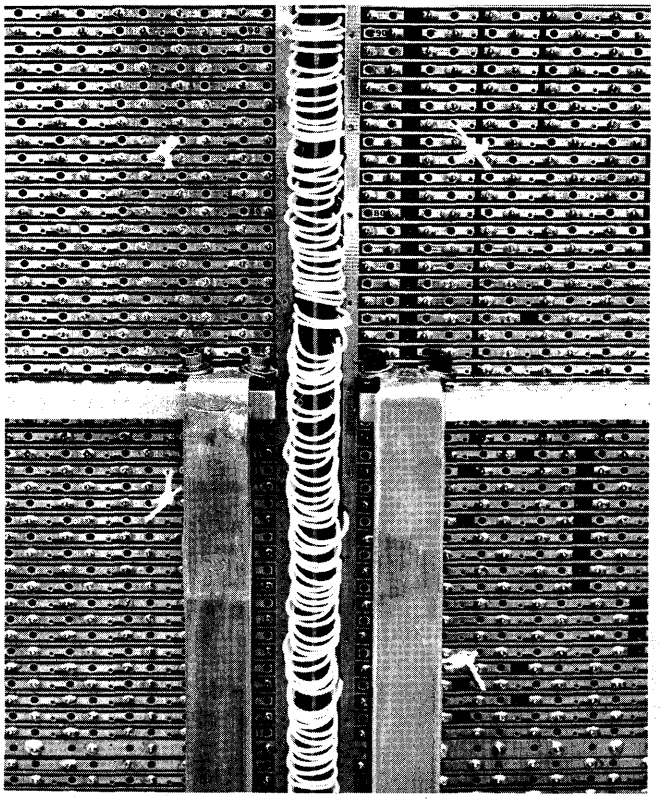

Figure 5—Motherboard module interconnect wires and main power distribution system

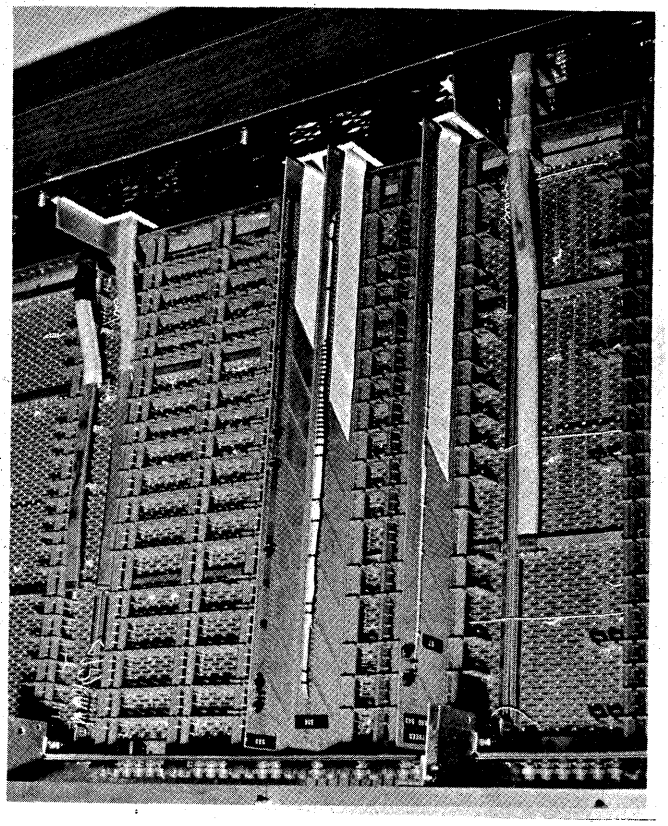

Figure 4—Paddleboards with cables to external peripheral equipment and bulk storage devices

Figure 6—Zero insertion force, cam-operated connector system

ELECTRICAL CHARACTERISTICS

A mechanical packaging system is useless unless the digital system itself can operate successfully in that package. The electrical characteristics of the SYMBOL system were chosen to provide a relatively high-speed system using conventional technology. Design decisions were made with speed enhancement and noise suppression high on the list of design criteria. Few concessions which compromise economy have been permitted.

Circuit family

The Complementary Transistor Micro-Logic (CTμL) circuit family chosen facilitated both the ease of design and the operating speed of the system. The CTμL family[4,5] is a positive logic family with wired-or capability at every point except at the flip-flop outputs. The basic AND gate is a emitter-follower device with relatively slow rise and fall times (7-10 nsec for the 3V swing) but with a relatively fast propagation delay through the gate (typically less than 5 nsec). The slow rise and fall times significantly reduce the problems of fabricating a high-speed system on two-sided printed circuit boards. However, since the basic gate is non-saturating, there is a slight voltage degradation through each gate. Thus, level restoring elements (AND, NOR, LATCH, FLIP-FLOP) are required at various places in a chain of logic as shown in Figure 8. In SYMBOL (a synchronous system) the total chain allowed in one clock cycle is four sets of the gate and level restorer combinations. The experience gained in SYMBOL shows the importance of the wired-or capability very clearly. There are a significant number of five, six, or seven-way wired-or ties. If discrete OR gates had been required, the size of the system would have been significantly larger. Most AND functions are four inputs or or less with the average about two-inputs. There are some 10-way and larger OR-ties.

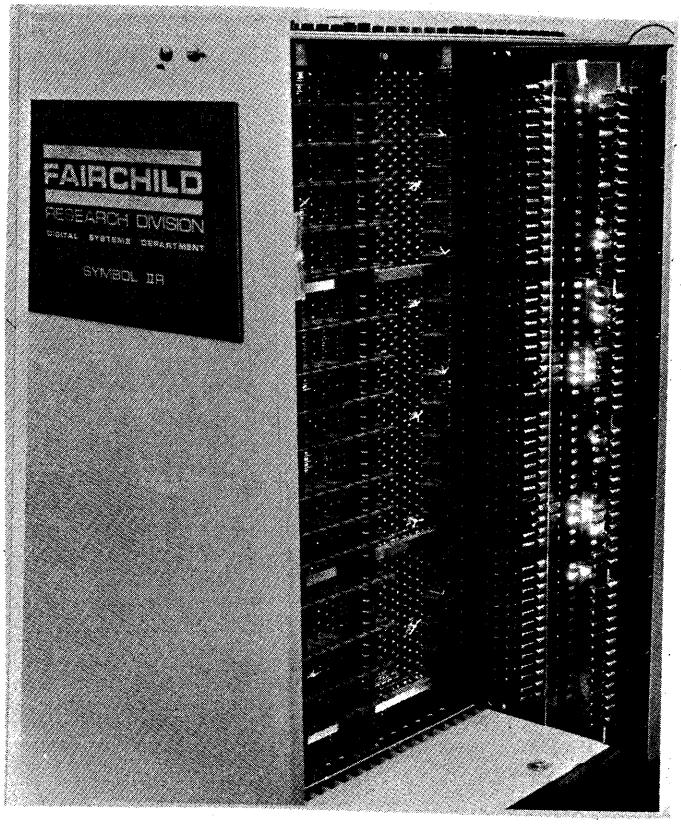

Figure 7—Wing panel in motherboard position for monitoring signal buses

CAD support

A computer-aided design (CAD) system was developed to assist appropriate design and fabrication operations in the development of SYMBOL. The approach was not one of developing a general system and then using it for the SYMBOL design. Instead, when a need developed where CAD programs could help, a new section of the system was generated specifically for that need. Usually the new section of the CAD system was generated by the engineer or designer first requiring that section. The resulting system greatly enhanced the power of the designers and the reliability of the final system.

One of the sections of the CAD system is a logic design assistance section. In this section, each device is characterized as it can be expected to perform in the system environment. This system characterization is in terms of quantized, normalized units of time delay, signal voltage degradation, threshold variations, and fan-in/fan-out effects. Time delay characterization includes an allowance for typical propagation delays as well as device delays. Special noise conditions (such as global signals or cables to peripherals) are accounted for by modifying the characterization of the devices used in these services. Special time or loading conditions can be forced, especially in the case of long bus signals. The CAD system points out violation of noise margins, load, or time delays so that the designer can modify a design to comply with the system rules.

In the section of the CAD system which performs the logic placement and wire routing functions, no attempt was made to specifically minimize wire lengths or to provide the maximum number of devices per board. Instead, placement and routing were based on interconnect capability of the two-sided printed circuit board. The rules for partitioning of logic to various boards by the designer were also based on this same criteria, modified by an added criteria that the printed circuit cards should consist of complete functions.

Signal distribution

Many signal distribution problems are encountered when using high speed circuits.[4,6,7] The choice of the CTμL logic family considerably reduces the problems of signal distribution in systems with two-sided printed circuit boards. Signals between boards within an AFU are treated no differently than on-board intraconnects. These signals are the AFU intraconnections on the motherboards and are less than eight inches in length. No attempt is made to provide terminations or impedance controls.

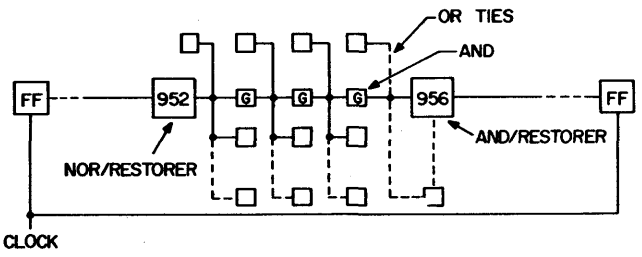

Figure 8—Representative $CT\mu L$ logic chain in SYMBOL

Global signals, on the other hand, can be as much as six feet long. The base interconnects for these signals are treated as transmission lines with distributed discrete loads, and an approximate termination is placed at each end of the lines. The clock line is a particular example of this type of signal (Figure 9). The copper trace for this signal is as wide as practical to reduce its impedance. The wide trace reduces the effect of the loads on the propagation velocity and minimizes reflections and distortion on the line. Each of the boards (107 total) in SYMBOL presents a load on the clock line of approximately 500 ohms to ground. To drive this low impedance load a special clock driver is required, one of the few discrete circuits in the system. The other main bus signals (except for system clear) did not require discrete circuits because each AFU was constrained to connect to the system bus only once.

POWER

The SYMBOL electro/mechanical system is designed to deliver properly regulated power at each circuit in the system and to remove the generated heat. Cooling of the system is accomplished with miniature axial fans blowing air upward through the card cage. No special room air conditioning is required. Power distribution is somewhat more complicated. Although the power distribution system was designed to provide excellent DC regulation, ease of installation and economy took precedence over requirements for dynamic performance. However, power distribution had to be appropriate for the high-speed circuits in the system.[8] Power is distributed throughout the system using a combination of large copper bus bars on the motherboards and a power distribution grid of printed-circuit wires on the logic boards.

The current in a thirty card module is approximately 200-250 amperes. To distribute this much current over the fifteen inch span of the module, a large copper bus is used. This bus in turn is connected to the main distribution bus by laminated copper risers (see Figure 5).

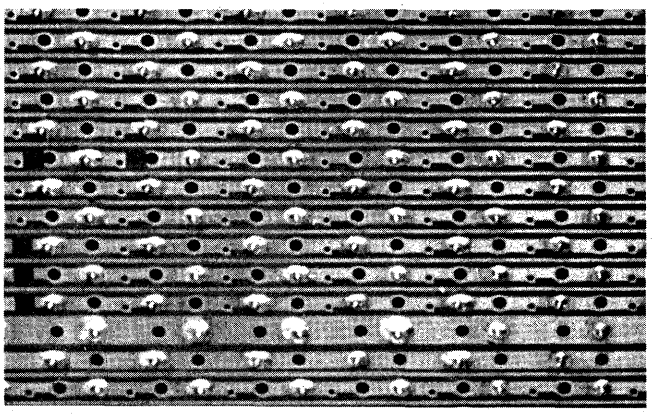

Figure 9—Close-up of motherboard showing wide clock line with wide and narrow ground lines for shielding

The system power is distributed longitudinally near the lower edge of the motherboards. The voltage regulators use remote sensing at the main distribution buses. The riser, distribution bus, and printed circuit board distribution system are sufficiently massive to provide regulation of less than fifty millivolts from the sense point to the remote sectors of the printed circuit board.

The power distribution system on the logic boards is standardized to provide a pseudo-ground plane made up of the composite of the positive, negative, and ground distribution grids (Figure 10). The grid geometry was chosen so that the circumference of a net cell is less than a half wave length for the highest frequency of appreciable magnitude. The size of the logic board is such that local filtering on the boards is more efficient and productive than attempts to provide super-low distribution impedance. The decoupling capacitors can be seen on the logic board in Figure 2.

The CTμL circuit family chosen for use in SYMBOL requires two supply voltages in addition to ground. The three-terminal DC equivalent circuit can be represented as in Figure 11. As can be seen, the ground terminal can be viewed as a current source to the power system, requiring that approximately thirty percent of the positive terminal current be diverted by an appropriate sink. In the SYMBOL system, a shunt regulator stabilizes the potential between the negative terminal and the ground terminal. This technique is used instead of the normal two supply (+V, −V) system because only 4I worth of supplies and related inefficiencies are required (3I for +V and I for ground regulation) instead of 5I (3I for +V and 2I for −V).

The power supply system used is a floating supply which uses a combination of unregulated and regulated supplies to generate 800 amps at 6.7 V. Since the power load of CTμL does not change appreciably with the state of the device, the variation in the current within the system is less than thirty percent. Most of the current is supplied by unregulated sources (a sort of poor man's current source). The remainder is provided by tightly regulated, commercially available voltage sources which are distributed along the main power bus and provide current required to maintain regulation. Each component of the power system is small enough for easy installation and maintenance, yet large enough to provide economical power. In addition to being economical, the distribution elements are self-adjusting in case of failure. Consider the two possible modes of failure, over voltage or loss of voltage. If a single unit fails by over voltage, all the other regulated sources shut off. The resulting load of the system imposed by these sources shutting off prevents the voltage from rising to destructive levels. If a single unit loses voltage, remaining supplies have a sufficient reserve of current capacity to provide the necessary current with only a minor degradation in regulation in a localized sector of the system.

TESTING TECHNIQUES

Since logic designers and logic devices never seem to be perfect, all the advances in architecture and mechanical packaging would not be useful unless some techniques were developed to allow the system to be tested. Many approaches to solving the testing problem have been reported.[9,10,11] SYMBOL has unique prob-

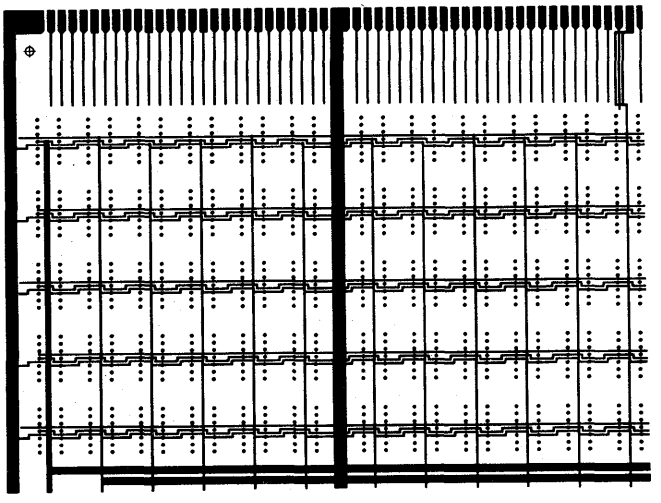

Figure 10—Composite +V, −V, GND power distribution grid on SYMBOL logic boards prior to signal routing

lems analogous to trying to test both the CPU and most of the executive system simultaneously. During design and system partitioning it was found that functional splitting of logic tended to minimize bus lines used. Such a split also became useful during testing. A combination of manual and automatic test aids has been developed to support the SYMBOL project. The SYMBOL documentation, board test, system monitoring, and system test techniques (discussed below) are low-cost approaches to solving the unique SYMBOL testing problems.

Documentation

Documentation of the system was one of the first problems encountered. The documentation used to support SYMBOL fabrication and testing is quite simple. A computer-generated listing from the CAD system describes (in a pseudo-equation form) the logic implemented on each node, the name and reference number of each signal involved, the physical location of the pins on the logic element which implements the node, and the origins and/or destinations of all signals involved. Since all cross-references for a node are given at one point in the document and since the signals are listed in both alphabetic (by signal name) and numeric (by reference number) order, engineers and technicians waste little time trying to find related logic. The CAD system includes comprehensive document editing features to allow easy modification of the original logic and specification of added logic. Both logical and physical descriptions in the document can be edited. The editing features combined with simple procedures to obtain up-to-date documents have provided excellent communication of logic changes to all those involved with the testing process.

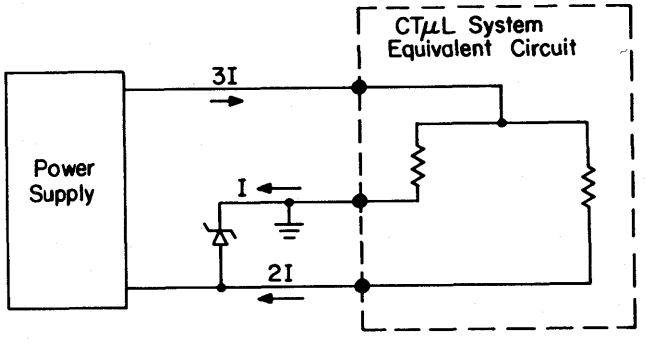

Figure 11—DC equivalent circuit of SYMBOL

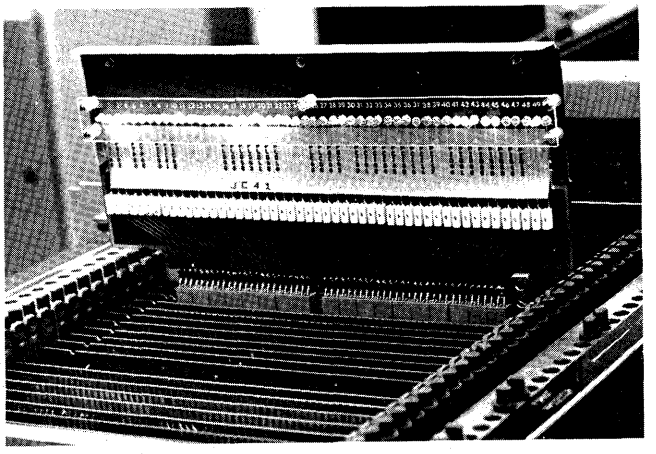

Figure 12—Test point panel used to monitor logic boards during system operation

Test point and bus monitoring

It was noted earlier that the printed circuit logic boards have fifty test points along the top edge. In SYMBOL the designer assigned these test points to signals he thought were of interest. These signals are usually phase-counters and their controls, state flip-flops and central logic decision points. In a production environment, the test points would probably be chosen to allow efficient isolation of fabrication errors (rather than logic design errors as in the prototype). A special indicator panel, called a test point panel, has been designed to connect to the test points and to receive power from the board under test. Figure 12 shows this panel installed on a printed circuit board. Note that there is an indicator light and a probe point for each of the fifty test points. The lamp corresponding to a particular test point will light if the test point is at a high voltage (logic "one"). In some cases, a panel with pulse stretchers between each of the test points and the lamps is used so that transient logic conditions can be detected.

The design of the motherboards allows the straight line buses to be broken at various points in the system. By using breaks and bypasses, the separate AFU's can have a local signal bus in addition to their connection to the global bus lines. To allow monitoring of the signals on these buses, a monitoring panel called a "wing" panel has been designed to insert in a connector on the outside of the motherboard much as a cable connector paddleboard does. Figure 6 shows the wing panel in more detail. Note that the wing panel has one indicator light and one switch for each of the 100 signal pins on the motherboard at the point of connection. The indicator lamp is lit if the associated signal line is

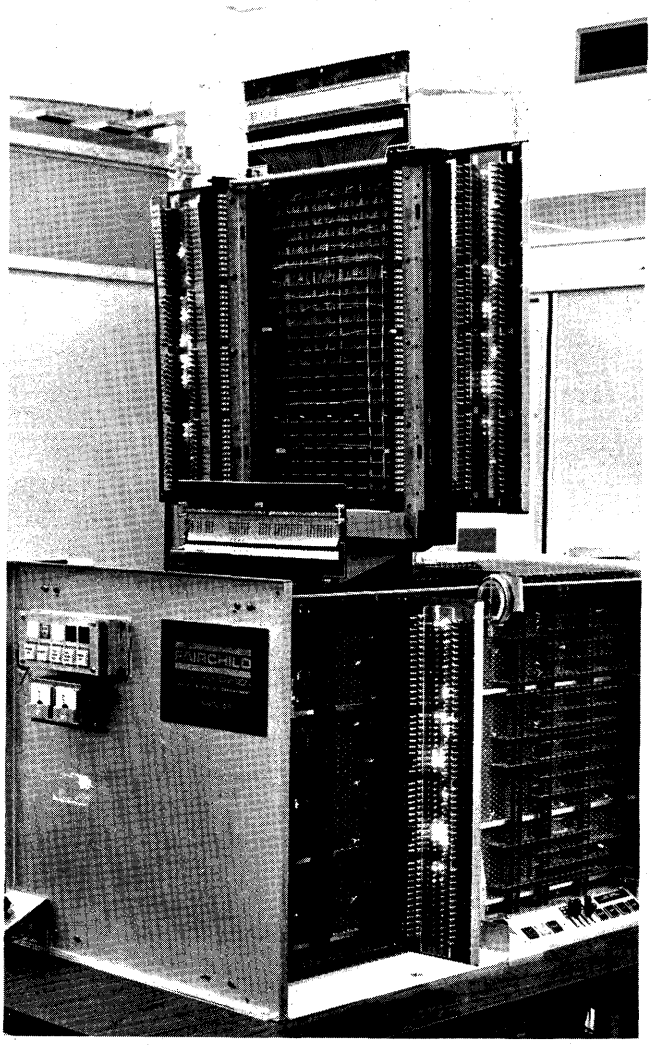

Figure 13—Typical SYMBOL system test configuration with board extender, test point and wing panels in place

at a high voltage and off otherwise. Two types of wing panels are available, a right wing panel and a left wing panel. The two types allow viewing of wings on each of the two motherboards from the same end of the SYMBOL system. One of the reasons that the bused-signal concept is successful is that the CTμL family provides a true wired-or capability. Because of this capability, a switch on a wing panel can be used to force (i.e., "or") a logic "one" on the associated signal bus on the motherboard. It should be noted that the test point panel and the wing panels are also standard two-sided printed circuit boards.

Unfortunately, it is necessary, from time to time, to probe signals on the logic board itself during operation of the system. To do this, a board extender was developed, again using two-sided printed circuit boards and simple mechanical parts. The wing panels can be connected to the board extender also. Figure 13 shows a typical system debugging setup with test point panels, wing panels and extender in place. Because of the system timing rules followed during design, no problems have been encountered due to the extra signal propagation time when a logic board is extended.

Logic board testing

In the early stages of the SYMBOL project, an automatic programmable logic board tester was constructed. However, it soon became clear that too great an investment of engineering time was required to perform successful tests. The major problem was that the boards being tested were not necessarily logically correct. An added complication was that the tests were programmed by hand. As a result, the tests required an excessive amount of time to program and as much time was spent debugging the test program as debugging the board under test.

A human-factors analysis of the specific operations required for functional board testing (in combination with the usually limited R and D budget) resulted in the development of a board tester used for most of the SYMBOL project. This tester (Figure 14) was designed to minimize the number of physical motions required during manual testing of prototype logic boards. In addition, every attempt was made to eliminate the need for any other instrumentation during testing. The same test point panel and wing panels used for system testing mount on the board tester and are used to force and/or monitor logic conditions at the 200 signal pins and fifty test points on the boards. Switch bounce is no problem because board testing is not dynamic in this tester.

During functional board test, signals on the logic board must also be traced and/or monitored. The tester control panel has been designed to help support these requirements. A single clock pulse with the same dynamic characteristics as seen in the SYMBOL system is generated by the CLOCK switch. The LOGIC test probe is used to monitor signal points on the board under test. The condition of the signal probed is indicated by both an audio and a visual signal. Three indicator lamps, one on the control panel and one on top of each of the two uprights, light when a logic "one" is probed. However, that is not sufficient to show that a particular signal line is electrically active or that the probe even made contact. Therefore, an audio signal is generated to indicate both logic one and logic zero via high and low frequencies; for an open circuit, no tone is generated. A set of lamps and switches is connected

through a cable to a fourteen pin package probe. This probe can be used both to monitor and to test a logic element. All lamps on the control panel have associated pulse stretchers to detect transient logic conditions.

During the initial testing of a logic board, continuity of signal traces is often suspect. The board tester can also assist in continuity checking. When the power to the board under test is turned off, the jack under the board power switch on the front panel is energized with a logic "one". A probe from this jack and the LOGIC probe can be used in place of an ohmmeter to check continuity. A similar operation can be done through use of the LOGIC probe and the package probe. The LOGIC probe generates an audible confirmation of continuity precluding the need for separate observation of a meter.

The ease of use of the board tester is best seen in the average time for testing. The automatic board tester averaged about two man weeks per board. The manual functional tester required about one man day per board. It is anticipated that when a system such as SYMBOL enters volume production it might be economical to return to the automatic tester since the logic design will have been debugged and the investment in tester programming could be amortized over the production run.

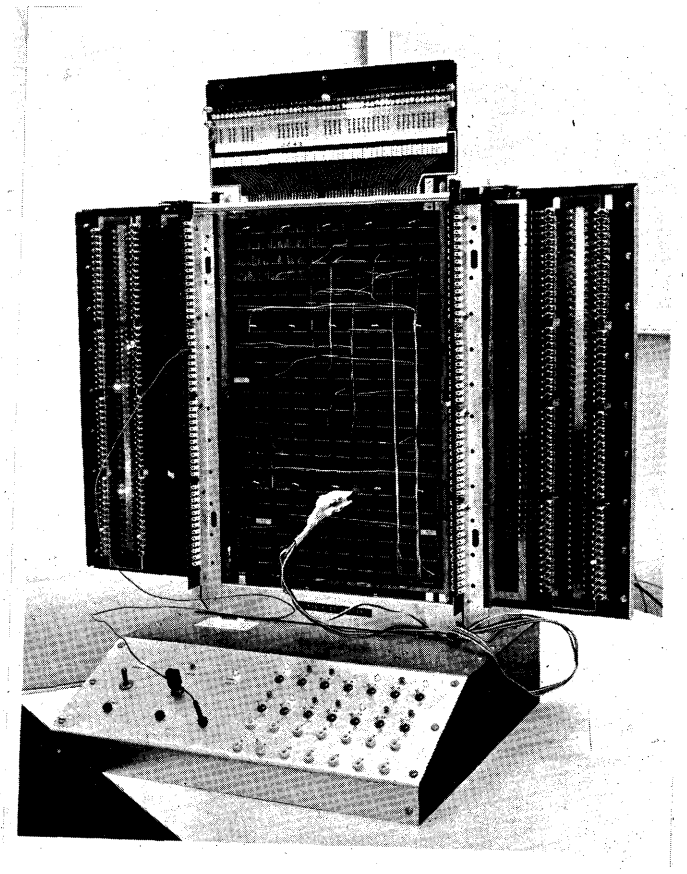

Figure 14—Manual, functional, logic board tester

System test

The problems encountered during system test on the SYMBOL system have been typical prototype test problems. The SYMBOL system is a synchronous design. Thus signals must propagate through whatever logic chains are required before the arrival of the subsequent clock. Although no timing rules were violated in the initial design, some logic corrections could be made less complex if the system timing rules could be relaxed. Also, some of the requirements of the initial system tester (described below) required a longer clock cycle. Thus, a second, slower, system clock speed was introduced at the outset.

Both automatic and manual aids are used for SYMBOL system test. Automatic testing aids are used to help isolate problems to a specific area in an AFU while manual aids are used to isolate the specific problem. Many of the manual test aids have already been shown. The board extender (Figure 13) allows a particular board to be accessible at its position in the system. The wing panels (Figure 7) can be mounted on the outside of the motherboards at positions which were specified by the designers during AFU design. The test point panels (Figure 12) monitor boards in the system. The normal complement of black boxes for monitoring the logic conditions of all pins on a package, for stopping the system clock on a logic condition, for determining how far operation proceeded through a sequential network before halting or forking, etc., has been constructed and is used during detailed logic debugging.

Extremely few areas of system test require the use of an oscilloscope. The electronics controlling the magnetic disk and magnetic core memories requires an oscilloscope to set up and verify timing. The portions of the system involved with various I/O clock frequencies such as peripheral controllers and transceivers also often require an oscilloscope. Very few other system problems have been discovered through the use of oscilloscopes. These few problems generally have been fabrication errors such as the case where the power supply filter capacitors were incorrectly inserted between ground and a signal line (resulting in *very* slow rise and fall times of the signal).

It is impractical to use manual techniques for system debugging. Such techniques would be analogous to single stepping an executive system program to find errors in loops buried deep within a software system.

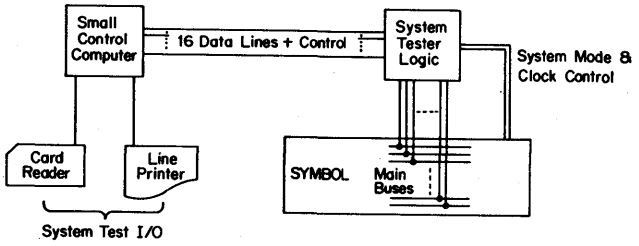

Figure 15—Programmable SYMBOL system test support configuration

Some kind of program trace must be generated. The analogy is particularly apt in the case of SYMBOL since the hardware includes most of the executive system. The SYMBOL system construction schedule was such that I/O equipment was one of the last things to become operational. Thus, self-diagnostics were impractical until late in the program. Some way of exercising and/or monitoring various AFU's and portions of the system automatically and of recording the results of these tests was absolutely necessary. In response to that need the SYMBOL system tester was developed (See Figure 15).

The system tester consisted of a small control computer with on-line disk storage, card reader, line printer and typewriter, interfaced to the SYMBOL main buses and to the SYMBOL mode and clock control lines. Since all SYMBOL system operation is coordinated via signals on the main signal bus, the control computer was programmed to substitute for any missing part of the system and to exercise any portion of the system accessible via the main bus. In addition, the main bus could be "watched" during independent system operation and desired data could be recorded. The discrepancy between the speed of the control computer with a limited bandwidth data channel and the SYMBOL clock speed was resolved by allowing the interface to turn off the SYMBOL clock temporarily when any data needed to be transferred to or from the main bus buffer register in the interface. Control of the clock in this manner significantly reduces the execution rate of the SYMBOL system while monitoring the actions of the system although this approach is considerably faster than simulation techniques. Except for real-time support logic, all logical sequences were executed in the same order with respect to each other no matter what the actual clock speed.

The general use of the system tester consisted of first initializing the memory with appropriate data, setting the system mode to AFU test or system test, starting the appropriate portion of the system, and monitoring the system operation via the line printer. Sixteen extra data lines, in addition to the SYMBOL main bus lines were provided to allow arbitrary signals in the system to be patched into the system tester. These lines could be connected to local buses, local control lines, etc. A language called DEBUG was developed to allow direct execution of any of the virtual memory operations and system supervision cycles under control of the small computer. The system supervision cycles allowed starting and stopping of the various AFU's in the system. An automatic memory exercising mode was included. Any arbitrary pattern could be written into all words, read and checked. Any errors detected were automatically listed on the line printer. The "watching" of the bus signals was done in a TRACE mode. During TRACE, all memory operations performed by a particular AFU and/or inter-AFU control communication were listed on the line printer. Since the control computer was programmable, special problems such as illegal use of particular memory words could be tracked through the use of special monitoring programs.

To provide independent maintenance and debugging capability, a substitute for the programmable test system was devised. An additional AFU called the Maintenance Unit (MU) was defined and implemented. Figure 16 shows the final system configuration of SYMBOL with the Maintenance Unit. I/O equipment from the remote interactive batch terminal is used as the input/output medium. A special punched card format (produced by the SUPERBUG language processor) was defined and is used as input to the

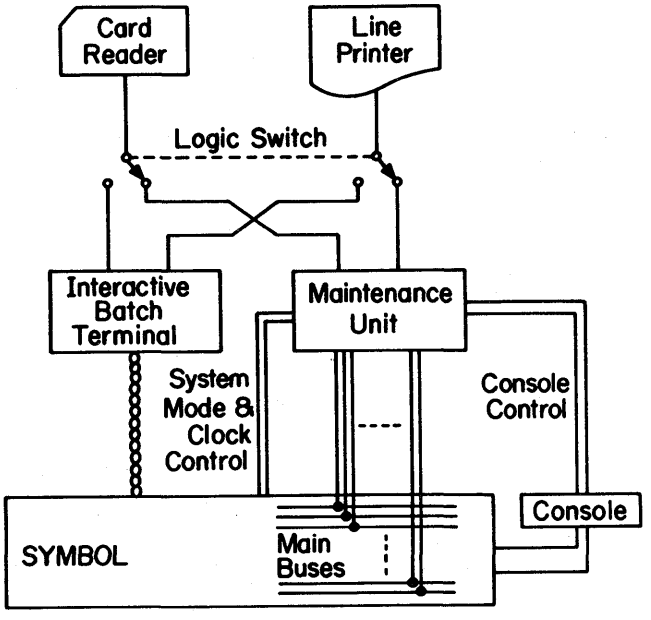

Figure 16—SYMBOL system maintenance unit configuration

DEBUG operations which are hard wired into the MU. The MU implements a majority of the most frequently used features of the programmable system tester and does not implement those features which were relatively unused. The SYMBOL control console also controls the MU.

The use of the limited bandwidth channel from the SYMBOL main buses to the control computer in the system tester proved the feasibility of performing remote testing of complex computing equipment. No good solution has yet been discovered for isolating errors in peripheral equipment using these techniques. The small number of system interconnections has been instrumental in making this system testing approach possible.

CONCLUSIONS

The SYMBOL project has developed a generally useful and inexpensive technology which includes system packaging, computer-aided engineering design and circuit board and system testing techniques.

The system packaging techniques use two-sided printed circuit boards for both signal and power distribution intraconnections. A cam-operated zero-insertion force, high pressure connector gives reliable but inexpensive pluggable connections. All system level interconnections are made on two-layer printed circuit motherboards. No wire wrap or other forms of wired connections are used. The cam-operated contacts solder directly onto the motherboards for mechanical stability and electrical reliability. Simple forced air cooling is used. Inexpensive power is provided by a high current main supply and a low-voltage, lower-current shunt supply.

A complete engineering design package using computer aids was developed for the project. From logic equation input, electrical and timing checks are made (human aided), factoring and functional unit selections are made, automatic placement is accomplished, wire routing is done, and finally, printed circuit board artwork is automatically generated.

The testing techniques allow single circuit boards, several boards, a functional unit, several functional units, or the complete system to be exercised. Single boards may be tested in a separate "board tester." Any board in the main frame of the system may be placed on a board extender for scoping, etc. The parallel line motherboards permit "wings" to be placed at any desired main frame location for observing or controlling logical states. The main frame can be driven by a small computer to simulate operating conditions at any level from a single board up to the complete system. A programmed debug package was developed for the small computer to activate the system and to help diagnose trouble.

These SYMBOL technologies have already proven useful in the implementation of the following projects:

- Minus; a smaller-than-mini computer with a 512 word, 9 bit semiconductor memory,
- SYMBOL Terminal; an interactive, remote-batch terminal;
- LSI Memory; the 2048 word × 64 bit production bipolar memories used for the ILLIAC IV computer Process Element Memories,
- Board Testers; the memory and SYMBOL logic board testers,
- Automatic AC Functional Memory Tester; a special tester for AC functional testing of LSI memory components

We believe that, taken together, these techniques will be very useful in low-cost commercial computing systems for years to come.

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