# Performance and power dissipation analysis for CCD memory systems

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## ABSTRACT

In CCD memory systems a tradeoff exists between the frequency at which the memory system is operated and the power dissipation. The higher the frequency of operation, the lower is the service time and the higher is the power dissipation. A close look at the initial cost of the CCD memory system and the cost of maintaining these memory systems will show that the cost of maintenance for a year is nearly equal to the initial cost. This high cost necessitates an analysis of the CCD memory system design for service time and power dissipation.

In this analysis three different states called the Access, Refresh, and Idle states are defined for a CCD memory system. Each state is characterized by a frequency and five different modes of operations are defined depending on the relation between the frequencies. Average service time and power dissipation equations are then derived and each mode is analyzed. Contrary to the normal belief that the power dissipation increases with access frequency, it is shown that for certain modes the power dissipation is constant and is independent of frequency. Finally, a figure of merit is defined and the different modes are compared.

## INTRODUCTION

In the last few years, extensive work has been done on Charge Coupled Devices (CCD's). These devices have a potential of becoming basic building blocks to construct memories for digital computers. Many papers are available that analyze and propose designs for the basic component and its layout on the chip.[1-3] Very little analysis is available on the use of the chip in a memory system. It is predicted that the cost/bit for CCD memory systems will be 15 to 30mø/bit[4] and power dissipation of 20 uw/bit. Using a rule of thumb of 1 mø/uw/year for the operation of semiconductor memory systems stated by Morton,[5] it is evident that the initial cost and the operating cost for a year are equal for CCD memory systems even when operated at low frequencies. The situation would be still worse at higher frequencies.

Here we will analyze some aspects of the CCD's pertaining to their use in a memory system design. The analysis will show the tradeoffs of operating and using different devices and an insight into the design of the chip.

## CCD CHIP PARAMETERS

Most common types of CCD chips being designed are of the closed loop shift register type. Therefore, we will analyze such a chip. A typical chip will have S shift registers with $N_t$ cells in each shift register (Figure 1). The design of the device will determine the refresh time ($t_r$), which is the maximum allowable time before which a new refresh cycle must be started. Usually a refresh amplifier is available after every $N_r$ cells, and $N_t$ is an integer multiple of $N_r$, with $N_r$ and

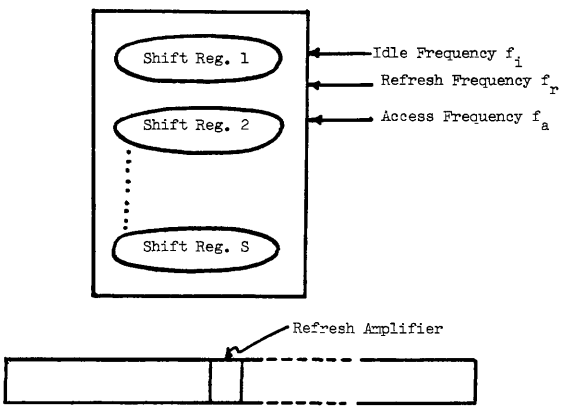


Figure 1—Schematic of a closed loop shift register type CCD chip

| Chip Parameter | Symbol | Typical Values |
|---|---|---|
| Shift Registers | S | 32~128 |
| No. of Cells/Shift Register | $N_t$ | 64~256 |
| No. of Cells between Refresh Amp. | $N_r$ | 32~256 |
| Refresh Time | $t_r$ | 2msec. and above |

TABLE I—Various Chip Parameters and Their Typical Values

$N_t$ being powers of two. Some typical values for S, $N_t$, $N_r$ and $t_r$ are given in Table I.

## MODES OF OPERATION

With the above mentioned basic parameters for the chip a memory system can now be designed to operate in three different states. The three states are the Access state when the data is being accessed (read or written) from the chip, Idle state in which the chip is doing nothing and the Refresh state in which the data in the shift register is being refreshed.* The three states can be characterized by having three different frequencies: Access frequency $f_a$, Idle frequency $f_i$ and Refresh frequency $f_r$. By definition, a memory system can be in the Access state and Refresh state at the same time if the frequencies for these two states are the same. A state transition diagram for the three states is shown in Figure 2.

In evaluating the performance of the chip, the following assumptions will be made:

(1) The refresh state has priority over both the access and idle state, whereas the access state has priority over the idle state.
(2) The data transfer in a shift register is always initiated from the bit addressed as the first bit. This is not always necessary and different assumptions can be treated as special cases and the analysis pursued here modified accordingly.
(3) A new access for data is not made when a previous access is pending. This assumption implies a buffer in which all the requests to the memory system are stored and serviced with some scheduling strategy.
(4) There is an equal probability that the refresh, idle or access states are started at any bit in the shift register.
(5) The power dissipation is proportional to the frequency at which the data cells are being moved.[6] Notice that the power dissipation of the peripheral circuitry, drivers and the shift register array is a function of the frequency.[1]
(6) The refreshing and accessing can be done simultaneously, if, and only if, the refreshing frequency ($f_r$) and the accessing frequency ($f_a$) are the same. This implies that the interface to the CCD memory system always transfers or receives data at the same frequency.
(7) Once a data transfer is started all the bits in a shift register must be transferred.

* The Access state may be further divided into an Aligning state and a Transfer state. Presently, we will not make any distinction and the analysis made here can be easily extended to that case.

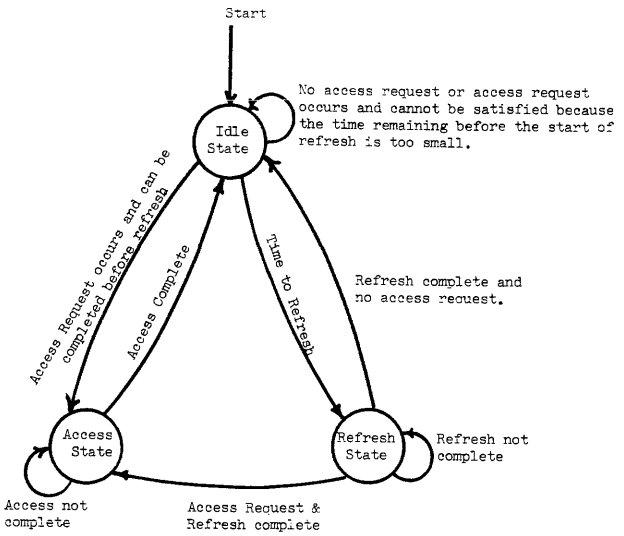


Figure 2—State and transition diagram for the different states of CCD memory operation

By choosing different values for the three frequencies $f_a$, $f_r$ and $f_i$, the chip and hence, the memory system can be operated in five different modes (Table II) requiring one, two, or three clocks. Notice that the number of clocks required is an indication of the complexity of control required by the memory system and, therefore, in some sense defines the cost for control circuitry.

The five modes of operation and their implications are tabulated in Table II. Mode 5 is the most general mode of operation and the other modes can be considered as a limiting case of this mode. For example, mode 3 can be considered as a limiting case of mode 5, when $f_i$ tends to $f_r$.

Before evaluating the different modes, the implications of the modes of operation on a memory system design are qualitatively discussed. In a semiconductor memory system design some major parameters of interest are: (a) power dissipation which influences the cost of maintaining the memory, (b) access and service times which influence the performance of the system, (c) the interface requirements such as, the data width and data rate, and (d) the control complex-

| MODE | FREQUENCY | METHOD OF OPERATION |
|---|---|---|
| 1 | $f_a = f_r = f_i$ | Continuous Refresh<br>Most common mode of operation in the near future. |
| 2 | $f_a \neq f_r$<br>$f_a = f_i$ | Burst Refresh<br>Possible low access frequency due to interface requirements. |
| 3 | $f_a \neq f_r$<br>$f_i = f_r$ | Possible high Access rate. Useful when the memory is expected to remain idle for a large percentage of the time. |
| 4 | $f_a \neq f_i$<br>$f_a = f_r$ | Zero idle frequency is possible. Minimum access frequency determined by the lowest allowable refresh frequency. |
| 5 | $f_a \neq f_i \neq f_r$ | Zero idle frequency possible. Interface requirement of low access frequency can be satisfied. |

TABLE II—Possible Modes of Operations for a CCD Chip

ity which determines the difficulty and the amount of overhead involved in the design of the memory system.

Mode 1 is a continuous mode of operation in which all the bits are moving all the time and has the simplest control circuitry. This will be the most common mode of operation in the early systems.

Mode 2 requires two frequencies and, therefore, has a control complexity higher than Mode 1. One method of operating in Mode 2 would be to use low idle and access frequencies and high refresh frequency. Such a mode is applicable when an external device with low data rate is interfaced with CCD's and real time transfers are made. Also, when memory is operated in a 'vertical mode',[7] as is recommended for CCD device,[8] it is necessary to shift the bits at a low frequency.

Mode 3 of operation has equal idle and refresh frequency and either low or high access rate. The control complexity is the same as in Mode 2. It is necessary that $f_r (=f_i) > N_r/t_r$. Intuitively, such a design is attractive only when the memory system is expected to remain in the idle mode for a high percentage of the time. Mode 4 of operation is again as complex as Mode 2 and Mode 3 and can be operated with burst refresh and zero idle frequency. Finally, Mode 5 is the most general mode of operation and will have the maximum control complexity. A practical application of this would be: (1) when the system is idle most of the time, (2) the external requirement necessitates low data rate, and (3) burst refresh is to be used to refresh the memory. The analysis later will show that only some of these modes are advantageous from the performance and power dissipation considerations.

On the following pages, equations for Mode 5 of operation will be developed. Then the equations for the other modes of operation will be determined as a limiting case of Mode 5.

## ANALYSIS OF SERVICE TIME

Service time is defined as the time elapsed between the moment a request is made to the memory for some information to the moment when all the information is delivered.

When a request is made to a CCD memory system for particular information, the bits in the shift registers have to be shifted until the shift register is positioned at bit 1 under the read/write circuit. The time required to do this will be called the access time ($t_a$). Once the shift register has been positioned then the

data may be transferred and the time required to transfer the data will be called the transfer time ($t_t$). The service time ($t_s$) is the time required to service a request and is given by

$$t_s = t_a + t_t$$

and the average value of service time ($\bar{t}_s$) is

$$\bar{t}_s = \bar{t}_a + \bar{t}_t$$

Assume that $t_a$ is a random variable and can be determined as a sum of three random variables given below.

$X_r$ = random variable that represents time spent in refreshing when a service request is made.

$X_a$ = random variable that represents time spent in aligning the shift register to bit 1 when a service request occurs.

$X_d$ = random variable that represents time lost when a service request cannot be satisfied because the refresh cycle has to be started before all the bits in the shift register are transferred.

Then

$$t_a = X_r + X_a + X_d$$

and because $X_r$, $X_a$ and $X_d$ are independent random variables, we have

$$\bar{t}_a = \bar{X}_r + \bar{X}_a + \bar{X}_d$$

We have to determine the values of $X_r$, $X_a$ and $X_d$. The probability density function of $X_r$ is given in Figure 3. From the figure

$$\bar{X}_r = \frac{1}{2}\left(\frac{N_r}{f_r}\right)^2 \cdot \frac{1}{t_r}$$

The value for $X_a$ is simple to calculate and is given by

$$\bar{X}_a = \frac{1}{2}\frac{(N_t - 1)}{f_a} \approx \tfrac{1}{2}(N_t/f_a) \qquad \text{[for large } N_t\text{]}$$

To calculate $\bar{X}_d$, notice that if a request arrives at a time when the shift register is at position N, then the minimum time required to access and transfer the block is given by

$$\frac{N_t + (N_t - X)}{f_a} = \frac{2N_t - X}{f_a}$$

Because the probability that a request occurs at any particular bit is the same, the expected value of $X_d$ is (Figure 4) derived as

$$\bar{X}_d = \sum_{X=1}^{N_t} \frac{1}{N_t t_r}\left[\frac{1}{2}\frac{(2N_t - X)^2}{f_a^2} + \frac{N_r(2N_t - X)}{f_r f_a}\right]$$

$$= \frac{1}{2t_r f_a^2}\left[\frac{7}{3}N_t^2 - \frac{3}{2}N_t + \frac{1}{6}\right] + \frac{N_r}{N_t t_r f_r f_a}\left[\frac{3N_t^2 - 2N_t}{2}\right]$$

Notice that for large values of $N_t$

$$\left(\frac{3}{2}N_t - \frac{1}{6}\right) \ll \frac{7}{3}N_t^2 \text{ and } 2N_t \ll 3N_t^2$$

$$\bar{X}_d \approx \frac{7}{6t_r}\left(\frac{N_t}{f_a}\right)^2 + \frac{3N_t N_r}{2t_r f_r f_a}$$

Then the average value of $t_a$ is

$$\bar{t}_a = \frac{N_t}{2f_a} + \frac{1}{2t_r}\left[\left(\frac{N_r}{f_r}\right)^2 + \frac{7}{3}\left(\frac{N_t}{f_a}\right)^2 + \frac{3N_t N_r}{f_a f_r}\right]$$

For a shift register of length $N_t$ and transfer frequency $f_a$

$$\bar{t}_t = \frac{N_t}{f_a}$$

Therefore, the average value of the service time is

$$\bar{t}_s = \frac{3N_t}{2f_a} + \frac{1}{2t_r}\left[\left(\frac{N_r}{f_r}\right)^2 + \frac{7}{3}\left(\frac{N_t}{f_a}\right)^2 + \frac{3N_t N_r}{f_a f_r}\right]$$

## ANALYSIS OF POWER DISSIPATION

In CCD's power dissipation is proportional to the frequency.[6] Amelio[1] gives equation for the average power dissipated ($P_d$) on chip for a data frequency f as

$$P_d = 2N(0.2 \times 10^{-12})f$$

where $P_d$ is the power dissipated due to a shift register of N bits being shifted at a frequency f.

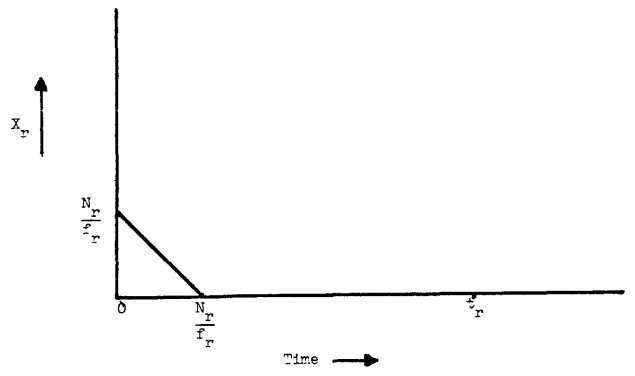


Figure 3—Probability density function of $X_r$

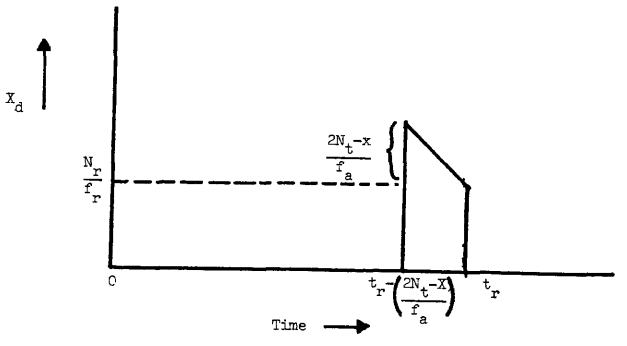


Figure 4—Probability density function for $X_d$ when a service request is made at bit position x

Because the CCD electrodes have a large capacitive load, the power dissipated in the drivers is much larger and is given by

$$P_d = CV^2f$$

where C is the capacitive load, and V is the voltage applied.

We will represent the constant of proportionality between power dissipation and frequency as K. Usually the power dissipation due to the drivers is much larger than the power dissipation due to the shift register array and hence, $K = CV^2$.

Then if $t_1, t_2, t_3 \ldots t_n$ are different time intervals in which frequencies $f_1, f_2, \ldots f_n$ are applied to the chip, the average power dissipation is given by

$$\bar{P}_d = K\frac{t_1f_1 + t_2f_2 + \ldots\ldots\ldots + t_nf_n}{t_1 + t_2 + \ldots\ldots\ldots + t_n}$$

The three different states of the CCD memory systems will determine three different time intervals and three different frequencies.

These are:

(1) Total time spent in refresh state ($T_r$) and refresh frequency $f_r$.
(2) Total time spent in idle state ($T_i$) and idle frequency $f_i$.
(3) Total time spent in access state ($T_a$) and access frequency $f_a$.

Then the average power dissipation ($\bar{P}_d$) is given by

$$\bar{P}_d = K\frac{f_r\bar{T}_r + f_i\bar{T}_i + f_a\bar{T}_a}{\bar{T}_r + \bar{T}_i + \bar{T}_a}$$

To determine the average values for the different times we will consider a basic period as the time from the beginning of one Refresh cycle to the beginning of the next Refresh cycle. Then

$$\bar{T}_r = \frac{N_r}{f_r}$$

The remaining time in a cycle is the sum of the total idle time and the total service time. Therefore

$$T_a + T_i = \left(t_r - \frac{N_r}{f_r}\right)$$

$$\bar{T}_i = \left(t_r - \frac{N_r}{f_r}\right) - \bar{T}_a$$

To determine the average total time spent in servicing requests ($\bar{T}_a$) assume that in any given cycle there is a possibility of maximum of s accesses. Then let

p(j) = probability that j accesses are made

(j = 0, 1, 2 ... s)

The average time spent when one access is made is already determined and is given by $\frac{3N_t}{2f_a}$ and, therefore,

$$T_a = \sum_{j=0}^{s} j\,p(j)\frac{3N_t}{f_a}$$

$$\text{Let } Q = \sum_{j=0}^{s} j\,p(j)$$

Intuitively Q represents the average number of requests per period.

Then

$$\bar{T}_a = \frac{3N_tQ}{2f_a}$$

and

$$\bar{T}_i = t_r - \frac{N_r}{f_r} - \frac{3N_t}{2f_a}Q$$

Adding the various terms and rearranging gives the average power dissipation for mode 5 of operation as

$$\bar{P}_d = K\left\{f_i + \frac{N_r}{t_r}\left(1 - \frac{f_i}{f_r}\right) + \frac{3N_tQ}{2t_r}\left(1 - \frac{f_i}{f_a}\right)\right\}$$

This general analysis for average service time and power dissipation can now be applied to each mode of operation.

## ANALYSIS OF DIFFERENT MODES

In this section we will analyze each mode of operation. The service time and power dissipation equations for the different modes derived from the analysis of general Mode 5 are given in Table III. The graph in Figure 5 denotes the average service time and power dissipation for Mode 1 of operation and the graphs in Figures 6 to 10 denote the percentage improvement in average power dissipation and percentage degradation in service time for Modes 2 to 5 over that of Mode 1 of operation.

Mode 1 will be the most usual mode of operation in the near future. A plot of access frequency vs service

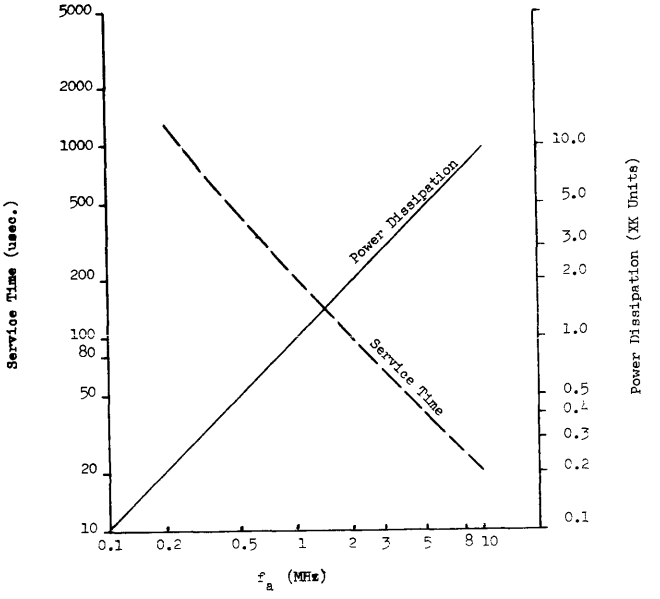


Figure 5—Graph of service time and power dissipation vs. access frequency for mode 1 of operation

| MODE | FREQUENCY | SERVICE TIME | POWER DISSIPATION | REMARKS |
|---|---|---|---|---|
| 1 | $f_a=f_r=f_i$ | $\frac{3N_t}{2f_a}+\frac{1}{2t_r}\left\{\frac{3N_r^2+7N_t^2+9N_tN_r}{3f_a^2}\right\}$ | $Kf_a$ | Power Dissipation directly proportional to frequency |
| 2 | $f_a \neq f_r$<br>$f_a = f_i$ | $\frac{3N_t}{2f_a}+\frac{1}{2t_r}\left\{\frac{N_r^2}{f_r^2}+\left[\frac{7}{3}\right]\frac{N_t^2}{f_a^2}+\frac{3N_tN_r}{f_af_r}\right\}$ | $K\left\{f_a+\frac{N_r}{t_r}\left[1-\frac{f_a}{f_r}\right]\right\}$ | Very little advantage over Mode 1 for both service time or power dissipation |
| 3 | $f_a \neq f_r$<br>$f_r = f_i$ | Same as Mode 2 | $K\left\{f_r+\frac{3N_tQ}{2t_r}\left[1-\frac{f_r}{f_a}\right]\right\}$ | Values of $f_i$=1 to 3Mcycles/sec. are advantageous from both service time and power dissipation considerations |
| 4 | $f_a \neq f_i$<br>$f_a = f_r$ | Same as Mode 1 | $K\left\{\left[1-\frac{2N_r+3N_tQ}{2f_at_r}\right]f_i+\frac{2N_r+3N_tQ}{2t_r}\right\}$ | For $f_i = 0$ and a given value of Q, the power dissipation is constant |
| 5 | $f_a \neq f_r \neq f_i$ | Same as Mode 2 | $K\left\{f_i+\frac{N_r}{t_r}\left[1-\frac{f_i}{f_r}\right]+\frac{3N_tQ}{2t_r}\left[1-\frac{f_i}{f_a}\right]\right\}$ | For $f_i$=0 and a given value of Q, the power dissipation is constant. No advantage over Mode 4 unless $f_a \neq f_r$ due to interface requirements |

TABLE III—Service Time and Power Dissipation Equations for Different Modes of Operation

time is given in Figure 5. The dominating factor for service time in the equation given in Table III is $3N_t/2f_a$. At small values of access frequency ($f_a$= 200KHz) the contribution due to the second term is quite high (about 40 percent), whereas at moderate values ($f_a$=1MHz) it is about 10 percent and at high values it is negligible (less than 1 percent). The second term can be decreased by increasing $t_r$. $N_r$ has no appreciable influence on the service time. The power dissipation is seen to be directly proportional to frequency.

Again, for Mode 2, the dominant term for service time is $3N_t/2f_a$. The power dissipation equation shown in Table III has two terms. The first term is the same as Mode 1 and the second term can be made negative by making $f_a > f_r$.

Figure 6 shows the percentage improvement in power dissipation and percentage degradation in service time over Mode 1 vs the access frequency for different values of $f_r$. The results show that either the degradation in service time is quite high or power dissipation improvement is quite low. A similar analysis for various values of $N_r$ will show the same conclusion. Therefore, this mode of operation has little advantage over Mode 1. The service time equation for Mode 3 is the same as that for Mode 2 but the power dissipation equation is different.

Figure 7 shows the percentage improvement in power dissipation and percentage degradation in service time vs the access frequency for various values of Q. Service time is independent of Q but the improvement in power dissipation is reduced as Q increases. The difference in $\bar{P}_d$ improvement between the lowest and the highest value of Q is quite small and is of the order of 10 to 15 percent. Note that there is a rapid improvement in power dissipation from 1 to 5MHz and then the improvement tapers off. The worst case service time degradation is about 8 percent. Therefore, a good cut-off point for this mode of operation is around 5MHz when the service time degradation is about 5 percent.

The variation of percentage improvement in power dissipation and degradation in service time vs the access frequency for various values of $f_r$ is shown in Figure 8. It shows that high values of $f_r$ are disadvantageous from both power dissipation and service time point of view. Generally, this mode is better than Mode 2 of operation.

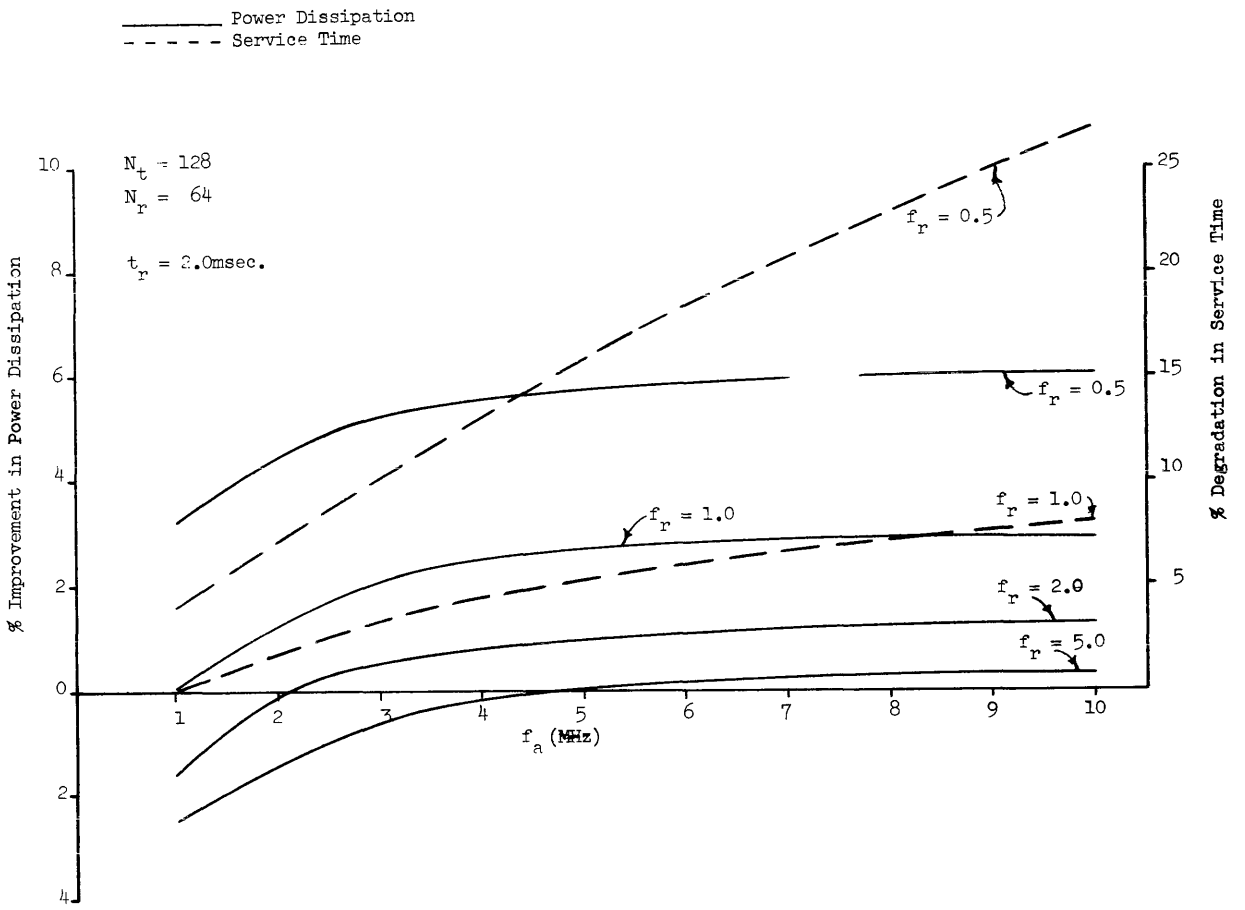


Figure 6—Percentage improvement in power dissipation and percentage degradation in service time vs access frequency for mode 2 of operation

In the Mode 4 of operation the average service time equation is the same as Mode 1. Physically, this is understandable due to two reasons: the idle frequency moves the information bits without doing any useful work and there is an equal probability of a service request at any bit.

Power dissipation equation has two terms, one proportional to the frequency $f_i$ and the other a constant. By making $f_i$ zero, and if the different parameters of a chip (e.g. $N_a$, $t_r$, etc.) are given, then power dissipation is only dependent on Q and is independent of the access frequency. Notice that increasing $t_r$ reduces the power dissipation. This is again physically understandable, since the chip will have to be refreshed less regularly. The power dissipation also can be decreased by decreasing $N_r$ or $N_t$. Notice that the second term can never be negative. Therefore, the minimum value of power dissipation occurs when $f_i=0$. Because the most interesting point is $f_i=0$, we will further analyze this mode at this operating point. With $f_i=0$ the power dissipation for Mode 4 and Mode 5 are the same.

Figure 9 shows the percentage improvement in power dissipation and percentage degradation in service time vs the access frequency for various values of Q for Modes 4 and 5. The percentage improvement in power dissipation increases as access frequency increases. Increase in the value of Q decreases the percentage power dissipation. For smaller values of access frequency ($f_a=1$ to 3MHz) the slope of the power dissipation curve is quite high (40) whereas at higher values it is small (2). The power dissipation improvement for values of $f_a$ greater than 3.5 to 4MHz is marginal. Therefore, an optimal point of operation is $f_a=3$MHz for small values of Q and $f_a=4.5$ to 5MHz for large values of Q.

Finally, the following observations can be made:

(1) It is possible to operate a memory system at the highest possible frequency with about 90 percent improvement in power dissipation over Mode 1 of operation.

(2) It is advisable to make the time between refreshing ($t_r$) as large as possible both to decrease the average power dissipation and service time.

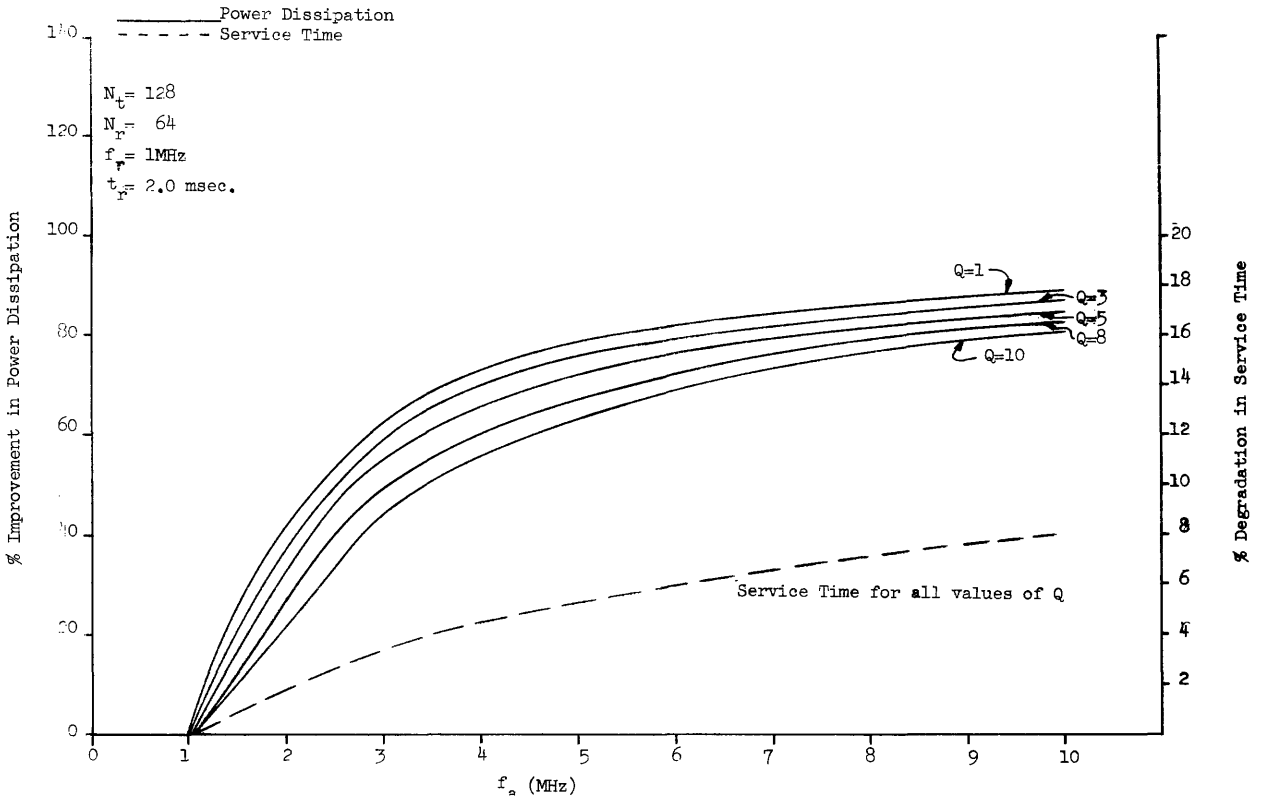


Figure 7—Percentage improvement in power dissipation and percentage degradation in service time for various values of Q for mode 3 of operation

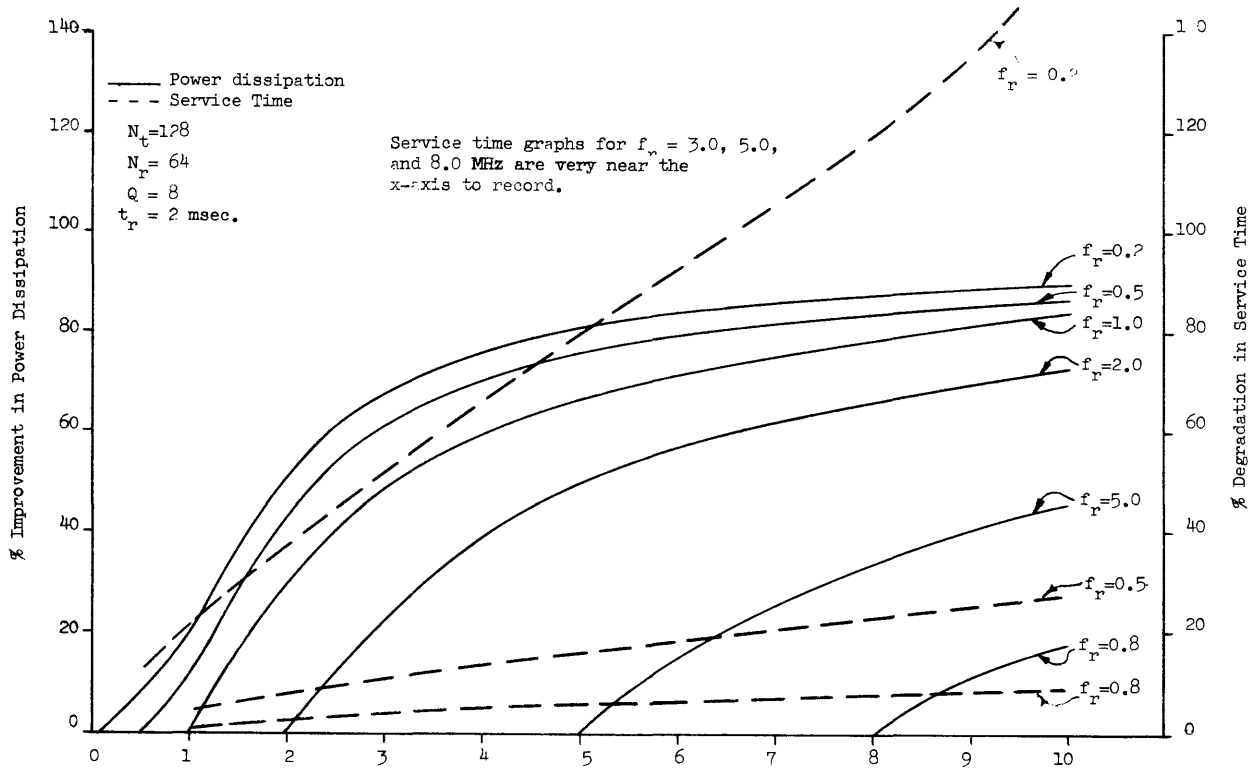


Figure 8—Percentage improvement in power dissipation and percentage degradation in service time vs access frequency for various values of $f_r$ for mode 3 of operation

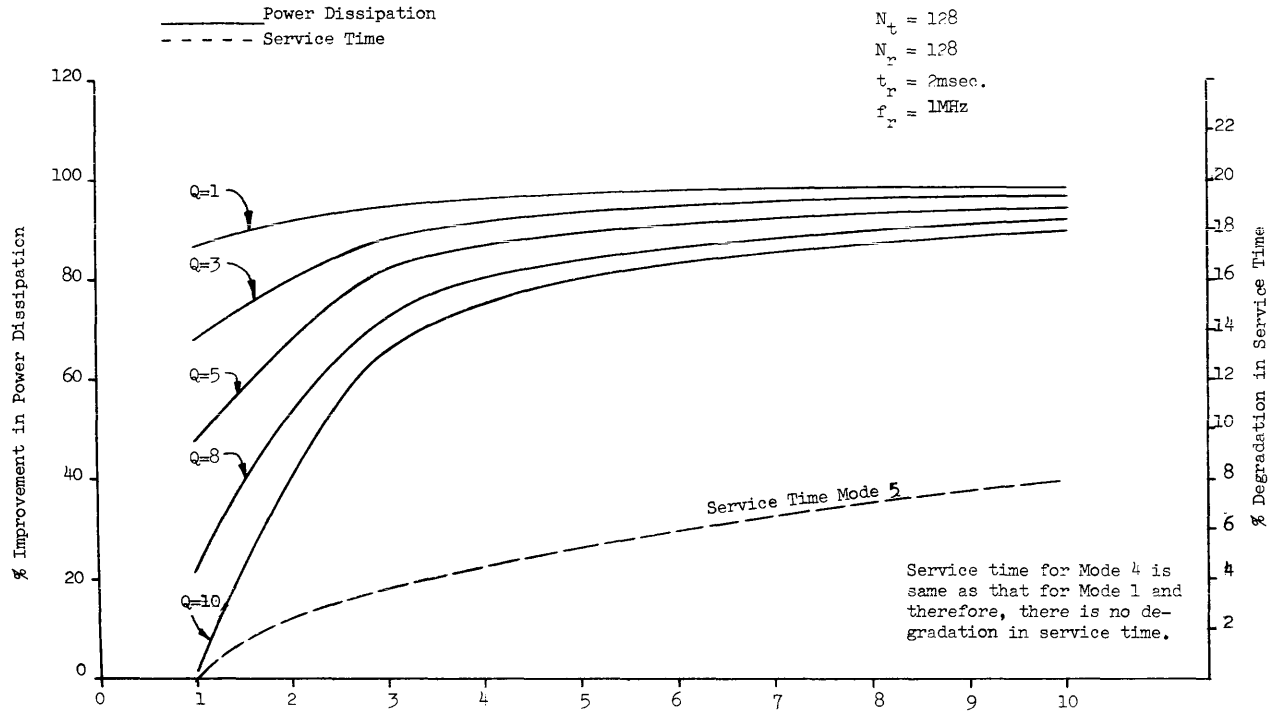


Figure 9—Percentage improvement in power dissipation and percentage degradation in service time for mode 4 and mode 5 of operation

(3) The interesting modes of operation are derived by making idle frequency zero. This is intuitively valid because moving the bits in a shift register during idling does not have any advantage either from performance or from power dissipation viewpoint.

## COMPARISON OF DIFFERENT MODES

In this section we will compare the different modes of operation. To make a comparison we will define a figure of merit (Fgm) as the number of possible services per unit time per unit power dissipation.

$$\text{Fgm} = \frac{1}{\text{average service time} \times \text{average power dissipation}}$$

Thus, a mode that has higher Fgm is better than one that has a lower Fgm.

In Figure 10 we draw a graph of Fgm vs. Access frequency for various modes. The typical values chosen for $N_t$, $N_r$, and $t_r$ are 128, 64 and 2msec. The Refresh frequency, whenever it is different from Access frequency is chosen as 1MHz. The Mode 1 and Mode 2 are independent of Q, whereas Modes 3, 4, and 5 are dependent on Q and, therefore, graphs are drawn for various values of Q.

Mode 2 has the worst Fgm for all access frequencies and, therefore, is the worst mode of operation. Mode 1 has a typical Fgm of about 5 and is constant over all frequencies. For values of $f_a > 1$MHz Modes 3 and 4 and Mode 5 are better than Mode 1 for all values of Q up to 10. For $f_a = 1$MHz and values of Q=1,5, Mode 1 of operation is better than Mode 3. Also, for Q=10 Mode 1 is better than Mode 4 or Mode 5. But notice that for Q=10 Mode 3 is the best mode of operation for small values of $f_a$. At higher values of $f_a$ Mode 4 is the best mode, closely followed by Mode 5 for all values of Q. The Fgm for Modes 3, 4 and 5 is reduced as Q increases. The reduction for Modes 4 and 5 is much higher than that for Mode 3.

Table IV lists the various modes and a qualitative comparison of these modes with respect to control complexity and cost of design.

## CONCLUSIONS

Memory systems built with CCD's are shown to have three states of operation: The Access state, Refresh state and Idle state and each state has a frequency associated with it. Three different modes of operation are defined and average service time and average

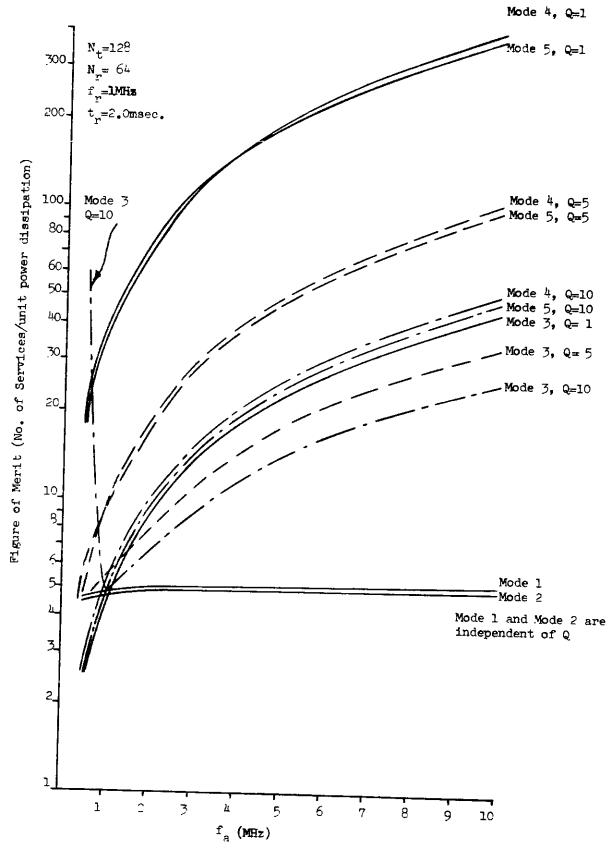


Figure 10—Figure of merit vs access frequency for various modes of operation

TABLE IV—A Qualitative Comparison of Different Modes of Operation

| MODE | NO. OF CLOCKS REQUIRED | CONTROL COMPLEXITY | COST OF DESIGN | REMARKS |
|---|---|---|---|---|
| 1 | 1 | Minimum | Minimum | Simplest mode of operation |
| 2 | 2 | Moderately Low | Moderate<br>Lower than Mode 4 if $f_i \neq 0$ | Worst mode of operation |
| 3 | 2 | Moderately High | Moderate | For small $f_a$ ($f_a$ <1MHz) .<br>A good mode of $^a$operation |
| 4 | 2 if $f_i \neq 0$<br>1 if $f_i = 0$ | High if $f_i \neq 0$<br>Low if $f_i = 0$ | Low if $f_i = 0$ | For $f_a$ > 1MHz the best mode of operation |
| 5 | 3 if $f_i \neq 0$<br>2 if $f_i = 0$ | Maximum | Maximum | Best mode of operation except for mode 4 |

power dissipation equations for a general case of operation are derived. Equations for each mode are then derived as a limiting case of these general equations. The different modes are analyzed individually and, finally, a comparison between the different modes is made by defining a figure of merit. An interesting result derived is that the power dissipation is constant and is independent of Access frequency for Modes 3 and 4 when they are operated with $f_i = 0$. Mode 4 is shown to be the best mode of operation. A simple qualitative comparison is finally made for the cost of implementation.

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