Superconducting memories employing Josephson devices

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INTRODUCTION

Experimental superconducting Josephson devices being investigated for use in digital logic and memory circuits have been demonstrated to switch in the 10 to 100 picosecond (1 picosecond = 10^{-12} sec) range. Projections based on the operation of individual logic circuits indicate that they may surpass semiconductor circuits in very high performance CPU's. This potential is based on the fact that these circuits dissipate extremely little energy, on the order of 10 to 1000 attojoules (attojoule = 10^{-18} joule), while operating with subnanosecond delays. It should, therefore, be possible to package Josephson devices very densely and interconnect them by properly terminated superconducting transmission lines so that the fast switching speed of individual circuits is retained throughout large logic networks.

Ultrafast CPU's need, of course, suitable memories, which are fast enough to provide requested data quickly and which are large enough to ensure that high throughput is sustained. It is likely that memory hierarchies will be needed to satisfy these requirements. Improved performance of the individual memories forming these hierarchies will, however, be required also, to avoid excessive "tuning" of such hierarchies, i.e., good performance for only narrow classes of computational tasks. The potential of Josephson devices to provide such memories and measures to "detune" such hierarchies will be discussed in this paper.

JOSEPHSON DEVICES AND CIRCUITS

Devices

Based on superconductivity and electron tunneling effects discovered in the early 1960's by Josephson[1] and Giaever,[2] one may construct a thin film switching device as shown in Figure 1a. Two thin film strips of superconducting material, e.g., Pb, are deposited in a partially overlapping arrangement but separated from each other by an extremely thin "native" oxide tunnel barrier of about 30 Å (1 Å = 10^{-8} cm) thickness. A small voltage of a few millivolts will cause a tunneling current of single electrons through the insulating oxide barrier by virtue of the quantum mechanical tunnel effect. The current-voltage relation is linear, as shown in the current-voltage plot of Figure 1b, as long as the temperature T of the structure is above the critical temperature T_c of the film strips (in case of Pb films $T_c = 7.2°K$). One may represent this behavior by a voltage independent so-called normal tunnel conductance.

If the structure of Figure 1a is immersed in liquid helium, which maintains a temperature of 4.2°K under atmospheric pressure, both film strips are superconducting and the current-voltage relation undergoes two characteristic changes, as shown in Figure 1c. First, a supercurrent,[3] made up of paired electrons (Cooper pairs) which are formed below T_c and are responsible for all superconducting effects, can flow through the oxide barrier up to a well defined dc-Josephson current threshold I_m without causing any voltage drop ($V=0$) across the oxide barrier. Second, the current-voltage relation becomes non-linear, i.e., the tunnel conductance becomes voltage dependent. In particular, the tunnel current is strongly suppressed at voltages $V<V_g$, it surges up at $V=V_g$ and it approaches the "normal" tunnel current at $V>V_g$. Here, $V_g=2\Delta/e$ denotes the gap voltage ($V_g=$ 2.5 mV for Pb), 2Δ the superconducting energy gap of the film strips and e the electronic charge.

Apparently, the thin film structure of Figure 1a, when immersed in liquid helium, behaves either as a superconductor ($V=0$) or as a tunnel conductance ($V\neq 0$) over a substantial range of current. Figure 1d denotes a further property of this structure, namely, a dependence of the dc-Josephson current threshold I_m on magnetic flux Φ enclosed in the junction. This dependence is more clearly shown in the I_m vs Φ plot of Figure 1e. One may exploit this property by providing a third thin film strip on top of the junction and insulated from both junction electrodes. A "control" current I_c flowing through this third line generates a magnetic flux penetrating the junction and thus modulates the threshold I_m. Accordingly, one may relabel the horizontal axis of Figure 1e by I_c and interpret the plot as follows: if the vector sum of junction and control currents falls inside of the area under the curve, the voltage across the junction is zero; if the vector falls outside of the area, the voltage is finite. The functional dependence of $I_m(I_c)$ can be varied widely and predictably by engineering design.

The transition time from $V=0$ to $V=V_g$ is predominantly governed by the junction capacitance C and the charging current I_g through the junction and is given approximately by

$$t_R = C(V_g/I_g) \qquad (1)$$

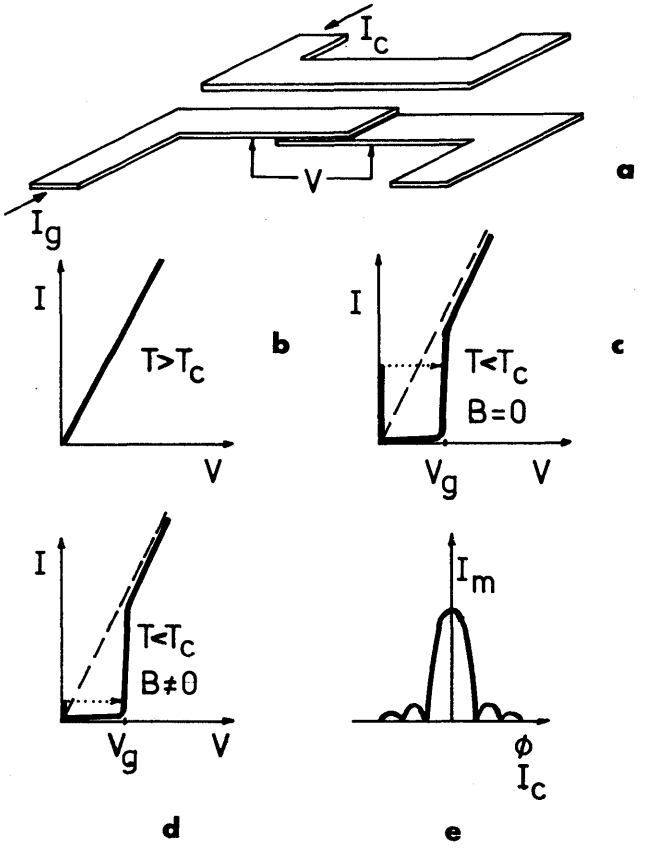


Figure 1—Josephson tunneling device (a) Structure (b, c, d) Current-voltage plots (e) Threshold current-flux (and control current) plot

Since, for miniaturized junctions, C becomes quite small and V_g is small anyway, transition times of 10 to 50 psec are readily obtainable.[4,5] It should be noted that the transition back to $V=0$ occurs usually at a current much less than I_m, i.e., the device exhibits hysteresis,[6] and the transition proceeds somewhat more slowly. Extensive reviews of Josephson devices can be found in References 7 and 8.

Circuits

Most circuits with Josephson devices which have been investigated so far are of the basic configurations shown in Figures 2a and 2b. Either Josephson devices are incorporated in both branches[9] of a superconducting loop (Figure 2a) or one Josephson device is shunted via superconducting striplines with a resistor[10,11] (Figure 2b). External current supplied to the loop of Figure 2a can be routed through either branch by forcing the Josephson device of the alternate branch into the $V\neq 0$ state. The device will automatically revert to the $V=0$ state when all (or almost all) current has been rerouted. Except during actual rerouting of current, no power will be dissipated in this circuit. It is noteworthy that, once all incoming current is routed into one branch, the device in the other branch has reverted to $V=0$, and when the external current is then switched off, a circulating current is established in the loop to maintain the magnetic flux linked with the totally superconducting loop. The circulating current is persistent, does not dissipate power and can be used to store binary information. The time required to reroute current is governed by the inductance L of the loop, the driving voltage V_g and the amount of current I to be rerouted. It is approximately given by:

$$\Delta t = L\left(\frac{I}{V_g}\right) . \qquad (2)$$

The incoming current in the configuration of Figure 2b will pass totally through the Josephson device as long as it is in the superconducting state. When it is switched to $V\neq 0$, part of the incoming current (i.e., V/R) will be diverted to the resistor path. The resistor value may be chosen to intersect the current-voltage characteristic of the device at $V=V_g$ or at $V<V_g$ and, in particular, such that the circuit is "latching"[10,11,12] i.e., needs resetting to $V=0$, or "non-latching," i.e., follows the input control signals as, for example, described in Reference 13. As indicated in Figure 2b, more than one control line may be placed on top of the junction and be used by proper design to perform AND and OR logic functions.[12] Clearly, networks can be assembled with circuits as shown in 2a and 2b by using the output striplines of devices to control other devices.

The characteristic impedance of the striplines connecting Josephson device and resistor can be chosen such that the resistor represents a matched termination, thus providing a zero reflection factor. In this case, the time needed to establish the output current at the location of the resistor is governed by the voltage risetime and the propagation delay of the striplines.

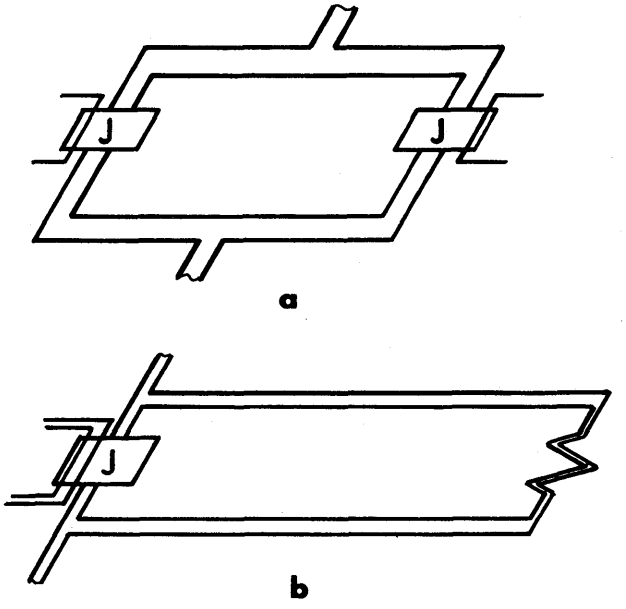


Figure 2—Josephson device circuits (a) Superconducting loop with two devices (b) Resistive loop with one device

Hence

$$\Delta t = t_R + t_d \tag{3}$$

where t_R denotes the risetime at the device and t_d the delay in the lines. An average logic delay of 200 psec per circuit has been demonstrated in a 1 bit full adder[14] controlled with Josephson devices.

MEMORY COMPONENTS

NDRO Loop Cells

A practical NDRO memory cell[15,16] for bit organized random access operation is shown in Figure 3. It comprises a superconducting loop with Josephson devices A and B in each branch, both controlled by "control" bit lines for writing; one branch of the loop acts as control for a third Josephson device S for non-destructive read out. Persistent circulating currents ($I_w/2$) in clockwise or counterclockwise directions represent stored binary ones and zeros, respectively. The conservation of magnetic flux, for as long as the loop remains totally superconducting, dictates that when an external current I_w is applied, it must split equally into both branches and superimpose on the circulating current such that I_w flows through one branch and zero current through the other; it also dictates that the original circulating current is restored when the external current is switched off. Thus, the direction of circulating current can be detected without disturbing the information by applying a word current I_w which causes either I_w or zero current to flow in the branch controlling device S and a sense current I_s which causes the device S to switch only when its control current exceeds $I_w/2$. Data is written into a cell by coincident word current I_w and bit current I_B which can switch one device in the selected cell and reroute the word current into the alternate branch.

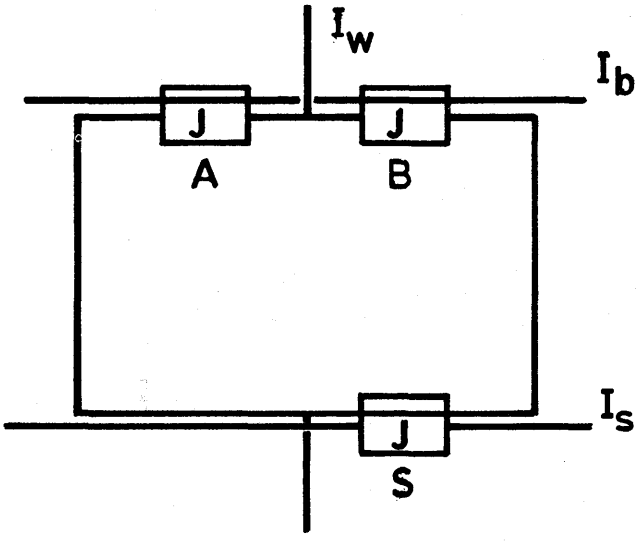


Figure 3—NDRO random access memory cell

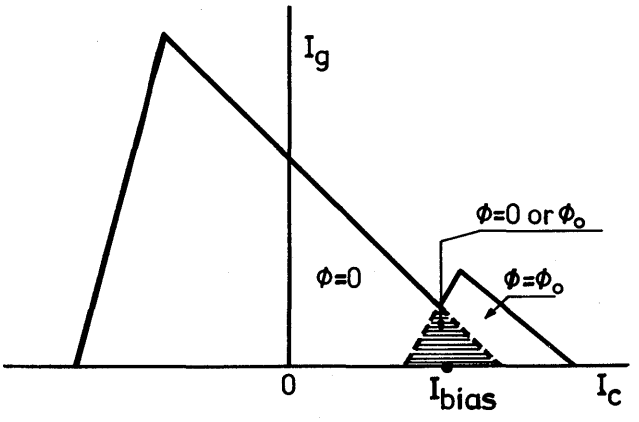


Figure 4—Gate current-control current plot of single device memory cell

Experiments have demonstrated that data can be written in rather large memory cells[16] with 2 mil minimum line width and ~250 mil² area in about 600 psec and in miniaturized cells[17] with 2μ minimum line width and ~1.4 mil² area in less than 100 psec. It was also demonstrated that more than $5 \cdot 10^8$ NDRO operations left the stored information undisturbed.[16]

DRO Single Device Cells

Single specially shaped or elongated Josephson devices[18,19] can be used for data storage in a DRO bit organized random access mode as well. These devices admit magnetic flux in discrete quanta of magnitude $\Phi_o = h/2e \sim 2 \cdot 10^{-15}$ V-sec, where h denotes Plank's constant and e the electronic charge, when their control currents are steadily increased; they possess an operating region in the $I_g - I_c$ plane as shown shaded in Figure 4 in which either 0 or 1, flux quanta can be maintained without standby power and stably by a suitable bias control current. The number of flux quanta actually stored in such devices can be increased (decreased), from 0 to 1 (1 to 0) by a temporary increase (decrease) of the bias control current. The presence of a flux quantum can be detected either by the occurrence of an energy spike[18] upon reduction of the bias control current if a flux quantum was stored or by the modification[19] which a stored flux quantum exerts on the dc-Josephson threshold current I_m. In both cases, the stored information is destroyed and must be rewritten. The energy associated with a flux quantum which is maintained in a device, for example, by a circulating current of 1 to 10 mA amounts to about 2 to 20 attojoules. Although this energy is extremely small, even fractions of it have been detected experimentally by Josephson device detectors.[18] This is in part due to the fact that the release of a flux quantum as found by simulation leads to an energy spike of only a few picoseconds duration, but a peak of a few hundred microvolts and microamperes. The expected advantage of single device cells is their potential for large memories with high bit densities.

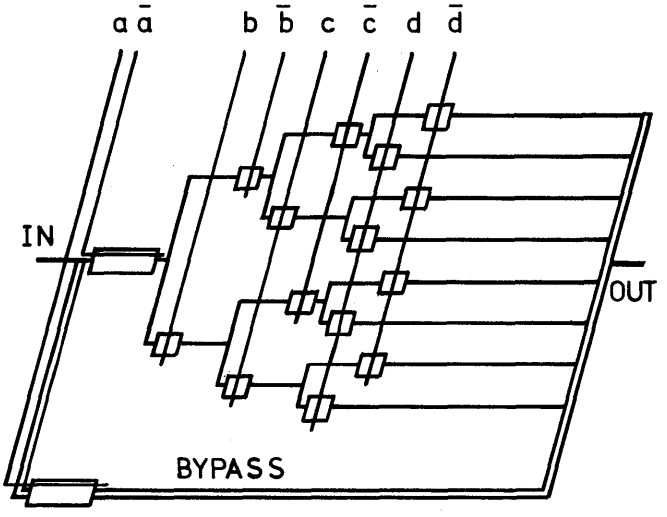


Figure 5—Tree decoder

Decoders and Drivers

Addresses can be decoded with Josephson devices by tree[15] decoders. Tree decoders consist of branching networks with one or more Josephson devices in each branch, as shown in Figure 5. The branches of the last stage can be connected either directly or via drivers to the array lines. The Josephson devices in each branch are controlled by the "true" and "complement" outputs of address registers. For each address, all but one branch through the decoder tree contain Josephson devices in the $V \neq 0$ state, while all Josephson devices along the selected branch remain in the $V = 0$ state. It is convenient to provide a bypass line to carry the current around the array when desired. The decoder and bypass configuration can be supplied with dc current. Apparently, any selected branch and array line form a "giant" superconducting loop with the bypass line, where current rerouting is driven by the one or more Josephson devices in the bypass line. The time needed to route current from the bypass into a selected array line is then given by Equation 2. The operational speed can be increased and residual disturb currents in nonselected array lines eliminated by using line drivers comprising Josephson devices which are controlled by output branches of a tree decoder; their output lines are connected to array lines. Thus, the tree decoder loops are minimized and speed is gained when the output (array) lines of the drivers are terminated in their characteristic impedance. The total delay time is then the sum of (reduced) current routing time through the tree decoder according to Equation 2 and the signal propagation time through the array line according to Equation 3.

Sense Signal Detection

Sense gates of NDRO loop cells (see Figure 3) can be interconnected into rows of sense lines[15] which are provided at one edge of the array with superconducting bypass lines, as shown in Figure 6. These bypass lines can control, in turn, a column of Josephson devices outside of the array which, via another bypass line, can finally control a single read out Josephson device for the whole array. In this arrangement, the read out time, beginning from the time when a sense gate in the array has been switched, is given by the sum of two current routing times according to Equation 2.

Of course, it is possible, in principle, to terminate sense lines and the "column" line in their own characteristic impedances also, in which case the read out time would be the sum of signal propagation times according to Equation 3 for one row and the "column" line. The practicality of this approach depends on tolerance and margin considerations and can be assessed only in a realistic and detailed design.

DRO single device cells generate their read out signals on that array line on which they are serially strung. In coincidence operation, this line will carry a current pulse for cell selection. The read signal must, therefore, be separated from the drive pulse during read out. Special strobed read detection circuits are required if the energy spike upon release of a flux quantum is to be detected. That this can be done in principle has been experimentally demonstrated.[18] If, on the other hand, the modification of the threshold current I_m by a stored flux quantum is used for read out,[17] either one of the schemes described in conjunction with the NDRO loop cells can be employed for read out.

LSI FABRICATION

Since Josephson devices can perform memory, drive, detection and decode functions, integration of arrays and peripheral circuits on a common substrate and—drawing on experience from semiconductor technology—adoption of a wafer and chip fabrication concept[20] with photolithographic techniques for pattern definition and evaporation and sputtering methods for building a multilayered structure are quite natural. Once large scale integration has been adopted, the fabrication process must allow for material and process compatibility of all required circuit components, i.e., Josephson devices, resistors, superconducting interlayer contacts,

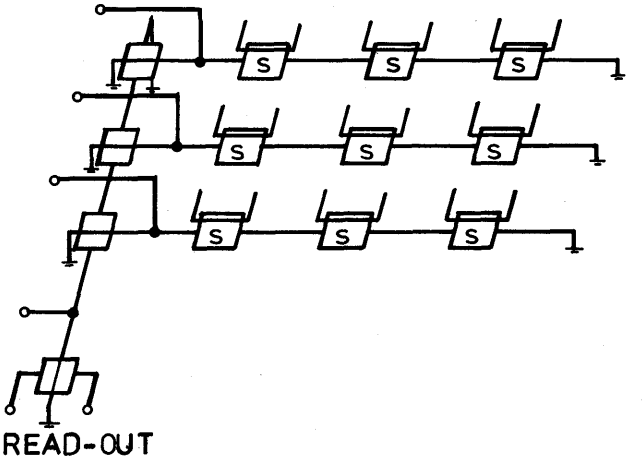


Figure 6—Sense detection scheme

insulation and striplines. A major challenge in this respect, of course, is the reproducible preparation of extremely thin and pinhole-free native oxide tunnel barriers on the surface of thin metal films which have been subjected to photolithographic chemistry and ambient atmosphere with contamination being unavoidable. An RF sputter technique[21] in which growth rates of oxidation and removal rates of sputter etching are balanced has been developed and has so far provided encouraging results as to the thickness reproducibility of thin oxide tunnel barriers.

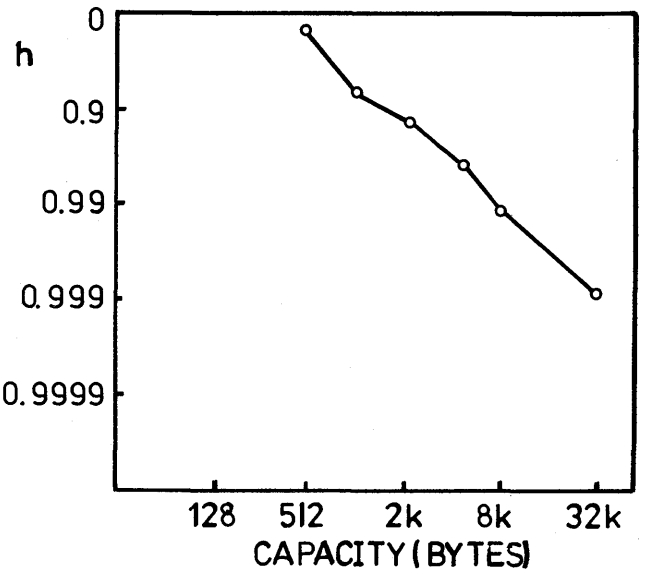
PERFORMANCE PROJECTION

To date, memories of practical size have not been built or designed. Performance must, therefore, be projected by estimating cell and array sizes and cycle and access times on the basis of the experimental circuits and the delay equations mentioned above. Since LSI has been adopted, it is all but impossible to predict ultimate bit densities and access times because they depend strongly on line width resolution which, in turn, is likely to improve as a result of present exploration of uv, *e*-beam and x-ray exposure techniques. Just how much improvement is possible is not clear yet, however. Potential performance of Josephson device memories with present state-of-the-art resolution of, say 0.2 mil minimum line width—i.e., what could be expected if Josephson device technology were developed and ready for manufacturing—is estimated instead.

On the basis of the previously mentioned 1.4 mil^2 loop cell with 2μm wide lines and an upper bound of switching time of 100 psec, an NDRO loop cell with 0.2 mil wide striplines may be estimated to occupy an area of about 2.5×2.5 mil and to switch in about 100 psec. Then, an array of 64×64=4096 cells of NDRO loop cells should fit into an area of about 160×160 mil. With peripheral circuits being located on the same chip, one may make the following assumptions for such an array: word, bit and sense lines, tree decoder branches, matrix decoder control lines and a sense column line are all about 160 mil long and 0.2 mil wide. The loop inductance for those striplines (with 2000 Å thick insulation) would amount to $L\sim350$ pH, the propagation delay to $t_d\sim100$ psec and the risetime of the output of a Josephson device driver to $t_R\sim50$ psec. It is also assumed that drive currents of about 10 mA and sense currents of about 2.5 mA are used and that four serially connected Josephson devices per decoder branch and bypass line are provided.

Taking note finally of the pulse sequences required for bit organized NDRO random access and allowing for sufficient pulse overlap, access and cycle times on the order of 2 to 2.5 nsec are derived for a low power, 4K bit random access NDRO array with a bit density of about $1.6\cdot10^5$ bits/inch^2.

DRO single device cells are likely to occupy less area than NDRO loop cells since only one Josephson device and no loop is required. Four times as many cells could possibly be fitted in the same array area. Total access and cycle times would likely be longer due to the need for extra pulses to perform rewriting and the possible need for sense signal amplification. However, even if access and cycle times would turn out to be



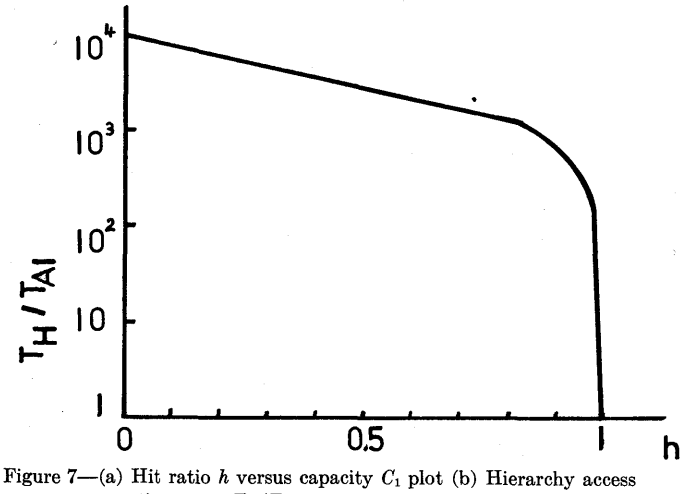


Figure 7—(a) Hit ratio h versus capacity C_1 plot (b) Hierarchy access time ratio T_H/T_{A1} versus hit ratio h plot

an order of magnitude longer than those derived above, the potentially high bit density of about $6.4\cdot10^5$ bit/inch^2 combined with low power and 20 to 30 nsec access and cycle time would appear quite attractive for use as main or bulk memory in hierarchies to feed ultrafast CPU's.

A NOTE ON MEMORY HIERARCHIES

Although the memory hierarchy concept has been proven to approximate the ideal of a large *and* fast memory quite well, it is noteworthy that certain drawbacks are associated with the concept as well. Memory hierarchies tend to be "tuned" to specific classes of computational tasks and moreover, the sharpness of the "tuning" curve depends on the access time

ratio of the hierarchy's memories and their capacities. To elucidate this point, consider first the effective hierarchy access time T_H of a two level hierarchy with memories M_1 and M_2.[22] T_H is a function of the so-called hit ratio h and the access time ratio of T_{A2}/T_{A1} where T_{A1} and T_{A2} denote the access times of memory M_1 and M_2 respectively. The hit ratio h is an empirical measure defined by the ratio of requested data found in M_1 over the total number of data requests issued by the CPU. It is clearly a measure of dynamic clustering of data addresses in address space. It depends, however, also on the capacity of the faster and smaller memory (here M_1) of the hierarchy, as indicated in the plot of Figure 7a,[22] which shows that h increases for increasing C_1. The hierarchy access time T_H as a function of h for a rather large ratio of $T_{A2}/T_{A1}=10^4$ is plotted in Figure 7b. This plot signifies that T_H drops significantly only when the bit ratio h exceeds 0.95 to 0.99. Clearly, this hierarchy would perform well only for a set of tasks with large hit ratios h. One can "detune" this hierarchy by (a) providing memories M_1 and M_2 with a more favorable, i.e., smaller, T_{A2}/T_{A1} ratio and (b) providing larger memory capacity C_1.

In the case of Josephson device memory hierarchies for ultrafast CPU's, the following strategy might be suggested: since M_1 with access time T_{A1} on the order of 3 nsec is so fast that considerations of signal delays through the memory package will likely be limiting its capacity C_1, it is advisable to reduce the access time T_{A2} of M as much as possible to obtain a favorable ratio T_{A2}/T_{A1} of, say, 10 to 20. The memory M_2 will likely be backed up by conventional memory or storage device levels M_3 with a rather large access time ratio T_{A3}/T_{A2} being unavoidable. Therefore, the capacity C_2 of M_2 should be made as large as feasible to increase h. In consequence, one should focus on making M_2 as large and as fast as possible.

SUMMARY

Josephson devices, circuits and memory components have been reviewed. An estimate of potential memory performance with state-of-the-art photolithographic resolution has been made, and it is found that rather high performance buffer and main memories for ultrafast CPU's can be envisioned. It is indicated that considerations of memory hierarchy performance favor the provision of a main memory with large capacity and access times on the order of 20 to 100 nsec. It is believed that the performance potential of Josephson device memories and CPU's warrants further investigation of the feasibility of this new technology.

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