Modeling of Intermediate Node States in Switch-Level Networks*

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Abstract - An algorithm is presented for event-driven switch-level simulation of CMOS networks in which intermediate signal values are common. The proposed method is based on a local signal propagation scheme and an extended node model including both a logical low and a high contribution to the state of a node. The quantization effects of typical CMOS networks can thereby be modeled and, hence, the spread of undetermined logic values is in many cases prohibited.

I. INTRODUCTION

Switch-level modeling and simulation have become an important method for predicting the behavior of MOS circuits under the presence of faults. In the design phase, simulation-based approaches can be used to evaluate important dependability aspects of integrated circuits such as: fault coverage, error detection latency and diagnosability.

By operating directly on the transistor network, switch-level simulators can reliably model many important phenomena in MOS circuits [1]-[6]. However, new algorithms, are needed to accurately and efficiently handle the abnormal situations that may occur in circuits under the presence of faults. Steady-state intermediate node voltages frequently occur when realistic faults, such as transistor stuck-on faults and various short faults, are introduced into CMOS networks. In a traditional switch-level model, these situations give rise to undetermined logic states (X) that are likely to propagate to the primary outputs of the network, and hence reducing the degree of confidence when, for instance, estimating the fault coverage of a test set.

Consider, for example, the circuit shown in Fig. 1, in which the transistor M_1 is permanently conducting (stuck-on) owing to a fault. When considering minimum-size implementations, in which all transistors have the same (minimal) size, the ratio between n-MOS and p-MOS transistor driving strengths is about three. The figure shows three n-MOS transistors in series driving the node N_a low and the faulty p-MOS transistor driving the node high, which results in an intermediate voltage level of 2.7 V at node N_a. However, owing to the voltage transfer characteristic of the subsequent gates, this voltage is quantized, and the nodes N_b and N_c will assume logical definite values. In a traditional switch-level logic the node N_a will be

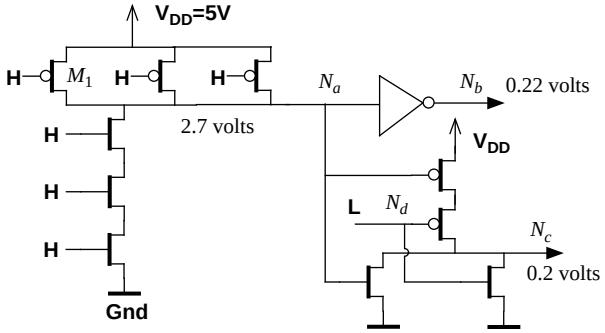

Fig. 1. Node voltages when transistor M_1 is permanently conducting.

assigned the undetermined logic state (X) forcing the output nodes N_b and N_c into the X state. Thus, an unwanted spread of unknown values results in incorrect node states on the output nodes. A correct handling of undetermined values in switch-level networks has generally proven to be one of the most time-consuming algorithmic tasks [8][9].

It would be convenient to define a new logic node state, I, in situations in which there are conducting paths both from V_{DD} and ground of similar resistance connected to a node. Both n-MOS and p-MOS transistors should be regarded as conducting when this logic state is assigned to a gate node. By this approach, it is possible to model the quantization effects in minimum-size implementations of CMOS gates caused by the greater driving strength of n-MOS transistors. An example of this quantization is illustrated in Fig. 2. For the case that the input node is assigned the logic state I, both the n-MOS and p-MOS transistors are conducting. The output node will typically be assigned the logical low state, as the n-MOS transistor driving strength is much greater than that of the p-MOS transistor and, consequently, the intermediate input value has been quantized.

This paper presents a new and efficient event-driven algo-

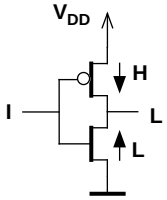

Fig. 2. Quantization in a CMOS inverter.

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rithm suitable for the simulation of MOS networks in which different signals simultaneously drive high and low logical values to a node. The node model includes an intermediate logic state and an extended dominance relation to efficiently exclude or propagate values between neighboring nodes. Most earlier work on switch-level modeling has focused on global algorithms [5]-[7], in which a steady-state solution is obtained by solving a set of network equations or by tracing paths in a graph representing the network. In the model proposed in [10], which is based on Kirchoff's laws, no intermediate state is necessary and, in [2], a logic state corresponding to an intermediate voltage interval is proposed. The algorithm proposed in this paper, on the other hand, is based on a local approach [1][11]-[13] in which only a single node and its interaction with neighboring nodes are considered at one time. During the node evaluation procedure, the state of a node is predicted and events are generated and put in a time ordered list whenever there is a change in the predicted state in comparison with the current state of the node. The event scheduling follows traditional algorithms and will not be discussed in this paper.

The advantage of a local algorithm is that it is cost-effective and that the signal propagations follow the ordinary transient behavior of a network, which is a requirement when, for example, tracing glitches. In the proposed method, the well-known dominance principle [1][5][12] is extended to include two dominant signals associated with each node: one driving the node high and one driving the node low. The signal propagation between neighboring nodes is based on the principle that the influence of any node whose strength is directly dependent on a certain target node must be ignored when the target node itself is evaluated.

II. State Prediction Based on Signal Values

A. Signal Values

A signal, S, is defined by a value, $< S >$, and a direction which is given by an index of S. The value of a signal is represented by a pair, $< S > = < l, r >$ in which l is a logic state and r is a resistance (inverse strength). The way a node is influenced by a neighboring node via a conducting element is described by a signal whose value is given by a transfer function, T. Given a transistor, M, and the logic state and resistance assigned to a drain/source node of M, the function T computes the logic state and strength of a signal directed to the source/drain node of M based on the transistor's gate state and the adopted transistor model. The value of a signal, $<S_{bi}>$, propagating from a node, N, to another node, N_b, through a transistor, M_i, is written as $<S_{bi}> = T\,(M_i, <L, R>)$, in which L is the logic state of node N and R is the resistance of N. As undetermined logic states can occur on the gate node of a transistor, a transistor resistance may be represented by an interval such as $[r_t\,,\ \infty]$ where r_t is the resistance of a transistor that is fully conducting.

B. Conductance Ratio and Logic States

The set of logic states adopted in the proposed node model is { L,D,I,U,H,X }, in which L and H represent the usual logical low and high states, and X is the undetermined logic state that represents an unknown voltage level. The D state, which is a logical low state, represents the threshold voltage drop occurring when a low signal is passed through a conducting p-MOS transistor, and U represents the analogous situation for an n-MOS transistor. The states D and U may also be predicted on the node when there are signals simultaneously driving logical high and low values to a node. Fig. 3 shows the basic model for the prediction of the logic state of a node when there are no signals driving the X state to the node. G_{HU} represents the sum of all signal conductances driving the logic state H or U to the node and, analogously, G_{LD} is the sum of signal conductances driving the logic state L or D. Let K denote the conductance ratio $K = G_{LD} / G_{HU}$. Each one of the logic states represents a non-overlapping voltage interval which can be mapped into a corresponding interval of conductance ratios. The correspondence between the logic states and conductance ratios together with the symbols used to represent the interval boundaries are shown in Fig. 4.

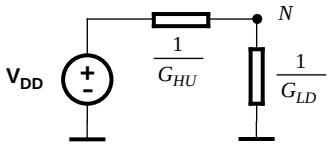


Fig. 3. Simplified node model for the prediction of a logic state.

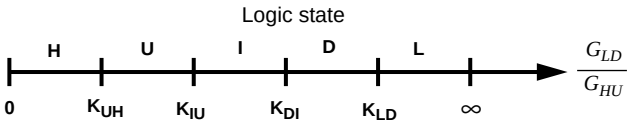


Fig. 4. Correspondence between conductance ratio intervals and logic states.

The boundary between the voltage intervals representing the states L and D is chosen to be identical to the threshold magnitude, $|V_{TP}|$, of a p-MOS transistor, in agreement with the pass transistor threshold voltage drop discussed earlier. This voltage level corresponds to the conductance ratio

$$K_{LD} = \frac{V_{DD}}{|V_{TP}|} - 1.$$

Analogously, the boundary between the voltage intervals corresponding to the states H and U is defined as one n-MOS threshold voltage drop (V_{TN}) below V_{DD}. The conductance ratio, K_{UH}, for this case can be written as

$$K_{UH} = \frac{V_{TN}}{V_{DD} - V_{TN}}.$$

C. Intermediate Logic State, I

The logic state I corresponds to the voltage interval between the D and U intervals. It is required that the I state, when for example applied to the input of an inverter, shall drive the out-

put low, which means that the n-MOS transistor must be fully conducting. The voltage transfer characteristic of a CMOS gate with more than one input is sensitive to the logic function realized and to the input pattern as shown in Fig. 5. The voltage level, V_{DI}, corresponding to the boundary between the D and I intervals can therefore be defined from the transfer characteristic of an inverter or primitive gate (NAND, NOR) as the least input voltage for which the output voltage does not exceed V_{TN} for any of the transfer characteristic as illustrated in Fig. 5. The choice of V_{TN} as output voltage guarantees that, when the I state is applied as input to a primitive gate the output is interpreted as a logical low value. This choice of V_{DI} results in an expansion of the logic state D into the transition regions (interval V_R in Fig 5) which, consequently, may result in an incorrect behavior when the D state is applied to the input of a logic gate. However, for internal nodes that are not connected to any transistor gate node it is irrelevant whether the logic state of a node is D or I as long as the node model includes both a logical low and high contribution to the state (see Section III). Circuit-level simulations are needed to extract the value of V_{DI} for the CMOS gates considered.

Finally, the upper voltage boundary of the I interval is not a very critical parameter for the minimum-size transistor implementations considered in this paper. This boundary can be defined as the greatest voltage, when applied to the gate of a p-MOS transistor whose source is connected to V_{DD}, for which the transistor still remains conducting.

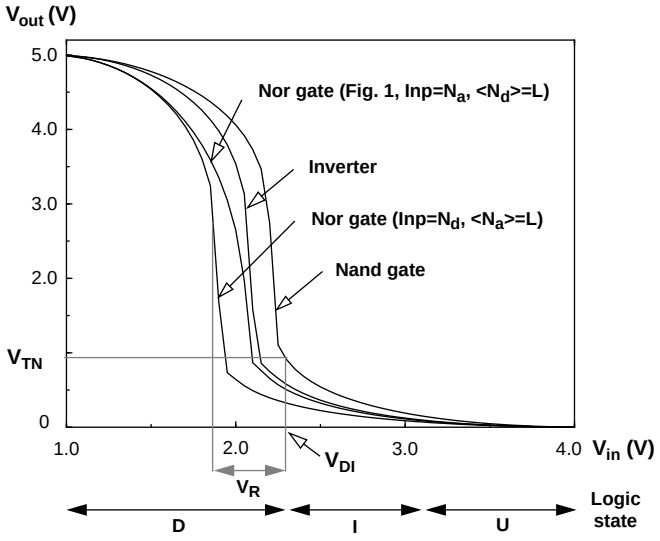


Fig. 5. Voltage transfer characteristic of typical primitive CMOS gates.

D. Transistor Transfer Characteristic

The transfer characteristic of a transistor when its gate node is assigned the logic state I is given in Table I. It can be seen that the transistor is fully conducting only for the case in which the logic state of the terminal node is L(H) for an n(p)-MOS transistor. An unknown resistance, represented by an interval of possible values, must be propagated in the cases in which it is uncertain whether the transistor is conducting or non-conducting (for example, when the terminal node of an n-MOS transistor is D).

For cases in which the gate node of an n(p)-MOS transistor is assigned H/U(L/D) and the drain/source node is assigned the logic state D,I or U, the signal value that is propagated through the transistor is transformed into two values of the logic states H and L (see Section IV).

E. Unknown Signal Values

The node model in Fig. 3 must be modified when there are signals driving the X state. Let G_X denote the sum of all signal conductances driving the logic state X to the node. This sum must be added either to G_{LD} or G_{HU} or both depending on what boundary is checked when the logic state of the node is computed. Moreover, when there are signal values whose resistances are intervals, the conductances in the node model in Fig. 3 represent intervals: $G_{LD} = [G_{LDmin}, G_{LDmax}]$ and $G_{HU} = [G_{HUmin}, G_{HUmax}]$. To predict a definite logic state, the entire interval of possible conductance ratios must fall within one of the intervals in Fig. 4. The X state is otherwise predicted. For example, the conditions for predicting the logic state D are:

$$\frac{G_{LDmax} + G_X}{G_{HUmin}} < K_{LD} \quad \text{and} \quad K_{DI} \le \frac{G_{LDmin}}{G_{HUmax} + G_X} .$$

The conductance ratio boundaries used in the examples and simulation results presented in this paper are: $K_{LD} = \frac{1}{K_{UH}} = 4$, $K_{DI} = 1.4$ and $K_{IU} = 0.5$.

TABLE I
SIGNAL PROPAGATION THROUGH A TRANSISTOR WITH THE GATE NODE ASSIGNED THE LOGIC STATE I

Transistor, M (gate state = I)	Drain/source terminal logic state, L_a	T (M, <L_a, R_a >)
n-MOS	L	< L, $R_a + r_t$[a] > (on)
	D / I / X	< D / I / X , [$R_a + r_t$, ∞] >
	U / H	< U / H , ∞ > (off)
p-MOS	H	< H, $R_a + r_t$ > (on)
	U / I / X	< U / I / X , [$R_a + r_t$, ∞] >
	D / L	< D / L , ∞ > (off)

a. r_t denotes the constant resistance of a conducting transistor.

III. AN EXTENDED NODE STATE

To represent the state of a node assigned the logic state L or H, the traditional *single-strength* node state, < L, R >, represented by a logic state, L, and a single resistance, R, is adopted. The treatment of nodes assigned the X state is performed according to [13] in which a new (secondary) node state is defined as the state obtained when the node is re-evaluated with the strongest signal driving the X state excluded. It is possible to reduce the spread of X states using this secondary node state.

For the cases in which the predicted logic state of a node is

D,I or U, the single-strength node model must be extended to take into account the strength of both logical high and low contributions to the node.

The *extended state* of a node, *N*, is represented by a value, <N> = < *P*, *Q*, *R*, *R''* >, and by two dominant signal connections which are determined dynamically based on signal strength. The value of the node, denoted <*N*>, is defined by the predicted logic state *P*, $P \in$ { D, I, U }, a quantized logic state *Q*, $Q \in$ { H, L } and by two node resistances, *R* and *R''*. The quantized logic state, *Q*, has the value H(L) if $G_{HU} \geq G_{LD}$ ($G_{LD} > G_{HU}$). The *primary dominant* signal, S_{dom}, is defined as the strongest signal driving a logic state identical to *Q* (or *Q* with a threshold drop) to the node, and the node resistance, *R*, is assigned the resistance value of this signal, in agreement with the dominance principle. The *secondary dominant* signal, S_{snd}, is defined as the strongest signal for which the logic state is $\overline{Q}$[1]. The secondary resistance, *R''*, of the node is defined as the resistance value of the signal S_{snd}. Note that the primary and secondary dominant signals in some situations may originate from the same node.

IV. Signal Transformations

The signal transformation scheme is based upon the principle that the effects of a particular node on the state of the neighboring nodes must not be taken into account when the node itself is evaluated. By analyzing the local dominance situation at the node under evaluation, it is possible to sort out the node's own contribution to the incoming signals from the neighboring nodes. Table II shows the necessary transformation of an incoming signal directed to a node N_b from an adjacent node N_a for various dominance situations. Both nodes are assigned an extended node state meaning that the predicted node state is D, I, or U and that the state of each node has two main signal contributions based on the dominant signals. In the table, the absence of a certain dominance relation to a node means that it is irrelevant in the particular situation from which node the dominant signal originates.

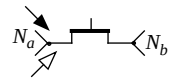
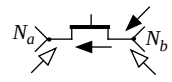
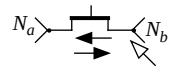
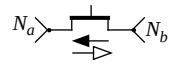
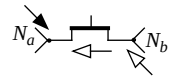
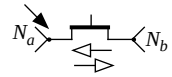
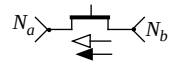
Consider for example the dominance situation in case 1 in Table II. Both the logical high and low contributions to the state of node N_a originate from nodes other than N_b and, consequently, node N_b has no influence on the signals from node N_a, which means that the strength of both the logical high and low contributions to node N_a can be propagated to node N_b. In the dominance situation in case 2, on the other hand, node N_b is the primary dominant node of N_a, which means that the quantized logic state Q_a and primary resistance R_a of node N_a are derived from node N_b. The state Q_a should therefore not be permitted to effect node N_b. However, as seen in the table, node N_b is not the secondary dominant node of N_a and therefore the strength by which N_a is driven to the inverse state $\overline{Q}_a$ is not influenced by N_b. The logic state $\overline{Q}_a$, with the corresponding strength, can thus be propagated to node N_b. Note that in an ordinary switch-level algorithm, without the secondary dominant signal, the signal originating from node N_a should be completely excluded and, hence, a correct prediction of intermediate values would be impossible.

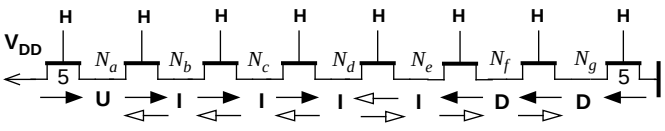
In the case that node N_b, as shown in case 7, is both the primary and secondary dominant node of node N_a, the signal from N_a must be excluded in the evaluation of N_b. Signal exclusion is also performed in the dominance situation illustrated in case 3, in which an inconsistent situation of a transient nature has arisen.

Consider a chain of conducting transistors as shown in Fig. 6. The transistors at the ends of the chain have the normalized resistance value of 5, and all other transistors have a resistance value of 1. As can be seen, the predicted states of

1. $\overline{Q}$ means the inverse state of *Q*, that is $\overline{Q}$ is L/D if *Q* is H/U and $\overline{Q}$ is H/U if *Q* is L/D.

TABLE II
Signal Transformation Through a Conducting Transistor when the Drain/Source Nodes are Assigned Extended Node States
Let $<N_a> = <P_a, Q_a, R_a, R"_a>$

Case	Dominance relations	Signal values to node N_b from node N_a
1		$< S_{ab1} > = <Q_a,\ R_a + r_t>$ $< S_{ab2} > = <\overline{Q}_a, R"_a + r_t>$
2		$< S_{ab} > = <\overline{Q}_a, R"_a + r_t>$
3		S_{ab} is excluded
4		$< S_{ab} > = <\overline{Q}_a, R"_a + r_t>$
5		$< S_{ab} > = <Q_a, R_a + r_t>$
6		$< S_{ab} > = <Q_a, R_a + r_t>$
7		S_{ab} is excluded
	= Primary dominant signal = Secondary dominant signal	



Node states and voltage values in a corresponding resistance chain.

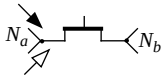
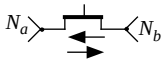
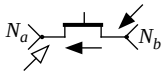
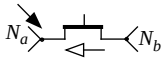
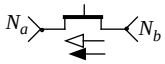
$<N_a>$ = <U, H, 5, 11>	3.4 V	$<N_e>$ = <I, L, 7, 9>	2.2 V
$<N_b>$ = <I, H, 6, 10>	3.1 V	$<N_f>$ = <D, L, 6, 10>	1.9 V
$<N_c>$ = <I, H, 7, 9>	2.8 V	$<N_g>$ = <D, L, 5, 11>	1.6 V
$<N_d>$ = <I, H, 8, 8>	2.5 V		

Fig. 6. Dominance relations in a chain of n-MOS transistors.

the nodes are not symmetric, although the transistor chain is symmetric. The reason for this is the asymmetry in the chosen conductance ratio boundaries K_{DI} (=1.4) and K_{IU} (=0.5). Node N_f, for example, has the conductance ratio G_{LD}/G_{HU} of 10/6, which results in the predicted state D, while node N_b, with the ratio G_{LD}/G_{HU} of 6/10, is assigned the I state. The situation given in the figure is the steady-state solution of the network in which all nodes are consistent and no events can be generated. Consider, for example, node N_d. The signal from node N_c is transformed according to case 5 in Table II to <H, 7+1>, and the signal from node N_e is transformed according to case 6 to <L, 7+1>, which gives the ratio G_{LD}/G_{HU} of 8/8.

Table III shows the corresponding signal transformation scheme for the case in which node N_b is assigned the logic state H or L and therefore is assigned a single-strength node state.

TABLE III
SIGNAL TRANSFORMATION WHEN NODE N_b IS ASSIGNED A SINGLE-STRENGTH NODE STATE

Case	Dominance situation	Signal values to node N_b from node N_a
8		$< S_{ab1} > = <Q_a,\ R_a + r_t>$ $< S_{ab2} > = <\overline{Q}_a, R"_a + r_t>$
9		S_{ab} is excluded
10		$< S_{ab} > = <\overline{Q}_a, R"_a + r_t>$
11		$< S_{ab} > = <Q_a, R_a + r_t>$
12		S_{ab} = is excluded

V. EXAMPLES OF NETWORK SOLUTIONS

Consider the network in Fig. 7 which shows many typical situations that occur when faulty transistors are present in CMOS networks. The logic states predicted in both the proposed two-dominance model (bold logic states) and in a traditional switch-level model (logic states shown within parenthesis) are shown for comparison. As can be seen, the traditional switch-level model predicts the X state for many of the nodes. The two-dominance model, on the other hand, predicts the correct logic state for all nodes. It should be noted that the I state can be quantized in subsequent gates which is not possible in the case of the X state.

As an example of the proposed node evaluation procedure, consider node N_a in Fig. 7. Four conducting transistors (M_1 - M_4) are connected to that node. The signal associated with transistor M_1 is transformed (case 2, Table II) to $<S_{a1}>$ = <H, 12> in order for N_a to be affected only by the inverse quantized state of node N_b. The dominance situation is the same for the signal associated with M_2 and, consequently,

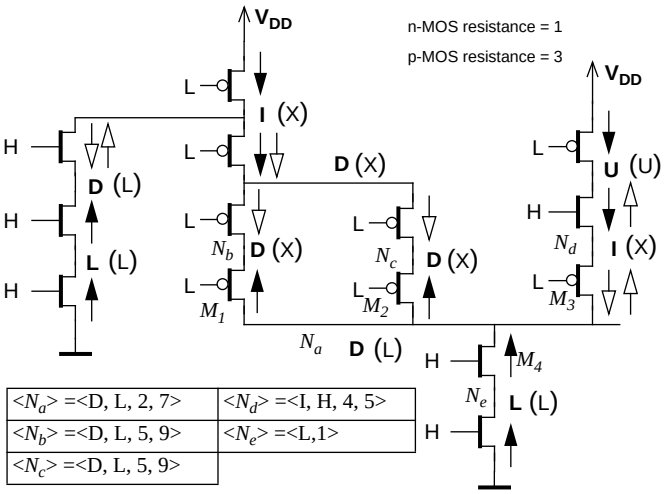


Fig. 7. A network containing several conducting paths.

an identical transformation is conducted on that signal. As the strength of the logical low contribution to the state of N_d originates from node N_a, which is indicated by the secondary dominant signal connection to N_d from N_a, the signal through M_3 is transformed (case 6, Table II) to <H, 7>. The signal associated with transistor M_4, $<S_{a4}>$ = <L,2> is not transformed, as node N_a is neither the primary nor the secondary dominant node of N_e. Given all the transformed signals, the conductance ratio is G_{LD}/G_{HU} = 21/13 = 1.6 which, according to Section II, will result in the prediction of the logic state D. The strongest signal driving the logic state L is through M_4 and, hence, this signal will become the primary dominant signal of node N_a. The secondary dominant signal, i.e. the strongest signal driving the inverse quantized logic state of N_a (H), is the signal originating from node N_d.

VI. EXPERIMENTAL RESULTS

An experimental simulator was developed that implements the proposed extended node model and signal transformation scheme. Simulation experiments were performed to determine the accuracy of the proposed algorithm. As an example, transistor stuck-on faults (STON) and shorts between the drain and source terminals of a transistor (DSS) were injected into CMOS networks. For each input vector applied, the steady-state value of each output node was compared with the output value obtained from a corresponding circuit-level simulation, and any discrepancy in terms of logical interpretation was recorded. The number of discrepancies observed is shown in Table IV. As a comparison, identical fault simulations were carried out with another switch-level simulator, BiDom [13], which has an efficient masking capability for handling the X state. However, there is neither an intermediate logic state nor a two-dominance model included in that simulator. Any X value was regarded as a discrepancy in the comparison between the circuit-level and switch-level output node values, as the voltage values obtained from the circuit-level simulations were always in the intervals: less than 1V or greater than

4V. All networks simulated are minimum-size implementations, meaning that the ratio between the n-MOS and p-MOS transistor driving strengths is 3. The 1-bit ALU includes a CMOS pass transistor network, and transistor implementations of the ISCAS-85 benchmark networks were obtained by converting each primitive gate to a standard static CMOS network. The RES3 network is an 8-bit residue-3 generator implemented from the minimized boolean functions as a standard static CMOS circuit. The total number of output node states observed is the product of the number of input vectors, the number of transistors fault injected and the number of output bits. It can be seen that the proposed algorithm results in a significant reduction in the number of discrepancies in comparison with the less sophisticated algorithm in BiDom. The average increase in the number of events generated per input vector in comparison with the BiDom simulator, which has a similar event generation scheme, was found to be about 7%.

A typical case in which the proposed model fails to predict the correct state is illustrated in Fig. 8 and is a general problem in any switch-level simulator based on signal dominance, which is also pointed out in [14]. The stability criteria require that the resistance of the strongest signal is chosen as the node resistance and not the equivalent parallel resistance of all signals driving the node. Node N_a is assigned the value < H, 3 > and, consequently, node N_b receives the signal values < H, 9 >, < U, 5 > and < L, 3 >, which results in the prediction of the logic state I (or X), while in the corresponding circuit-level resistance network the voltage of node N_b is about 2V which corresponds to the logic state D.

TABLE IV
COMPARISON BETWEEN SWITCH-LEVEL AND CIRCUIT-LEVEL SIMULATIONS

Network	Test set size	No. of node states observed	Number of discrepancies			
			STON faults injected		DSS faults injected	
			BiDom	Proposed method	BiDom	Proposed method
ALU1	4	408[a]	24	16	36	6
C432	16	24,528[b]	192	31	0	0
C880	8	30,576[b]	105	24	10	0
RES3	256	107,520[a]	6,128	2,684	1,894	1,484

a. Exhaustive input vector set and faults injected into all transistors.
b. Randomly chosen input vectors and randomly injected faults.

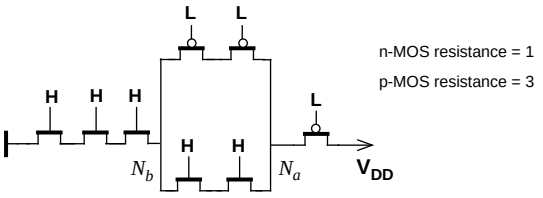


Fig. 8. A problematic situation for any dominance-based algorithm.

VII. CONCLUDING REMARKS

The presented algorithm has proven to be efficient and accurate for modeling CMOS networks in which intermediate values are common There are two dominant signal connections associated with the state of a node: one driving the node low and one driving the node high. A local signal transformation scheme is required to take into account the dependencies between neighboring nodes. With the two dominant signals, it is possible to locally propagate both the logical low and high contributions of the state of a node to its neighboring nodes. An experimental simulator was developed to implement the proposed algorithm, and comparisons with circuit-level simulations demonstrated that the accuracy in predicting the node states of networks under the presence of transistor faults is high. The increase in the number of events in comparison with a similar switch-level simulator not incorporating the local two-dominance model is about 7%.

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