CHIP HIERARCHICAL DESIGN SYSTEM (CHDS): A FOUNDATION FOR TIMING-DRIVEN PHYSICAL DESIGN INTO THE 21ST CENTURY

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ABSTRACT

This paper presents the description of the architecture of the Chip Hierarchical Design System (CHDS) and details on the required Timing Driven Physical Design capabilities that have been defined to satisfy the physical design needs for 0.25u technologies and beyond. These requirements are intended to solve the challenges including the Design Productivity Crisis identified by semiconductor industry, the shift in the design paradigm where the timing of a physical design will be dominated by interconnect effects, and the need for an integrated physical design system which still supports "plug-and-play" through the use of EDA standard languages, models, and interfaces.

1. INTRODUCTION

SEMATECH, a consortium focusing on advanced semiconductor manufacturing technology, is developing a new chip design system to enable chip design teams to design large complex chips in 0.25-micron technologies and beyond. This system is called the Chip Hierarchical Design System (CHDS). The genesis of CHDS can be traced to three separate factors - first, the Design Productivity Crisis (DPC) [1], identified in 1994 during a study of the future needs for design tools and capabilities to match the growth of technology as projected in the 1994 National Technology Roadmap for Semiconductors (NTRS) [2], second, the predicted shift in the design paradigm caused by the dominance of interconnect delays on design timing, and third, the need for "plug-and-play" to permit rapid and easy injection of "best-of-breed" tools, independent of their origins, into their The underlying goal is that CHDS will design flows. accommodate multiple methodologies for timing driven physical design of complex microprocessors and ASIC's.

Figure 1 presents the DPC. The upper curve shows that, as in years past, semiconductor technology is expected to grow at approximately a 58% annual compound growth rate. The lower curve shows our ability to exploit the same technology rising at 21% annual CGR. The discrete design points on this curve repre-

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sent several actual examples of design productivity spanning a time period from 1985 to 1996. The points on this chart are real data from major semiconductor manufacturers, underscoring the fact that this disparity is quite universal. The table that accompanies this graph shows that this difference has been compensated by growth in the size of design teams, with associated increases in design cost, to ensure that every new design can be completed in the same period of time. What provides urgency to the DPC is that sizes of design teams have reached their limit and future designs will need significant increases in productivity through design tools/systems to stay on the path of technology evolution as defined by the NTRS. The DPC gap will effectively increase further about the year 2002 when the number of interconnect signals that are at risk due to delays increases exponentially (Figure 1 - Equivalent Added Complexity). Note that the impact of DPC especially hits home for the greatly increasing efforts and complexity for the physical design of these chips. Most design teams' efforts for many upcoming chip designs is expected to be predominantly expended on estimated and detailed physical design.



Figure 1 - Design Productivity Crisis

Another major challenge for CHDS physical design capability is to support the design flows of all major US semiconductor manufacturers. This implies that there has to be seamless bidirectional connections between CHDS and internal EDA physical and other design tools within the member companies. This requires a level of "Plug-and-Play" that is unprecedented in EDA industry.

Section 2 describes the architecture of CHDS and explains how it addresses the three driving factors mentioned in this section. Section 3 describes the details of the Timing Driven Physical Design capabilities within CHDS. Section 4 talks about the details of Chip Parasitic Extraction and Signal Integrity Verification in support of timing driven physical design, and Section 5 discusses the use of CHDStd chip plug and play standard for physical design. Section 6 discusses conclusions about the CHDS system advances for timing driven physical design, and its impact on productivity required for large complex design for 0.25-micron and below technologies.

2. CHDS ARCHITECTURE FOR PHYSICAL DESIGN

Figure 2 shows the high-level architecture of CHDS. At first glance, it represents a classic top-down approach common to many existing systems. But there are fundamental differences between what is proposed in the fine details of CHDS and that which exists today.

Today's design systems do not possess the ability for rapid timing-driven design iterations. These systems do not handle hierarchy seamlessly, nor do they provide the ability to drive accurate physical timing parasitic and other data up to higher levels in the design process (e.g. architectural, behavioral or register-transfer design levels) so that physical effects can be accounted for earlier in the design flow. Given that timing of paths will be dominated by interconnection delays in estimated floorplans, early physical design decisions must be made more accurately. This can only be achieved if knowledge of the effects of interconnections, individually, and with coupling between each other, are available at the earliest stages of design. Hence, one of the key aspects of CHDS timing driven physical design lies in the development of improved early physical and timing estimation and later with superior accurate parasitic extraction, net timing calculation and signal integrity verification tools. This will be discussed further in Sections 3 and 4.



Figure 2 - CHDS Overall Architechture

The problem that CHDS timing driven physical design is being challenged to solve is that chip designs with up to 28M transistors must be done in the same period of time with approximately the same design team size as for today's smaller chips, and still meet the tighter timing constraints that are required by such designs. This implies at least a 4X increase in designer productivity per process generation. To achieve this goal, CHDS must provide the ability to move the design abstraction level up to RTL and behavioral level where physical, timing, and power constraints can be applied and driven forward in the design process. Early hierarchical physical design planning [3] will allow the design to be decomposed and partitioned recursively during early high-level design stages, with related physical, timing and other performance constraints apportioned accordingly. This is also the design level where decisions can be made as to which partitions of the physical design will be treated as a purely custom block, to be designed with transistor-level tools, and which partitions will be physically designed using a cell-based approach. This is also the level at which cores and pre-designed macros can be utilized for greater design productivity.

Physical design planning is closely tied into later floorplanning. Together, they form the bond between the front-end timing driven architectural, behavioral, RTL, logical, and electrical design and the back-end timing driven physical design. This will ensure that models used at different levels of the design hierarchy are consistent and that physical design timing closure is achieved in the fewest number of overall design iterations.

The design system must be hierarchically defined across the entire design process so that designers can focus on smaller number of entities at any given time and at any level of their design hierarchy. This will often also allow the tools to run faster. It is essential that hierarchy be implemented properly and completely. Given the expected complexity of designs, there often cannot be just one simple description of a design hierarchy. More likely there will be several. For instance, there may be a logical hierarchy that a system architect uses to view a design from the system point of view. A chip designer may prefer a physical hierarchy that shows how the distinct partitions will actually lie on the chip and how critical interconnections will appear as real wires on a chip. CHDS provides the structure to support the concept of divergent logical and physical hierarchies.

To provide this hierarchical capability, CHDS and CHDStd must be able to describe (i.e., populate) a single CHDStd design hierarchy consisting of both mixed logical and physical information, including references to any applicable behavioral design descriptions. With that in mind, a designer and/or EDA CHDS tools capabilities may populate a design hierarchy for the intended purpose of being viewed as 'only logical', although there will normally be some mixed-in physical design information included to support timing driven early design planning and early timing estimation. A chip designer also may, in parallel, populate an 'only physical' design hierarchy, although this will include netlist, hierarchical port-to-portinst interconnect to lower level blocks, digital timing information (rise, fall, on delay, off delay, drive, loading, et.al.) and, mixed in, test requirements and potential physical implementation constraints. Then CHDStd facilities for separate 'Logical vs Physical' hierarchies, required for many methodologies, is a matter of what is populated and what is intended for the populated CHDStd design hierarchy to mean.

CHDS therefore support designs that have a mixture of design details described using multiple hierarchies, e.g., logical, physical, test, tuned to implement a particular set of design functions. In the presence of such diverse hierarchies, it is essential that there be ways to manage correlation of design information between the hierarchies. To do this, CHDS will provide means via CHDStd to identify and track specific correlated points in design hierarchies where two hierarchies are intended to be the same. An example of this may be a logical net which has its physical counterpart implemented and identified in the physical hierarchy. By 'Tracking' these "correspondence points", timing assertions applied to a logical hierarchy can be migrated to a physical hierarchy so that CHDS timing driven physical design tools can also utilize them as constraints. Likewise, estimated or extracted data on timing, noise and other design constraints that are computed on the basis of a physical hierarchy can be backannotated to the logical hierarchy through the same "correspondence points". This approach must be complete and robust enough to support the usual forward design loop, as well as subsequent re-design and ECO processes.

Given that timing is the most important design constraint, it is important that all tools and capabilities in CHDS have a single, common (consistent) notion of delay and timing so that there can be no misinterpretation of delay and timing results between tools and levels of design. CHDS uses a common delay architecture (CDA) based on industry standards, such as Delay Calculation Language and Delay Calculation System (DCL/DCS) [4]. In addition, there must be a common interface for timing constraints, assertions and access.

"Plug-and-play" will be achieved through the use of an industrystandard information model and application programming interface (API) [5]. CHDS also assures this through use of agreed-to points in the design process where tools can be attached, independent of their origins. Section 5 describes this in more detail.

3. TIMING DRIVEN PHYSICAL DESIGN SUB-SYSTEM

Timing-driven physical design capabilities in CHDS [6] will contain major enhancements over currently available functions. All components in this area must be timing-driven, as well, as driven by or checked against other constraints (for example, power, noise, etc.). CHDS also requires greater integration with the logical/electrical design tools that would enable physical constraints to be accounted for much earlier in the design cycle. Tight linkage through the information model to the extraction and related tools (Section 4 below) will allow rapid back-annotation of timing and other data to higher levels of design. "Plug-andplay" will allow tools from other sources to be plugged in to satisfy the needs of the designers. Finally, the tools have a modularity that allows multiple methodologies to be supported, based on design intent and environment. Following are details of the individual capabilities required for physical design of chips that will contain 28M transistors (in .25u technologies) and much more for later technologies. The underlying message of CHDS and its PD capabilities is that improving the accuracy in early decision-making will reduce the number of design iterations, and thus, design time.

One of the looming issues for future designs is the use of "cores" containing intellectual property (such as, microprocessors). CHDS physical design must be capable of handling these IP cores as "black boxes" using the required information associated with them - their shapes and dimensions, timing models, existing routing patterns inside them, blockages, feed-throughs",... The

floorplanner and all subsequent PD tools must accept these cores as entities whose internal design is fixed and yet be able to design with it, around it and above it.

The floorplanner [3] is expected to provide a spectrum of capabilities that start at the design planning stage to work with behavioral/RT-levels of design in doing area planning and block sizing to details of block shaping. It must be capable of handling a distinct physical hierarchy and be able to bridge to/from a different logical hierarchy. This will be a marked improvement over what exists today. It must be able to traverse through the physical hierarchy in progressively detailing the floorplan blocks. To support both top-down and bottom-up methodologies, it must have the capability to perform assignment of pins at the chip and macro levels such that this assignment of pins at any level of hierarchy. Alternately, the placement of blocks at any level of hierarchy can drive the assignment of pins in the blocks at the next higher level in the hierarchy.

The floorplanner will have a global router that not only creates the global routes for a down-stream detailed router but can be used to ensure an optimum floorplan which will meet timing constraints based on the global routes. These global routes can also be used to estimate R-C values to much greater accuracy than is achievable today. Global routing will also allow more accurate estimation of congestion and power analysis. The floorplanner must have associated clock and power bus design capabilities that tie in with detailed clock and power routing tools. Few design groups agree on what constitutes the best clock or power design. So, the latter will be only a base capability, agreed to with the SEMATECH member companies, that serves as a framework to insert new methods that will be more context-sensitive to the particular design philosophy and the designer. Finally, the floorplanner must be able to link through the information model (Section 5) to enterprise-specific design tools, such as, data path, transistor-level or library design tools, such that specific floorplanned functional blocks can be designed in ways that are specific to a particular design or enterprise.

Placement is considered an extension of floorplanning but this is also an area where a customer can plug in his own placement capabilities. However, in the case of the latter, it is likely that there may be some performance penalties since it will not have access to the same run-time model as the floorplanner. Placement will run against very much the same constraints as floorplanning except that it is at a detailed level and must pay much greater focus on technology constraints, e.g., legality of placement, orientation of circuits, etc. Detailed clock placement capabilities must ensure that clock buffers are placed such that the likelihood of zero-skew clocking to all storage elements driven by a common clock is maximized. This is as much an issue of methodology as capabilities of particular tools. The same global router discussed above is also available here as well to both refine the placement and the global routes so that design constraints can be met, such as, timing, wirability, congestion, and power as well as to allow more accurate R-C estimation.

Detailed routing is expected to follow both the constraints defined by the user and those from floorplanning and placement. This is also a point in the design system where a user may choose to insert his own particular router provided it is capable of accepting constraints from the upstream processes. Routing is a key function in that it is the last tool that ensures that all design constraints are met and it also produces the output that parasitic extraction and signal integrity checking tools can utilize to do detailed analysis of the final result. Closely connected to detailed routing are the clock and power routing capabilities. Both these capabilities are very design-specific. Thus, these capabilities will provide basic functions to be determined in concert with SEMATECH member companies and will serve as a framework to insert additional methods that will be more context-sensitive to the particular design philosophy and the designer. All routing capabilities will connect to a rich set of extraction and checking capabilities described in the following section.

4. CHIP PARASITIC EXTRACTION AND SIGNAL INTEGRITY VERIFICATION

As feature sizes scale down and chip sizes grow [2,8], interconnect becomes a dominant factor in determining timing in deep submicron circuits. It is necessary to model interconnect more accurately in order to increase the accuracy of timing analysis and signal integrity verification. An increasing amount of time is spent on verification at the back end of the line. The verification process, however, requires a great deal of user intervention. A higher level of automation supported by a well integrated CAD environment as well as more accurate and efficient algorithms for point tools are needed to address functionality, performance and design productivity.

Presently available commercial products lack interconnect solutions with predictable error bounds, process variations and speed versus accuracy trade-offs in an integrated environment. CHDS will address these issues and improve on the conventional solutions in the following areas:

- Allow variable accuracy parasitic extraction and interconnect timing calculation in a single integrated environment. 3-D effects on capacitance will be computed with realistic geometric modeling of multi-level metal systems. Accuracy will be traded off for efficiency for non-critical nets.
- Provide error bounds for models at each computation step leading to interconnect delays, including parasitic extraction and delay calculation. Error bounds will increase the confidence level of the verification process.
- Provide a two-way interface between timing analysis and parasitic extraction. Acknowledging that it is not feasible to extract very accurate parasitic models for all interconnect on a chip, CHDS will automatically identify which nets to extract to higher accuracy.
- Allow computation of sensitivities of parasitic and interconnect timing parameters due to process variations. This is key to predictable product performance analysis as interconnect delay dominates performance.
- Provide tight integration between parasitic extraction, signal integrity verification, and power network distribution analysis (Fig. 3).
- Provide interconnect models and signal integrity design rules for use by physical and electrical design tools. Parasitic estimation models will be generated automatically using the same technology information used for post-layout verification to ensure timing closure. Physical level signal integrity rules will be generated from electrical design specs.

CHDS offers a single integrated environment to perform parasitic extraction, net timing calculations, signal integrity verification. Described below are the salient features of each of the capabilities in this analysis.



Figure 3 - CPE & SIV Architecture

Net Parasitic Extraction (NPE)

Net Parasitic Extraction addresses needs for different phases of design and for different levels of accuracy requirements for timing and signal integrity analysis. CHDS parasitic extraction will cover a full range from a fast full-chip extraction through detailed 3-D analysis for selected nets in the design. Technology details of multi-level interconnect systems such as anisotropic and conformal dielectrics, and irregular conductors will be considered during the extraction to accurately model the technology. Since interconnect will dominate product performance, sensitivity due to process variations will also be computed throughout the range of parasitic extraction methods. Error bounds will be computed for resistance and capacitance of each net to guide the accuracy of performance analysis. Detailed interconnect parasitics will be compacted considering both timing and signal integrity verification perspectives.

Net Timing Calculation (NTC)

Net Timing Calculation involves computation of timing parameters such as delays, edge rates and skews. Instead of using trapezoidal signal waveforms, general waveform parameters will be used to accurately model signal characteristics. Timing parameters will be computed to required levels of accuracy by appropriately choosing driver and interconnect models. Error bounds computed on parasitic resistance and capacitance will be used to compute error bounds on timing parameters. The effect of crosstalk from adjacent signals on delay will be comprehended by interfacing with timing analysis for signal transition information.

Signal Integrity Verification (SIV)

Crosstalk effects due to coupling capacitance in deep submicron designs could cause catastrophic failures in functionality of the design. Signal integrity verification will include detection of false switching, as well as the deterioration of the signal (e.g., increase in delay, edge rate) due to crosstalk. A set of sophisticated filtering mechanisms, taking into account the temporal correlation between signals will be used to identify potential signal integrity violations. Current densities on signals lines will be checked against electromigration rules to ensure reliability.

Power Distribution Network Analysis (PDNA)

The Power Distribution Network Analysis system will generate an accurate electrical model for the power distribution network, compute average and peak voltage drops at ports and check for electromigration violations on the network. Accurate timing information from the persistent information base will be used to take into account temporal correlation in determining peak current drives.

Transistor Level Timing (TLT)

Transistor Level Timing works either in conjunction with the Net Timing Calculator or as a stand alone tool. TLT can be used for custom blocks (including dynamic logic), sensitive nets (clocks, etc.) or whenever the specified net timing accuracy requires NTC to invoke this capability. The output of TLT can either be DCL or a pin-to-pin delay value, including error bounds.

Integration with Electrical and Physical Design

Unique value of the CHDS system is the ability to share information between different point tools needed to perform accurate analysis. The Net Parasitic Extraction, Net Timing Calculation and Signal Integrity Verification are closely linked to global static timing analysis and physical design through the persistent database, CHDStd (Fig. 4). For example, signal switching information which is crucial for signal integrity verification is obtained from global static timing analysis and accuracy of the timing analysis itself is improved by accurate net timing calculation.



Figure 4 - Integration of CPE & SIV with CHDS

5. STANDARD INFORMATION MODEL AND "PLUG-AND-PLAY"

CHDS includes a new chip representation standard for the technical design data used within CHDS and is known as CHDStd. The CHDStd standard is defined by a semantic information model of the design information covered in CHDS and an Application Program Interface (API) (i.e., software call interface) that is used by all CHDS tools. The Integrated Data Model (IDM) and API's [9] from IBM was selected as the starting point for developing CHDStd. All data required by CHDS applications will be stored into CHDStd and accessed via the CHDStd API in a form that satisfies the completeness of information types and efficiency in representation to ensure that

data storage and retrieval has minimal effect on application performance. CHDS assumes that certain applications that are part of a tight design loop may interact with each other through a highperformance common run-time model that is optimized to the context of its use. All run-time data is derived from and returned to the persistent CHDStd database via the API.



Figure 5 - CHDStd Architecture

Figure 5 shows a high-level architectural view of the CHDStd persistent database and API. All CHDS applications communicate with the database through the standardized CHDStd API. On the persistent database side, API calls are mapped through interface code into calls that can be CHDStd database implementation specific. Part of the integration of CHDS into any EDA system is generation of the code that implements the bidirectional connection between the API interface and the specific database within the host EDA system.

The initial version of CHDStd will be a union of the data (API semantics definition and call definitions) contained in IDM and the Delay Calculation Language (DCL) [4] and the related Delay Calculation System (DCS). Phased development will extend both the API and data content to subsume current international and de facto standards (e.g. EDIF, LEF/DEF, PDEF) so that CHDStd can be generalized to satisfy the chip design needs of the EDA industry.

CHDStd provides EDA applications (in-house and third party suppliers) with facilities to access both hierarchical and occurrence design information. This capability is very important as groups of tools set up common runtime access to occurrence specific views and work off of them together. This facility, together with direct API access to EDA design information, will greatly eliminate the read/parse/correlate/use/write paradigm in use today by EDA tools doing ASIC design. This architectural change provided by the CHDS infrastructure will greatly facilitate large design teams concurrent use of CHDS tools while working on different parts of large complex chips.



Figure 6 - CHDS System - Overall Plug and Play

Figure 6 shows how CHDS will support "Plug-and-Play". As mentioned before, all information required by CHDS applications will be contained in CHDStd directly or in some derived form to achieve storage efficiency and performance. Based on this assumption, there are some natural areas where some tools will operate in a tight loop within CHDS. One such area involves synthesis, floorplanning, placement, and timing. However, a physical design routing tools for signal, clock, power and ground connections may come from any source and be integrated into CHDS through CHDStd. Note that, while placement tools can also be connected to CHDS, there may be a potential loss of performance, since a foreign placement tool may not be integrated with the run-time data used within CHDS synthesis-floorplanning loops. Another specific area where CHDS provides "plug-andplay" benefits is in physical design verification. CHDS includes no specific solutions, but rather expects multiple supplier verification solutions to become available to users of CHDS. CPE/SIV also connects to the rest of CHDS through CHDStd which offers plug and play opportunities for using other parasitic extraction and timing capabilities within CHDS.

6. CONCLUSIONS

CHDS comprises both a long-range vision and a near-term solution for meeting the design productivity crisis for 0.25u technologies and beyond. The detailed requirements define significant enhancements in the capabilities for physical design, parasitic extraction and checking to ensure that designs can be achieved to meet the projected high operating frequencies and to meet constraints, for example, for power and noise. There are implied significant changes in design processes to account for physical phenomena at earlier levels of design but at the same time, there is an assumption that CHDS must accommodate multiple design methodologies to best suit the design at hand. "Plug-and-play" through the use of a hierarchical chip design standard is a central theme to allow capabilities from outside the CHDS definition to be inserted as alternatives or to provide specific additional capabilities that are quite often considered enterprise-specific, such as, data path, transistor-level, or library design capabilities.

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