Circuit Methods for the Integration of Low Voltage (1.1-1.8V) Analog Functions on System-on-a-Chip IC's in a Single-Poly CMOS Processes

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1. ABSTRACT

Several new building blocks are demonstrated, which enable low-power (1.1-1.8V) analog functionality in a single-poly, digital CMOS process. These cells facilitate the integration of analog converters on system-on-a-chip IC's without adding any extra cost to the process. A voice A/D, designed with these circuits, exhibited an SNR of 68 dB at an analog supply voltage of 1.1V, and 75dB at 1.8V. This is despite the noisy digital environment of an on-chip DSP operating at 60 Mhz and a digital supply voltage of 2.5V.

2. INTRODUCTION

There has recently been an increasing need to develop system-on-a-chip capability. This presents a special challenge for the design of analog blocks, since the switching noise on high frequency digital chips can severely degrade analog performance at the transistor and building block level. Futhermore, in many applications, such as DSP's and microcontrollers for wireless systems, the tendency has been to save power in the digital part by reducing the supply voltage (1.8V in the next generation). This complicates integrated analog functions, since many of the analog methods, such as stacked Vt's, can not be utilized. The low power requirement also requires a reduction in the VDSAT values, which makes the transistors more sensitive to digital noise. The conflicting requirements of low power and switching noise immunity make designing analog circuits an especially difficult task. Thus, the realization of analog functions integrated onto digital chips requires a rethinking of many of the analog building blocks.

Motorola has recently reported a DSP with an integrated voice codec which was fabricated with a standard digital CMOS process [1]. This process had no special analog additions, such as double-poly or salicide block. It thus utilized non-linear MOS capacitors and non-linear nwell resistors. Usage of a "pure" digital process makes the analog integration significantly more cost-effective, since in system IC's the analog part accounts for typically 3-5% of the area, and the added cost of the analog process (i.e. double poly and salicide block) would be imposed on the entire chip. In addition, the digital processes typically are qualified 6 months - 1 year before the analog processes. Thus, using a digital process improves the time-to-market when the IC's have an aggressive shrink path.

The analog part of this chip was functional down to 1.1V, and was highly insensitive to the digital noise while the DSP was operating at 60 MHz. In this paper, the circuit design approach for this technology, and its analog building blocks are reported for the first time.

3. ARCHITECTURE AND BUILDING BLOCKS

In standard sigma-delta converters, switched capacitor techniques are generally utilized. However, these types of methods are very deficient in the presence of digital noise. This is because a voltage is being sampled at a specific time point. Digital spikes are also sampled at this time and can be aliased back into the pass-band, causing a degradation of the analog performance. In the approach discussed here, a continuous, current steering method is used. In this mode, there is more averaging and filtering of the digital noise, and it has less of an effect on the analog performance. A sample architecture of the analog part of an A/D converter which uses this type of methodology is shown in fig. 1. This A/D is a single bit, first order sigma-delta modulator. The digital section of the A/D (not shown) contains a third order comb filter as well as a subtractive dither generator which is fed back to the analog part to reduce any periodic compo-

nents of the noise. More discussions about the digital portion of the A/D can be found in reference [1].

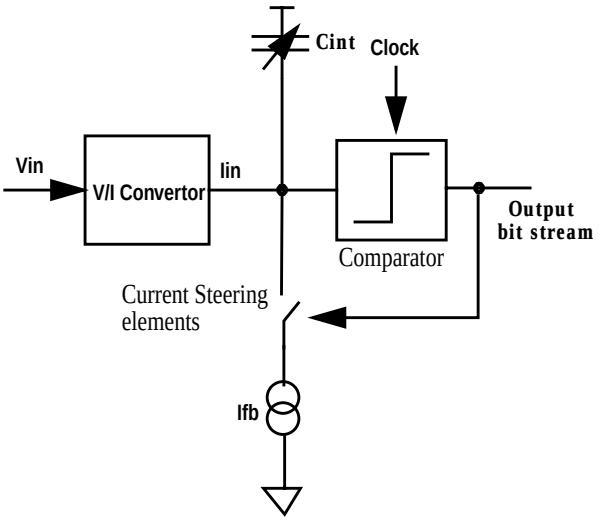

Figure 1: A/D Architecture

The integration capacitor in figure 1 is a MOS capacitor, since the process used is a single poly, standard digital CMOS process. The A/D architecture does not require this capacitor to be linear. Special care is taken to insure charge conservation on the capacitor so that information is not lost. The capacitor is separated from the current steering switch (see Fig. 1) by several folding and cascode stages.

3.1 Linear Voltage to Current Converter

In order to minimize distortions in the current signal, it is necessary to convert voltage signals into current (and current to voltage) in a linear fashion. A simplified circuit schematic of the linear voltage to current converter (V/I) is shown in fig. 2.

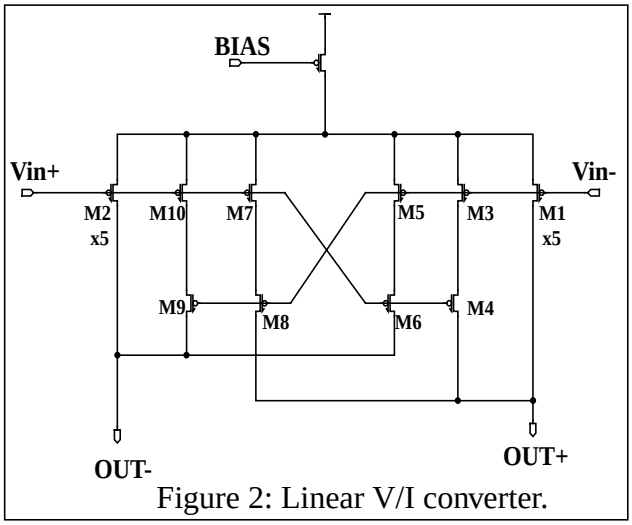

Figure 2: Linear V/I converter.

This V/I compensates for reduction in the gm of a differential pair by increasing the tail current. The gm remains more constant over the dynamic range, thus reducing the non-linearity. Transistors M1 and M2 in fig. 2 are the main "differential pair", while M3 - M10 are the compensation transistors. When the differential input is increased, at least one of the transistors on each compensation path begins to close, which reduces the current in that respective path. This forces more current into M1 and M2 and compensates for the gm reduction. The compensation paths are arranged such that the outputs are symmetrical with regards to the inputs.

The simulated spectrum of the differential current output for a sinusoidal voltage input is shown in fig. 3 for Vin=140mV, f=1MHz and a tail current of 3uA.

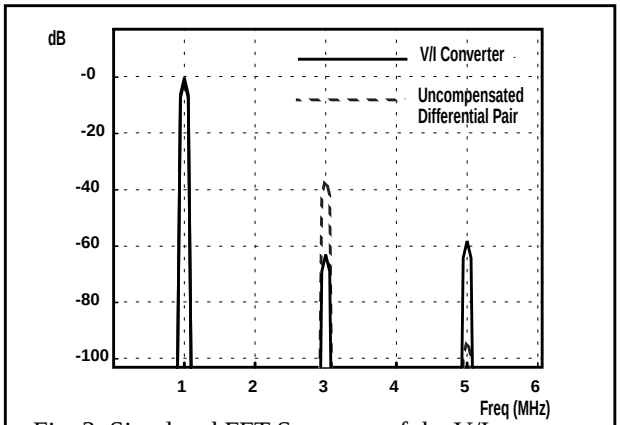

Fig. 3: Simulated FFT Spectrum of the V/I converter.

This spectrum is compared to that of an uncompensated differential pair of similar sizing. The V/I shows an improvement in distortions of > 20dB. This is true for all process corners and conditions. The V/I is a low current, low voltage (Vt + 2Vdsat) circuit, and operates at high frequencies with relatively low noise, and thus has significant advantages over other linearization methods. It is also possible to achieve linearization by cross coupling the outputs of two differential pairs [2]. However, this method significantly adds noise. In the present method, most of the current goes into the signal path, and thus the increase in noise is less than 15% comparing to a differential pair. It is also possible to achieve linearization with low-noise using adaptive biasing [2]. However, as this method contains a long compensation path, it is limited to lower frequencies or high currents. In noise-critical applications, it is possible to eliminate the noise contribution of the compensation paths entirely by connecting them to GND (instead of to the outputs as in fig. 2). In this case, however, the common mode output will be dependent on the differential signal, and will have to be compensated for.

It should be noted that the V/I can also be used as a voltage to current converter, or as a gm stage by connecting the inputs

to the outputs. Such gm stages are used as Gm/C filters. In these two applications, there will also be a 10x improvement in the linearity.

3.2 Constant Dynamic Range Biasing

In addition to enabling linearization, it is important that the V/I converter remain within its linear range for all process corners and conditions. Furthermore, it is highly desirable to maximize this range. This is accomplished by using a constant-dynamic-range bias. A simplified schematic of this circuit is shown in fig. 4, and its concept of operation is illustrated in fig. 5.

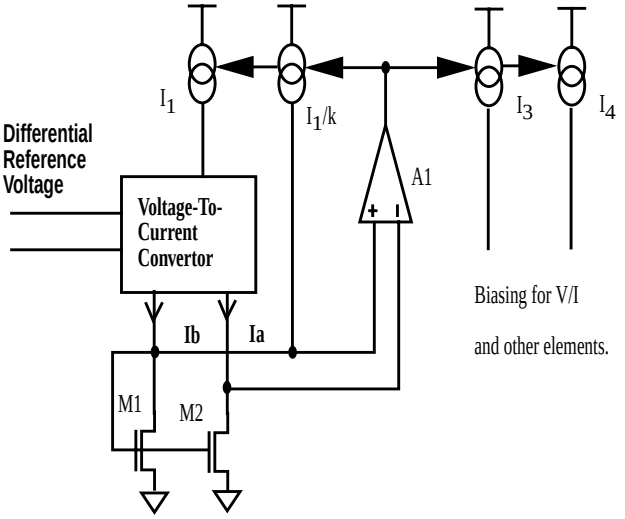

Fig. 4: Constant Dynamic Range Biasing

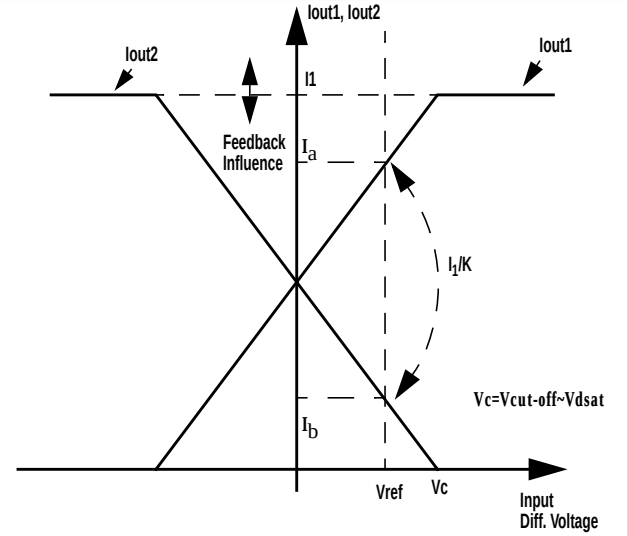

Fig. 5: Illustration of constant dynamic range bias.

The circuit utilizes the V/I converter shown in fig. 2, as well as a differential reference voltage provided by an on-chip bandgap reference. The feedback loop, provided by amplifier A1 fixes the difference between the differential output currents as follows:

$$I_a - I_b = gm * V_{ref} = I_1/K \qquad (1)$$

It is also true that:

$$I_a + I_b = I_1 \qquad (2)$$

Putting (1) and (2) together, the following is derived:

$$I_1 = gm * k * V_{ref} \qquad (3)$$

In order for (3) to be true, it is required that Vc, the cutoff voltage, be constant regardless of gm (fig. 5). And since Vc determines the dynamic range, this implies that the dynamic range is fixed for all process corners and conditions. The bias thus provides a maximized current output for all process variations and conditions, while simultaneously allow the V/I to remain in its linear range in all of these cases.

3.3 Equal GM Current Sources

All current-mode circuits require matched current sources and current mirrors with multiplication factors. In order for the current sources/mirrors to operate correctly when there are digital spikes, their gm's must be identical. This allows the spike to affect each current source in a similar manner. When the transistors are operating in strong inversion, current multiplication can be achieved simply by multiplying the magnitude of transistors on either side of a current mirror. However, in the case of low voltage designs, such as the present one, the transistors often operate in the region between strong and weak inversion for many or all of the process conditions. In those instances simple scaling does not guarantee an identical gm. Thus, a methodology must be established for equal-gm current mirrors, regardless of whether they are in strong inversion, and where the mirrors have different currents.

A circuit which enables this is shown in fig. 6. In this schematic, all transistors with the same number are matched (i.e. M1A=M1B=M1C=M1D). The low and high current differential pairs (M1A, M1B and M2A,M2B respectively) are separated by a voltage V. The transistors M1C, M1D, M2C, and M2D define currents Ia and Ib such that:

$$I_a - I_b = 2*(GM1-GM2)*V \qquad 4)$$

where GM1 and GM2 are the transconductances of low and high current differential pairs. In addition, M5A and M5B cause the following relation to be true:

$$I_a = I_b \qquad (5)$$

In order for both (5) and (6) to be true, it is necessary that GM1 be identical to GM2. This is true even if the nchannels are not in strong inversion. The feedbacks in the circuit

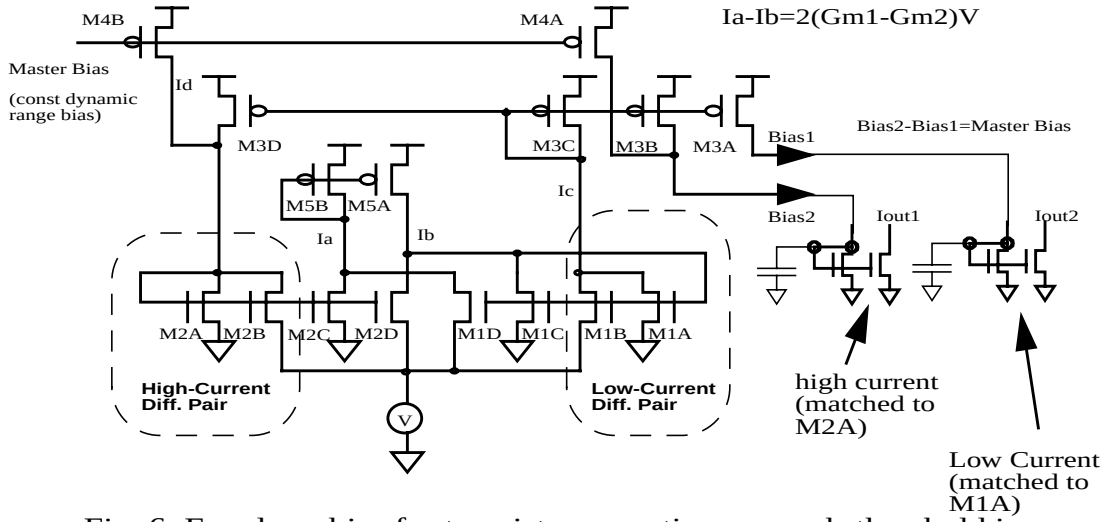

Fig. 6: Equal gm bias for transistor operation near sub-threshold in the presence of substantial digital noise.

enable all the transistors to be in saturation, allowing the circuit to correctly implement equations (4) and (5).

The outputs of the circuit are generated by transistors M3A and M3B. The difference between these two currents are equal to Id, the master bias, and the n-channels which generate them have identical gm's. These current sources are used in the current steering elements of the converters (see fig. 1).

It should be noted that in order for the circuit to operate, the W/L ratio of the M2 transistors must be smaller than that of the M1 set. This is because the M2's have a higher current going through them. Thus, if their W/L ratio were larger, it would be impossible for GM1 to be equal to GM2.

3.4 Measured Results

A voice A/D converter was designed using the building blocks described above. It's digital output was measured using Audio Precision System One equipment for an analog sinusoidal input at 1kHz. The measurement was performed while the on-chip DSP (from the Motorola 56600 family) was operating at 60 MHz and a digital supply voltage of 2.5V to create a highly noisy environment. The measured DFT spectrum is shown in fig. 7 for an analog supply voltage of 1.1 V. At this supply voltage, the A/D exhibited a THD of 55dB and SNR of 68dB also in the presence of the digital noise. At 1.8V, the A/D shows distortions under 55dB and an SNR of 75dB. The THD is limited by the non-linear nwell resistors used to divide the input voltage before the V/I converter (fig. 1). These are the only available resistors in the digital CMOS process. Under nominal conditions, the A/D consumes 60uA of current. The CMOS process was a standard 0.35 um, 70 A gate oxide single poly process.

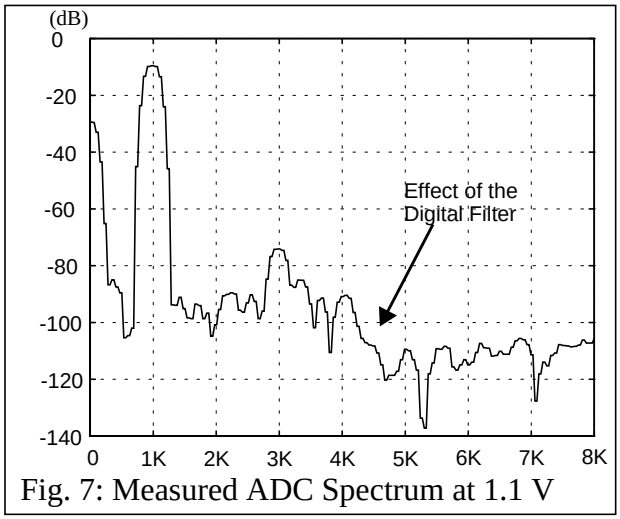

Fig. 7: Measured ADC Spectrum at 1.1 V

4. CONCLUSIONS

Several new building blocks for mixed signal system-on-a-chip IC's have been demonstrated. These analog circuits are highly insensitive to noise associated with digital switching and operate at very low power (1.1 to 1.8V). This technology enables integration of analog blocks with high performance DSP's and microcontrollers, without significant degradation of the analog functionality.

5. REFERENCES

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2) "Analogue IC Design: A Current Mode Approach" C. Toumazou, F.J. Lidgey and D.G. Haigh eds. (Peter Peregrinus, publisher; IEE, London, UK, 1990) pp. 181.