Topology-induced Enhancement of Mappings*

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ABSTRACT

In this paper we propose a new method to enhance a mapping $\mu(\cdot)$ of a parallel application's computational tasks to the processing elements (PEs) of a parallel computer. The idea behind our method TIMER is to enhance such a mapping by drawing on the observation that many topologies take the form of a partial cube. This class of graphs includes all rectangular and cubic meshes, any such torus with even extensions in each dimension, all hypercubes, and all trees.

Following previous work, we represent the parallel application and the parallel computer by graphs $G_a = (V_a, E_a)$ and $G_p = (V_p, E_p)$. G_p being a partial cube allows us to label its vertices, the PEs, by bitvectors such that the cost of exchanging one unit of information between two vertices u_p and v_p of G_p amounts to the Hamming distance between the labels of u_p and v_p .

By transferring these bitvectors from V_p to V_a via $\mu^{-1}(\cdot)$ and extending them to be unique on V_a , we can enhance $\mu(\cdot)$ by swapping labels of V_a in a new way. Pairs of swapped labels are local w.r.t. the PEs, but not w.r.t. G_a . Moreover, permutations of the bitvectors' entries give rise to a plethora of hierarchies on the PEs. Through these hierarchies we turn TIMER into a hierarchical method for improving $\mu(\cdot)$ that is complementary to state-of-the-art methods for computing $\mu(\cdot)$ in the first place.

In our experiments we use TIMER to enhance mappings of complex networks onto rectangular meshes and tori with 256 and 512 nodes, as well as hypercubes with 256 nodes. It turns out that common quality measures of mappings derived from state-of-the-art algorithms can be improved considerably.

KEYWORDS

multi-hierarchical mapping; parallel communication optimization; partial cube; Hamming distance

1 INTRODUCTION

Large-scale matrix- or graph-based applications such as numerical simulations [30] or massive network analytics [25] often run on parallel systems with distributed memory. The iterative nature of the underlying algorithms typically requires recurring communication between the processing elements (PEs). To optimize the running time of such an application, the computational load should be evenly distributed onto the PEs, while at the same time, the communication volume between them should be low. When mapping processes to PEs on non-uniform memory access (NUMA) systems, it should also be taken into account that the cost for communication operations depends on the locations of the PEs involved. In particular, one wants to map heavily communicating processes "close to each other".

More formally, let the application be modeled by an *application* graph $G_a = (V_a, E_a, \omega_a)$ that needs to be distributed over the PEs. A vertex in V_a represents a computational task of the application, while an edge $e_a = \{u_a, v_a\}$ indicates data exchanges between tasks u_a and v_a , with $\omega_a(e_a)$ specifying the amount of data to be exchanged. The topology of the parallel system is modeled by a processor graph $G_p = (V_p, E_p, \omega_p)$, where the edge weight $\omega_p(\{u_p, v_p\})$ indicates the cost of exchanging one data unit between the PEs u_p and v_p [8, 11]. A balanced distribution of processes onto PEs thus corresponds to a mapping $\mu : V_a \mapsto V_p$ such that, for some small $\varepsilon \ge 0$,

$$|\mu^{-1}(v_p)| \le (1+\varepsilon) \cdot \lceil |V_a|/|\mu(V_a)|\rceil \tag{1}$$

for all $v_p \in \mu(V_a)$. Therefore, $\mu(\cdot)$ induces a balanced partition of G_a with blocks $\mu^{-1}(v_p)$, $v_p \in V_p$. Conversely, one can find a mapping $\mu : V_a \mapsto V_p$ that fulfills Eq. (1) by first partitioning V_a into $|V_p|$ balanced parts [2] and then specifying a one-to-one mapping from the blocks of the partition onto the vertices of G_p . For an accurate modeling of communication costs, one would also have to specify the path(s) over which two vertices communicate in G_p . This is, however, system-specific. For the purpose of generic algorithms, it is thus often abstracted away by assuming routing on shortest paths in G_p [12]. In this work, we make the same assumption.

In order to steer an optimization process for obtaining good mappings, different objective functions have been proposed [8, 12, 17]. One of the most commonly used [24] objective functions is $Coco(\cdot)$ (also referred to as *hop-byte* in [33]), cf. Eq. (3):

$$\mu^* := \underset{\substack{\mu: V_a \mapsto V_p \\ \mu \text{ balance}}}{\operatorname{argmin}} \operatorname{Coco}(\mu), \text{ with } (2)$$

$$\operatorname{Coco}(\mu) := \sum_{\substack{\mathbf{e}_a \in E_a \\ e_a = \{u_a, v_a\}}} \omega_a(e_a) \, d_{G_p}(\mu(u_a), \mu(v_a)), \tag{3}$$

where $d_{G_p}(\mu(u_a), \mu(v_a))$ denotes the distance between $\mu(u_a)$ and $\mu(v_a)$ in G_p , *i. e.* the number of edges on shortest paths. Broadly speaking, Coco(·) is minimised when pairs of highly communicating processes are placed in nearby processors. Finding $\mu^*(\cdot)$ is \mathcal{NP} -hard. Indeed, finding $\mu^*(\cdot)$ for a complete graph G_p amounts to graph partitioning, which is an \mathcal{NP} -hard problem [10].

Related work and motivation. One way of looking at previous algorithmic work from a high-level perspective (more details can be found in the overview articles by Pellegrini [24], Buluç *et al.* [4], and Aubanel [1]) is to group it into two categories. One line has tried to couple mapping with graph partitioning. To this end, the objective function for partitioning, usually the edge cut, is replaced by an objective function like $Coco(\cdot)$ that considers distances $d_{G_p}(\cdot)$ [32]. To avoid recomputing these values, Walshaw and Cross [32] store them in a *network cost matrix* (NCM). When our proposed method TIMER (Topology-induced Mapping Enhancer) is used to enhance

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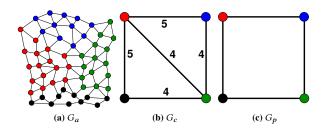


Figure 1: (a) Application graph partitioned into four blocks with unitary edge weights. (b) Resulting communication graph, numbers indicate edge weights. (c) The processor graph is a partial cube and the bijection $v(\cdot)$ between the vertices of G_c and those of G_p is indicated by the colors. Communication between the red and the green vertex has to be routed via an intermediary node (the blue one or the black one).

a mapping, it does so without an NCM, thus avoiding its quadratic space complexity.

The second line of research decouples partitioning and mapping. First, G_a is partitioned into $|G_p|$ blocks without taking G_p into account. Typically, this step involves multilevel approaches whose hierarchies on G_a are built with edge contraction [15, 20, 27] or weighted aggregation [6, 19]. Contraction of the blocks of G_a into single vertices yields the communication graph $G_c = (V_c, E_c, \omega_c)$, where $\omega_c(e_c)$, $e_c \in E_c$, aggregates the weight of edges in G_a with end vertices in different blocks. For an example see Figures 1a,1b. Finally, one computes a bijection $v : V_c \mapsto V_p$ that minimizes $Coco(\cdot)$ or a related function, using (for example) greedy methods [3, 8, 11, 12] or metaheuristics [3, 31], see Figure 1c. When TIMER is used to enhance such a mapping, it modifies not only $v(\cdot)$, but also affects the partition of V_a (and thus possibly G_c). Hence, deficiencies due to the decoupling of partitioning and mapping can be compensated. Note that, since TIMER is proposed as an improvement on mappings derived from state-of-the-art methods, we assume that an initial mapping is provided. This is no limitation: a mapping can be easily computed from the solution of a graph partitioner using the identity mapping from G_c to G_p .

Being man-made and cost-effective, the topologies of parallel computers exhibit special properties that can be used to find good mappings. A widely used property is that PEs are often "hierarchically organized into, e. g., islands, racks, nodes, processors, cores with corresponding communication links of similar quality" [29]. Thus, dual recursive bisection (DRB) [22], the recent *embedded sectioning* [18], and what can be called recursive multisection [5, 14, 29] suggest themselves for mapping: DRB and embedded sectioning cut both G_a (or G_c) and G_p into two blocks recursively and assign the respective blocks to each other in a top-down manner. Recursive multisection as performed by [29] models the hierarchy inherent in G_p as a tree. The tree's fan-out then determines into how many blocks G_c needs to be partitioned. Again, T1MER is complementary in that we do not need an actual hierarchy of the topology.

Overview of our method. To the best of our knowledge, TIMER is the first method to exploit the fact that many parallel topologies are partial cubes. A partial cube is an isometric subgraph of a hypercube, see Section 2 for a formal definition. This graph class includes all rectangular and cubic meshes, any such torus with even extensions in each dimension, all hypercubes, and all trees.

 G_p being a partial cube allows us to label its vertices with *bitvec*tors such that the distance between two vertices in G_p amounts to the Hamming distance (number of different bits) between the vertices' labels (see Sections 2 and 3). This will allow us to compute the contribution of an edge $e_a \in E_a$ to $\text{Coco}(\cdot)$ quickly. The labels are then extended to labels for vertices in G_a (Section 4). More specifically, a label of a vertex $v_a \in V_a$ consists of a left and a right part, where the left part encodes the mapping $\mu(\cdot) : V_a \mapsto V_p$ and the right part makes the labels unique. Note that it can be instructive to view the vertex labels of V_a , $l_a(\cdot)$, as a recursive bipartitioning of V_a : the *i*-th leftmost bit of $l_a(v_a)$ defines whether v_a belongs to one or the other side of the corresponding cut in the *i*-th recursion level. Vertices $u_a, v_a \in V_a$ connected by an edge with high weight should then be assigned labels that share many of the bits in the left part.

We extend the objective function $\text{Coco}(\cdot)$ by a factor that accounts for the labels' right part and thus for the uniqueness of the label, We do so without limiting the original objective that improves the labels' left part (and thus $\mu(\cdot)$) (Section 5). Finally, we use the labeling of V_a to devise a multi-hierarchical search method in which label swaps improve $\mu(\cdot)$. One can view this as a solution method for finding a $\text{Coco}(\cdot)$ -optimal numbering of the vertices in V_a , where the numbering is determined by the labels.

Compared to simple hill-climbing methods, we increase the local search space by employing very diverse hierarchies. These hierarchies result from random permutations of the label entries; they are imposed on the vertices of G_p and built by label contractions performed digit by digit. This approach provides a fine-to-coarse view during the optimization process (Section 6) that is orthogonal to typical multilevel graph partitioning methods.

Experimental results. As the underlying application for our experiments, we assume parallel complex network analysis on systems with distributed memory. Thus, in Section 7, we apply TIMER to further improve mappings of complex networks onto partial cubes with 256 and 512 nodes. The initial mappings are computed using KAHIP [28], SCOTCH [23] and LIBTOPOMAP [12]. To evaluate the quality results of TIMER, we use Coco(·), for which we observe a relative improvement from 6% up to 34%, depending on the choice of the initial mapping. Running times for TIMER are on average 42% faster than the running times for partitioning the graphs with KAHIP.

2 PARTIAL CUBES AND THEIR HIERARCHIES

The graph-theoretical concept of a partial cube is central for this paper. Its definition is based on the hypercube.

Definition 2.1 (Hypercube). A dim_H -dimensional hypercube H is the graph $H(V_H, E_H)$ with $V_H := \{0, 1\}^{dim_H}$ and $E_H := \{\{u_H, w_H\} u_H, v_H \in V_H$ and $d_h(u_H, v_H) = 1\}$, where $d_h(u_H, v_H)$ denotes the Hamming distance (number of different bits) between u_H and v_H .

More generally, $d_H(u_H, v_H) = d_h(u_H, v_H)$, *i. e.*, the (unweighted) shortest path length equals the Hamming distance in a hypercube.

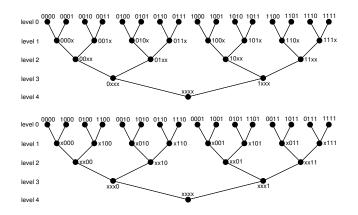


Figure 2: Two opposite hierarchies of the 4D hypercube. "x" means "0" or "1". Top: hierarchy H_{π} with $\pi = (1, 2, 3, 4)$. Bottom: hierarchy H_{π} with $\pi = (4, 3, 2, 1)$.

Partial cubes are isometric subgraphs of hypercubes, *i. e.*, the distance between any two nodes in a partial cube is the same as their distance in the hypercube. Put differently:

Definition 2.2 (Partial cube). A graph G_p with vertex set V_p is a partial cube of dimension dim_{G_p} if (i) there exists a labeling $l_p : V_p \mapsto \{0, 1\}^{dim_{G_p}}$ such that $d_{G_p}(u_p, v_p) = d_h(l_p(u_p), l_p(v_p))$ for all $u_p, v_p \in V_p$ and (ii) dim_{G_p} is as small as possible.

The labeling $l_p : V_p \mapsto \{0, 1\}^{dim_{G_p}}$ gives rise to hierarchies on V_p as follows. For any permutation π of $\{1, \ldots, dim_{G_p}\}$, one can group the vertices in V_p by means of the equivalence relations $\sim_{\pi, i}$, where $dim_{G_p} \ge i \ge 1$:

$$u_p \sim_{\pi, i} v_p :\Leftrightarrow \pi(l_p(u_p))[j] = \pi(l_p(v_p))[j] \tag{4}$$

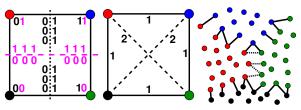
for all $1 \le j \le i$ (where l[i] refers to the *i*-th character in string *l*). As an example, $\sim_{id,i}$, where *id* is the identity on $\{0,1\}^{dim_{G_p}}$, gives rise to the partition in which u_p and v_p belong to the same part if and only if their labels agree at the first *i* positions. More generally, for each permutation $\pi(\cdot)$ from the set $\prod_{dim_{G_p}}$ of all permutations on $\{1, \ldots, dim_{G_p}\}$, the equivalence relations $\sim_{\pi,i}$, $dim_{G_p} \ge i \ge 1$, give rise to a hierarchy of increasingly coarse partitions ($\mathcal{P}_{dim_{G_p}}, \ldots, \mathcal{P}_1$). As an example, the hierarchies defined by the permutations *id* and $\pi(j) := dim_{G_p} + 1 - j$, $1 \le j \le dim_{G_p}$, respectively, are opposite hierarchies, see Figure 2.

3 VERTEX LABELS OF PROCESSOR GRAPH

In this section we provide a way to recognize if a graph G_p is a partial cube, and if so, we describe how a labeling on V_p can be obtained in $O(|E_p|^2)$ time. To this end, we characterize partial cubes in terms of (*cut-sets* of) convex cuts.

Definition 3.1 (Convex cut). Let $G_p = (V_p, E_p)$ be a graph, and let (V_p^0, V_p^1) be a cut of G_p . The cut is called *convex* if no shortest path from a vertex in $V_p^0 [V_p^1]$ to another vertex in $V_p^0 [V_p^1]$ contains a vertex of $V_p^1 [V_p^0]$.

The *cut-set* of a cut (V_p^0, V_p^1) of G_p consists of all edges in G_p with one end vertex in V_p^0 and the other one in V_p^1 . Given the above



(a) Processor graph G_p (b) Distances in G_p (c) Application graph G_a

Figure 3: G_p is a partial cube with two convex cuts: the dotted vertical cut and the dashed horizontal cut (3a). First [second] digit of vertex labels $l_p(\cdot)$ indicates position w.r.t. vertical [horizontal] cut. Distance between u_p and v_p in G_p equals Hamming distance between $l_p(u_p)$ and $l_p(v_p)$ (3b). In 3c, a mapping $\mu(\cdot)$ from V_a to V_p ' is indicated by the colors. Communication across solid [dashed] edges requires 1 hop [2 hops] in G_p .

definitions, G_p is a partial cube if and only if (i) G_p is bipartite and (ii) the cut-sets of G_p 's convex cuts partition E_p [21]. In this case, the equivalence relation behind the partition is the Djoković relation θ [21]. Let $e_p = \{x_p, y_p\} \in E_p$. An edge f_p is Djoković related to e_p if one of f_p 's end vertices is closer to x_p than to y_p , while the other end vertex of f_p is closer to y_p than to x_p . Formally,

$$e_p \ \theta \ f_p : \Leftrightarrow |f_p \cap W_{x_p, y_p}| = |f_p \cap W_{y_p, x_p}| = 1 \text{, where}$$
$$W_{x_p, y_p} = \{w_p \in V_p \mid d_{G_p}(w_p, x_p) < d_{G_p}(w_p, y_p)\}.$$

Consequently, no pair of edges on any shortest path of G_p is Djoković related. In the following, we use the above definitions to find out whether G_p is a partial cube and, if so, to compute a labeling $l_p : V_p \mapsto \{0, 1\}^{\dim_{G_p}}$ for V_p according to Definition 2.2:

- (1) Test whether G_p is bipartite (in asymptotic time $O(|E_p|)$). If G_p is not bipartite, it is not a partial cube.
- (2) Pick an arbitrary edge e_p^1 and compute the edge set $E_p(e_p^1, \theta) := \{f_p \in E_p \mid f_p \ \theta \ e_p^1\}.$
- (3) Keep picking edges e²_p, e³_p,... that are not contained in an edge set computed so far and compute the edge sets E_p(e²_p, θ), E_p(e³_p, θ), If there is an overlap with a previous edge set, G_p is not a partial cube.
- (4) While calculating $E_p(e_p^j, \theta)$ where $1 \le j \le \dim_{G_p}$, set

$$l_p[j](u_p) := \begin{cases} 0, & \text{if } u_p \in W_{x_p^j}, y_p^j. \\ 1, & \text{otherwise.} \end{cases}$$
(5)

For an example of such vertex labels see Figure 3a.

Assuming that all distances between node pairs are computed beforehand, calculating $E_p(e_p^j, \theta)$ for $1 \le j \le \dim_{G_p}$ and setting the labeling $l_p(\cdot)$ (in steps 2,3 and 4) take $O(|E_p|)$ time. Detecting overlaps with already calculated edge sets takes $O(|E_p|^2)$ time (in step 3), which summarizes the time complexity of the proposed method.

Note that the problem has to be solved only once for a parallel computer. Since $|E_p| = O(|V_p|)$ for 2D/3D grids and tori – the processor graphs of highest interest in this paper – and $|E_p| = O(|V_p| \log |V_p|)$ for all partial cubes, our simple method is (almost) as fast, asymptotically, as the fastest and rather involved methods that solve the problem. Indeed, the fastest method to solve the problem takes time $O(|V_p||E_p|)$ [13]. Assuming that integers of at least $\log_2(|V_p|)$ bits can be stored in a single machine word and that addition, bitwise Boolean operations, comparisons and table look-ups can be performed on these words in constant time, the asymptotic time is reduced to $O(|V_p|^2)$ [9].

4 VERTEX LABELS OF APPLICATION GRAPH

Given an application graph $G_a = (V_a, E_a, \omega_a(\cdot))$, a processor graph $G_p = (V_p, E_p)$ that is a partial cube and a mapping $\mu : V_a \mapsto V_p$, the aim of this section is to define a labeling $l_a(\cdot)$ of V_a . This labeling is then used later to improve $\mu(\cdot)$ w.r.t. Eq. (3) by swapping labels between vertices of G_a . In particular, for any $u_a, v_a \in V_a$, the effect of their label swap on $\mu(\cdot)$ should be a function of their labels and those of their neighbors in G_a . It turns out that being able to access the vertices of G_a by their (unique) labels is crucial for the efficiency of our method. The following requirements on $l_a(\cdot)$ meet our needs.

- (1) $l_a(\cdot)$ encodes $\mu(\cdot)$.
- (2) For any two vertices u_a, v_a ∈ G_a, we can derive the distance between μ(u_a) and μ(v_a) from l_a(u_a) and l_a(v_a). Thus, for any edge e_a of G_a, we can find out how many hops it takes in G_p for its end vertices to exchange information, see Figure 3c.
- (3) The labels are unique on V_a .

To compute such $l_a(\cdot)$, we first transport labeling $l_p(\cdot)$ from V_p to V_a through $l_p(v_a) := l_p(\mu(v_a))$ for all $v_a \in V_a$. This new labeling $l_p : V_a \mapsto \{0, 1\}^{dim_{G_p}}$ already fulfills items 1) and 2). Indeed, item 1) holds, since labels are unique on V_p ; item 2) holds, because G_p is a partial cube. To fulfill item 3), we extend the labeling $l_p : V_a \mapsto \{0, 1\}^{dim_{G_p}}$ to a labeling $l_a : V_a \mapsto \{0, 1\}^{dim_{G_a}}$, where yet undefined dim_{G_a} should exceed dim_{G_p} only by the smallest amount necessary to ensure that $l_a(u_a) \neq l_a(v_a)$ whenever $u_a \neq v_a$. The gap $dim_{G_a} - dim_{G_p}$ depends on the size of the largest part in the partition induced by $\mu(\cdot)$.

Definition 4.1 (\dim_{G_a}). Let $\mu : V_a \mapsto V_p$ be a mapping. We set:

$$dim_{G_a} = dim_{G_a}(\mu) = dim_{G_p} + \max_{v_p \in V_p} \lceil \log_2 |\mu^{-1}(v_p)| \rceil.$$
 (6)

For any $v_a \in V_a$, $l_a(v_a)$ is a bitvector of length \dim_{G_a} ; its first \dim_{G_p} entries coincide with $l_p(v_a)$, see above, and its last $\dim_{G_a} - \dim_{G_p}$ entries serve to make the labeling unique. We denote the bitvector formed by the last $\dim_{G_a} - \dim_{G_p}$ entries by $l_e(v_a)$. Here, the subscript *e* in $l_e(\cdot)$ stands for "extension". To summarize,

$$l_a(v_a) = l_p(v_a) \circ l_e(v_a) \text{ for all } v_a \in V_a, \text{ where}$$
(7)

 \circ stands for concatenation. Except for temporary permutations of the labels' entries, the set $\mathcal{L} := l(V_a)$ of labels will remain the same. A label swap between u_a and v_a alters $\mu(\cdot)$ if and only if $l_p(u_a) \neq l_p(v_a)$. The balance of the partition of V_a , as induced by $\mu(\cdot)$, is preserved by swapping the labels of V_a .

Computing $l_e(\cdot)$ is straightforward. First, the vertices in each $\mu^{-1}(v_p)$, $v_p \in V_p$, are numbered from 0 to $|\mu^{-1}(v_p)| - 1$. Second,

these decimal numbers are then interpreted as bitvectors/binary numbers. Finally, the entries of the corresponding bitvectors are shuffled, so as to provide a good random starting point for the improvement of μ , see Lemma 5.1 in Section 5.

5 EXTENSION OF THE OBJECTIVE FUNCTION

Given the labeling of vertices in V_a , *i.* e, $l_a(\cdot) = l_p(\cdot) \circ l_e(\cdot)$, it is easy to see that solely $l_p(\cdot)$ determines the value of $Coco(\cdot)$. (This fact results from $l_p(\cdot)$ encoding the distances between vertices in G_p .) On the other hand, due to the uniqueness of the labels $l_a(\cdot)$, $l_e(\cdot)$ restricts $l_p(\cdot)$: $l_e(u_a) = l_e(v_a)$ implies $l_p(u_a) \neq l_p(v_a)$, *i.* e, that u_a and v_a are mapped to different PEs.

The plan of the following is to ease this restriction by avoiding as many cases of $l_e(u_a) = l_e(v_a)$ as possible. To this end, we incorporate $l_e(\cdot)$ into the objective function, thus replacing $\text{Coco}(\cdot)$ by a modified one. Observe that $l_p(\cdot)$ and $l_e(\cdot)$ give rise to two disjoint subsets of E_a , *i. e.* subsets of edges, the two end vertices of which agree on $l_p(\cdot)$ and $l_e(\cdot)$, respectively:

$$E_a^p = E_a^p(l_a) := \{e_a = \{u_a, v_a\} \in E_a \mid l_p(u_a) = l_p(v_a)\},\$$
$$E_a^e = E_a^e(l_a) := \{e_a = \{u_a, v_a\} \in E_a \mid l_e(u_a) = l_e(v_a)\}.$$

In general these two sets do not form a partition of E_a , since there can be edges whose end vertices disagree both on $l_p(\cdot)$ and on $l_e(\cdot)$. With $h(\cdot, \cdot)$ denoting the Hamming distance, optimizing Coco(\cdot) in Eq. (3) can be rewritten as follows. Find

$$l_a^* := \underset{\substack{l_a: V_a \mapsto \mathcal{L} \\ l_a \text{ bijective}}}{\operatorname{argmin}} \operatorname{Coco}(l_a), \text{ where } (8)$$

$$\operatorname{Coco}(l_a) := \sum_{\substack{e_a \in E_a \setminus E_a^p(l_a)\\e_a = \{u_a, v_a\}}} \omega_a(e_a) \ h(l_p(u_a), l_p(v_a)). \tag{9}$$

For all $e_a = \{u_a, v_a\} \in E_a^e$ it follows that $l_p(u_a) \neq l_p(v_a)$, implying that u_a and v_a are mapped to different PEs. Thus, any edge $e_a \in E_a^e(l_a)$ increases the value of $\text{Coco}(\cdot)$ with a damage of

$$\omega_a(u_a, v_a) h(l_p(u_a), l_p(v_a)) > 0.$$
(10)

This suggests that reducing E_a^e may be good for minimizing $\text{Coco}(\cdot)$. The crucial question here is whether reducing E_a^e can obstruct our primary goal, *i. e.*, growing E_a^p (see Eq. (9)). Lemma 5.1 below shows that this is not the case, at least for perfectly balanced $\mu(\cdot)$. A less technical version of Lemma 5.1 is the following: If $\mu(\cdot)$ is perfectly balanced, then two mappings, where one has bigger E_a^p and one has smaller E_a^e (both w. r. t. set inclusion), can be combined to a third mapping that has the bigger E_a^p and the smaller E_a^e . The third mapping from which it inherited big E_a^p , as, due to smaller E_a^e , the third mapping is less constrained by the uniqueness requirement:

LEMMA 5.1 (REDUCING E_a^e COMPATIBLE WITH GROWING E_p^e). Let $\mu : V_a \mapsto V_p$ be such that $|\mu^{-1}(u_p)| = |\mu^{-1}(v_p)|$ for all $u_p, v_p \in V_p$ (perfect balance). Furthermore, let $l_a(\cdot)$ and $l'_a(\cdot)$ be bijective labelings $V_a \mapsto \mathcal{L}$ that correspond to $\mu(\cdot)$ as specified in Section 4. Then, $E_a^p(l_a) \supseteq E_a^p(l'_a)$ and $E_a^e(l'_a) \subseteq E_a^e(l_a)$ implies that there exists l_a^* that also corresponds to $\mu(\cdot)$ with (i) $E_a^p(l_a^*) = E_a^p(l_a)$ and (ii) $E_a^e(l_a^*) = E_a^e(l_a')$.

PROOF. Set $l_a^*(\cdot) := l_a^p(\cdot) \circ l_a^e(\cdot)$. Then, $l_a^*(\cdot)$ fulfills (i) and (ii) in the claim, and the first dim_{G_p} entries of $\mu(\cdot)$ specify $\mu(\cdot)$. If remains to show that the labeling $l_a^*(\cdot)$ is unique on V_a . This is a consequence of (a) $l_a(\cdot)$ being unique and (b) $E_a^e(l_a^*) = E_a^e(l_a') \subseteq E_a^e(l_a)$.

In practice we usually do not have perfect balance. Yet, the balance is typically low, *e. g.* $\epsilon = 0.03$. Thus, we still expect that having small $E_a^e(l_a)$ is beneficial for minimizing Coco(·).

Minimization of the damage to $Coco(\cdot)$ from edges in $E_a^e(l_a)$, see Eq. (10), amounts to maximizing the *diversity* of the label extensions in G_a . Formally, in order to diversify, we want to find

$$l_a^* := \underset{\substack{l_a: V_a \mapsto \mathcal{L} \\ l_a: W_a \mapsto \mathcal{L}}{\text{ index}}}{\text{ for all } l_a : V_a \mapsto \mathcal{L}}$$
(11)

$$\operatorname{Div}(l_a) := \sum_{\substack{e_a \in E_a \setminus E_a^e(l_a)\\e_a = \{u_a, v_a\}}} \omega_a(e_a) h(l_e(u_a), l_e(v_a)).$$
(12)

We combine our two objectives, *i. e.*, minimization of $\text{Coco}(\cdot)$ and maximization of $\text{Div}(\cdot)$, with the objective function $\text{Coco}^+(\cdot)$:

$$l_a^* := \underset{\substack{l_a: V_a \mapsto \mathcal{L} \\ l_a \text{ blicetive}}}{\operatorname{argmin}} \operatorname{Coco}^+(l_a), \text{ where } (13)$$

$$\operatorname{Coco}^{+}(l_{a}) := \operatorname{Coco}(l_{a}) - \operatorname{Div}(l_{a}).$$
(14)

6 MULTI-HIERARCHICAL LABEL SWAPPING

After formulating the mapping problem as finding an optimal labeling for the vertices in V_a , we can now turn our attention to *how* to find such a labeling – or at least a very good one. Our algorithm is meant to *improve* mappings and resembles a key ingredient of the classical graph partitioning algorithm by Kernighan and Lin (KL) [16]: vertices of G_a swap their membership to certain subsets of vertices. Our strategy differs from KL in that we rely on a rather simple local search which is, however, performed on multiple (and very diverse) random hierarchies on G_a . These hierarchies are oblivious to G_a 's edges and correspond to recursive bipartitions of G_a , which, in turn, are extensions of natural recursive bipartitions of G_p .

6.1 Algorithm TIMER

Our algorithm, see procedure TIMER in Algorithm 1, takes as input (i) an application graph G_a , (ii) a processor graph G_p with the partial cube property, (iii) an initial mapping $\mu : V_a \mapsto V_p$ and (iv) the number of hierarchies, N_H . N_H controls the tradeoff between running time and the quality of the results. The output of TIMER consists of a bijective labeling $l_a : V_a \mapsto \mathcal{L}$ such that $\text{Coco}^+(l_a)$ is low (but not necessarily optimal). Recall from Section 1 that requiring $\mu(\cdot)$ as input is no major limitation. An initial bijection $l_a(\cdot)$ representing this $\mu(\cdot)$ is found in lines 1, 2 of Algorithm 1.

In lines 3 through 21 we take N_H attempts to improve $l_a(\cdot)$, where each attempt uses another hierarchy on $\{0, 1\}^{\dim_{G_a}}$. Before the new hierarchy is built, the old labeling is saved in case the label swapping in the new hierarchy turns out to be a setback w.r.t. $\text{Coco}^+(\cdot)$ (line

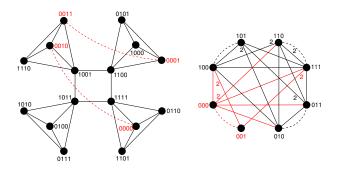


Figure 4: Graphs G_a^1 on level 1 of the hierarchy and G_a^2 on level 2 $(G_a^2 \text{ arises from } G_a^1 \text{ through contractions controlled by the labels) are shown on the left and right, respectively. The first [last] two digits of the labels on <math>G_a^1$'s vertices indicate $l_p(\cdot) [l_e(\cdot)]$, respectively. Swapping labels 000 and 001 on G_a^2 yields a gain of 1 in diversity (see Eq. (12)). The corresponding swaps in G_a^1 are indicated by the dashed red lines on the left.

4). This may occur, since the gain w.r.t. $\operatorname{Coco}^+(\cdot)$ on a coarser level of a hierarchy is only an estimate of the gain on the finest level (see below). The hierarchy and the current mapping are encoded by (i) a sequence of graphs $G_a^i = (V_a^i, E_a^i, \omega_a^i), 1 \le i \le \dim_{G_a}$, with $G_a^1 = G_a$, (ii) a sequence of labelings $l_a^i : V_i \mapsto \{0, 1\}^{\dim_{G_a^i}}$ and (iii) a vector, called parent, that provides the hierarchical relation between the vertices. From now on, we interpret vertex labels as integers whenever convenient. More precisely, an integer arises from a label, *i. e.*, a bitvector, by interpreting the latter as a binary number.

In lines 6 and 7, the entries of the vertex labels of G_a are permuted according to a random permutation $\pi(\cdot)$. The construction of the hierarchy (lines 9 through 14) goes hand in hand with label swapping (lines 10-12) and label coarsening (in line 13). The function contract(\cdot, \cdot, \cdot) contracts any pair of vertices of G_a^{i-1} whose labels agree on all but the last digit, thus generating G_a^i . The same function also cuts off the last digit of $l_a^{i-1}(v)$ for all $v \in V_a^{i-1}$, and creates the labeling $l_a^i(\cdot)$ for the next coarser level. Finally, contract(\cdot, \cdot, \cdot) builds the vector parent (for encoding the hierarchy of the vertices). In line 15, the call to assemble() derives a new labeling $l_a(\cdot)$ from the labeling $l_a^i(\cdot)$ on the levels $1 \le i \le dim_{G_a} - 1$ of a hierarchy (read more in Section 6.2). The permutation of l_a 's entries is undone in line 16, and $l_a(\cdot)$ is kept only if better than $l_{old}(\cdot)$, see lines 17 to 19. Figure 4 depicts a snapshot of TIMER on a small instance.

6.2 Function assemble()

Function assemble() (Algorithm 2) in line 15 of TIMER turns the hierarchy of graphs G_a^i into a new labeling $l_a(\cdot)$ for G_a , digit by digit, using labels $l_a^i(\cdot)$ (in Algorithm 2, " $\ll i$ " denotes a left shift by *i* digits). The least and the most significant digit of any $l_a^1(v_1)$ are inherited from $l_a(\cdot)$ (line 7 of Algorithm 1) and do not change (lines 2, 17 and 18). The remaining digits are set in the loop from line 5 to 16. Whenever possible, digit *i* of $l_a^1(v_1)$ is set to the last digit of the parent of v_1 (= preferred digit) on level *i*, see lines 9, 11. This might, however, lead to a label that is not in $l_a^1(V_a^1)$ any more, which would change the set of labels and may violate the balance constraint coming from $\mu(\cdot)$. To avoid such balance problems, we take the last

Algorithm 1 Procedure TIMER ($G_a, G_p, \mu(\cdot), N_H$) returns a bijection $l_a : V_a \mapsto \{0, 1\}^{dim_{G_a}}$ with a low value of $\text{Coco}(l_a)$.

1: Find a labeling $l_p(\cdot)$ of V_p 's vertices, as described in Section 2 2: Using $\mu(\cdot)$, extend $l_p(\cdot)$ to a labeling $l_a(\cdot)$ of V_a 's vertices, as described in Section 4 3: for $N' = 1 ..., N_H$ do $l_{old}(\cdot) \leftarrow l_a(\cdot)$ 4: ▶ just in case $l_a(\cdot)$ gets worse w.r.t. $Coco^+(\cdot)$ 5: parent \leftarrow [] ▶ parent will encode the hierarchy of the vertices Pick a random permutation $\pi : \{1, \ldots, dim_{G_a}\} \mapsto \{1, \ldots, dim_{G_a}\}$ 6: 7: $l_a(\cdot) \leftarrow \pi(l_a(\cdot))$ $G_a^1 \leftarrow G_a, \, l_a^1(\cdot) \leftarrow l_a(\cdot)$ 8: for $i = 2, ..., dim_{G_a} - 1$ do for all $u, v \in G_a^{i-1}$ with $l_a^{i-1}(u)/2 = l_a^{i-1}(v)/2$ do Swap labels $l_a^{i-1}(u)$ and $l_a^{i-1}(v)$ if this decreases $\operatorname{Coco}^+(l_a^{i-1})$ on G_a^{i-1} . 9: 10: 11: 12: end for $(G_a^i, l_a^i, \text{parent}) \gets \text{contract}(G_a^{i-1}, l_a^{i-1}, \text{parent})$ 13: end for 14: $l_a(\cdot) \leftarrow \text{assemble}(G_a^1, \dots, G_a^{dim_G-1}, l_a^1, \dots, l_a^{dim_{Ga}-1}, \text{parent})$ 15: $l_a(\cdot) \leftarrow \pi^{-1}(l_a(\cdot))$ 16: if $\operatorname{Coco}^+(l_a) > \operatorname{Coco}^+(l_{old})$ then 17: $l_a(\cdot) \leftarrow l_{old}(\cdot)$ 18: 19: end if 20: end for 21: return $l_a(\cdot)$

Algorithm 2 Function assemble($G_a^1, \ldots, G_a^{dim_G-1}, l_a^1, \ldots, l_a^{dim_{G_a}-1}$, parent) returns a new labeling $l_a^1(\cdot)$ of the vertices of $G_a^1 = G_a$ and thus a new labeling $l_a(\cdot)$ of G_a 's vertices.

1: for all $v_1 \in V_a^1$ do						
2: $l_a^1(v_1) \leftarrow \overline{l_a^1}(v_1) \mod 2$	 Write least significant digit 					
3: oldParent $\leftarrow v_1$						
4: $i \leftarrow 1$						
5: while $i < dim_{G_a^1}$ do	▶ Write digits 2, , $\dim_{G_1} - 1$					
6: newParent						
7: $i \leftarrow i + 1$						
8: newParentLabel $\leftarrow l_a^i$ (newParent)						
9: prefLabel $\leftarrow l_a^1(v_1) + (\text{newParentLabel} \ll (i-1))$	Preferred i least sig. digits					
10: if $\exists w \in V_1$ with $l_a^1(w) \mod 2^i = \text{prefLabel then}$	Part of existing label?					
11: $l_a^1(v_1) \leftarrow l_a^1(v_1) + ((\text{newParentLabel mod } 2) \ll (i-1))$	 Write preferred digit 					
12: else						
13: $l_a^1(v_1) \leftarrow l_a^1(v_1) + ((1 - (\text{newParentLabel mod } 2)) \ll (i-1))$	 Write other digit 					
14: end if						
15: $oldParent \leftarrow newParent$						
16: end while						
17: if $l_a^1(v_1) \ge 1 \ll (dim_{G_1} - 1)$ then						
18: $l_a^1(v_1) \leftarrow l_a^1(v_1) + (1 \ll (dim_{G_1} - 1))$	 Write most significant digit 					
19: end if						
20: end for						
21: return $l_a^1(\cdot)$						

digit of $l_a^i(v_a)$ if possible (in lines 9-11) or, if not, we switch to the (old) inverted digit, see line 13. Since $G_a^1 = G_a$, new $l_a^1(\cdot)$ on G_a^1 can be taken as new $l_a(\cdot)$ on G_a , see line 18 in Algorithm 1.

6.3 Running time analysis

The expected asymptotic running time of function assemble() is $O(|V_a| \cdot dim_{V_a})$. Here, "expected" is due to the condition in line 10 that is checked in *expected* constant time. (We use a hashing-based

C++ std::unordered_map to find a vertex with a certain label. A plain array would be too large for large grids and tori, especially if the blocks are large, too.) For Algorithm 1, the expected running time is dominated by the loop between lines 9 and 14. The loop between lines 10 and 12 takes amortized expected time $O(|E_a|)$ ("expected", because we have to go from the labels to the vertices and "amortized", because we have to check the neighborhoods of all u, v). The contraction in line 13 takes time $O(|E_a|)$, too. Thus, the

loop between lines 9 and 14 takes time $O(|E_a|dim_{G_a})$. In total, the expected running time of Algorithm 1 is $O(N_H |E_a| dim_{G_a})$.

An effective first step toward a parallel version of our algorithm would be simple loop parallelization in lines 10-12 of Algorithm 1. To avoid stale data, label accesses need to be coordinated.

7 EXPERIMENTS

7.1 Description of experiments

In this section we specify our test instances, our experimental setup and the way we evaluate the computed mappings.

The application graphs are the 15 complex networks used by Safro *et al.* [26] for partitioning experiments and in [11] for mapping experiments, see Table 1. Regarding the processor graphs, we follow loosely current architectural trends. Several leading supercomputers have a torus architecture [8], and grids (= meshes) experience rising importance in emerging multicore chips [7]. As processor graphs $G_p = (V_p, E_p)$ we therefore use a 2DGrid(16×16), a 3DGrid(8×8×8), a 2DTorus(16×16), a 3DTorus(8×8×8) and, for more theoretical reasons, an 8-dimensional hypercube. In our experiments, we set the number of hierarchies (N_H) for T1MER to 50 and whenever is needed for partitioning/mapping with state-of-the-art tools, the load imbalance is set to 3%. All computations are based on sequential C++ code. Each experiment is executed on a node with two Intel XeonE5-2680 processors (Sandy Bridge) at 2.7 GHz equipped with 32 RAM and 8 cores per processor.

Baselines. For the evaluation, we use four different experimental cases (c1 to c4), each of which assumes a different initial mapping $\mu_1(\cdot)$ as an input to TIMER (Algorithm 1). The different cases shall measure the improvement by TIMER compared to different standalone mapping algorithms. In the following, we describe how we obtain the initial mappings $\mu_1(\cdot)$ for each case separately.

In c1 we compare the improvement of TIMER on an initial mapping produced by SCOTCH. For that, we use the generic mapping routine of SCOTCH with default parameters. It returns a mapping $\mu_1(\cdot)$ of a given graph using a dual recursive bipartitioning algorithm.

In c2 we use the IDENTITY mapping that maps block *i* of the application graph (or vertex *i* of the communication graph G_c) to node *i* of the processor graph G_p , $1 \le i \le |G_c| = |G_p|$. IDENTITY receives its solution from the initial partition computed with KAHIP. This approach benefits from spatial locality in the partitions, so that IDENTITY often yields surprisingly good solutions [11].

In c3 we use a mapping algorithm named GREEDYALLC that has been previously proposed by a subset of the authors (implemented on top of KAHIP). GREEDYALLC is an improvement of a previous greedy algorithm [3] and is the best performing algorithm in [11]. It builds on the idea of increasing a mapping by successively adding assignments $v_c \rightarrow v_p$ such that (a) $v_c \in G_c$ has maximal communication volume with one or all of the already mapped vertices of G_c and (b) $v_p \in G_p$ has minimal distance to one or all of the already mapped vertices of G_p .

Finally, we compare against LIBTOPOMAP [12], a state-of-the-art mapping tool that includes multiple mapping algorithm. More precisely we use the algorithm whose general idea follows the construct method, in [3]. Subset of the authors has previous implemented the above algorithm on top of the KAHIP tool (named GREEDYMIN). As a result, and in order to accommodate comparisons with c2, c3 GREEDYMIN is used as the mapping algorithm for the experimental case c4.

Labeling. Once the initial mappings $\mu_1(\cdot)$ are calculated, we need to perform two more steps in order to get an initial labeling $l_a(\cdot)$:

- We compute a labeling l_p : V_p → {0, 1}^{dim_{Gp}}, where l_p(·) and dim_{Gp} fulfill the conditions in Definition 2.2. In particular, d_{Gp}(u_p, v_p) = d_h(l_p(u_p), l_p(v_p)) for all u_p, v_p ∈ V_p, where d_h(·, ·) denotes the Hamming distance. Due to the sparsity of our processor graphs G_p (grids, tori, hypercubes), we use the method outlined in Section 3.
- (2) We extend the labels of G_p 's vertices to labels of G_a 's vertices as described in Section 4.

Then, for each experimental case, TIMER is given the initial mapping $\mu_1(\cdot)$ and it generates a new mapping $\mu_2(\cdot)$. Here, we compare the quality of mapping $\mu_2(\cdot)$ to $\mu_1(\cdot)$ in terms of our main objective function $\text{Coco}(\cdot)$, but we also provide results for the edgecut metric and for the running times.

Metrics and parameters. Since SCOTCH, KAHIP and TIMER have randomized components, we run each experiment 5 times. Over such a set of 5 repeated experiments we compute the minimum, the arithmetic mean and the maximum of TIMER's running time (T), edge cut (Cut) and communication costs $Coco(\cdot)$ (Co). Thus we arrive at the values $T_{min}, T_{mean}, \ldots, Co_{max}$ (9 values for each combination of G_a , G_p , for each experimental case c1 to c4). Each of these values is then divided by the min, mean, and max value before the improvements by TIMER, except the running time of TIMER, which is divided by the partitioning time of KAHIP for c2,c3,c4 and by the mapping time of SCOTCH for c1. Thus, we arrive at 9 quotients $qT_{min}, \ldots, qCo_{max}$. Except for the terms involving running times, a quotient smaller than one means that TIMER was successful. Next we form the geometric means of the 9 quotients over the application graphs of Table 1. Thus we arrive at 9 values $qT_{min}^{gm}, \ldots, qCo_{min}^{gm}$ for any combination of G_p and any experimental case. Additionally, we calculate the geometric standard deviation as an indicator of the variance over the normalized results of the application graphs.

7.2 Experimental Results

The detailed experimental results regarding quality metrics are displayed in Figures 5a through 5d (one for each experimental case), while the running time results are given in Table 2. Here is our summary and interpretation:

• When looking at the running times for the experimental cases c2 to c4(in Table 2), we see that the running time results of TIMER are on the same order of magnitude as partitioning with KAHIP; more precisely, TIMER is on average 42% faster. Thus, inserting TIMER into the partitioning/mapping pipeline of KAHIP would not increase the overall running time significantly.

The comparison in case c1 needs to be different. Here the initial mapping is produced by SCOTCH's mapping routine (using partitioning internally), so that the relative timing results of TIMER are divided by SCOTCH's mapping time. SCOTCH is much faster (on average 19x), but its solution quality is also not good (see *Co* metric in Figure 5a). In informal experiments, we observed that only ten hierarchies (parameter N_h) are sufficient for TIMER to improve the communication costs significantly compared to SCOTCH– with a much lower running time penalty than the one reported here. Finally, recall that parallelization could reduce the running time of TIMER.

- · Processor graphs do have an influence on running times. The processor graphs, from top to bottom in Table 2, have 30, 21, 32, 24 and 8 convex cuts, respectively. Thus, if we keep grids and tori apart, we can say that the time quotients increase with the number of convex cuts. Recall that the number of convex cuts equals the length of the labels of V_p . Moreover, the length of the extension of V_p 's labels to those of V_a depends also on the processor graph, because a higher number of PEs (number of blocks) yields fewer elements per block. However, this influence on the length of the labels is small (increase of 1 in case of $|V_p| = 256$ compared to $|V_p| = 512$). Thus it is basically the length of V_a 's labels that determines the time quotients. For the experimental cases c2 to c4, this observation is in line with the fact that KAHIP takes longer for higher values of $|V_p|$ (see Table 3 in Appendix A.1).
- TIMER successfully reduces communication costs in a range from 6% to 34% over the different experimental cases

(see *minCo*, *Co* and *maxCo* values in Figure 7.2). It does so at the expense of the edge cut metric with an average increase between 2% to 11% depending on the experimental case. Note that for case c1 the edge cut increase is minimum (Figure 5a). Moreover, for cases c2 to c4 this increase is not surprising due to the different objectives of the graph partitioner (KAHIP) and TIMER. On grids and tori, the reduction of communication cost, as measured by $Coco(\cdot)$, is respectively 18% and 13% (on average, over all experimental cases).

The better the connectivity of G_p , the harder it gets to improve $\text{Coco}(\cdot)$ (results are poorest on the hypercube). (Note that q_{min} values can be larger than q_{mean} and q_{max} values due to the evaluation process described in Section 7.1.)

We observed before [11] that GREEDYALLC performs better on tori than on grids; this is probably due to GREEDYALLC "invading" the communication graph *and* the processor graph. The resulting problem is that it may paint itself into a corner of the processor graph (if it has corners, like a grid). Thus, it is not surprising that for c2 the improvement w. r. t. $Coco(\cdot)$ obtained by TIMER is greater for grids than for tori. Likewise, we observe that TIMER is able to decrease the communication costs significantly for c1 (even more than in the other cases). Apparently, the generic

Name	#vertices	#edges	Туре
p2p-Gnutella	6 4 0 5	29 215	file-sharing network
PGPgiantcompo	10680	24 316	largest connected component in network of PGP users
email-EuAll	16 805	60 260	network of connections via email
as-22july06	22 963	48 436	network of internet routers
soc-Slashdot0902	28 550	379 445	news network
loc-brightkite_edges	56739	212 945	location-based friendship network
loc-gowalla_edges	196 591	950 327	location-based friendship network
citationCiteseer	268 495	1 156 647	citation network
coAuthorsCiteseer	227 320	814 134	citation network
wiki-Talk	232 314	1 458 806	network of user interactions through edits
coAuthorsDBLP	299 067	977 676	citation network
web-Google	356 648	2 093 324	hyperlink network of web pages
coPapersCiteseer	434 102	16 036 720	citation network
coPapersDBLP	540 486	15 245 729	citation network
as-skitter	554930	5 797 663	network of internet service providers

Table 1: Complex networks used for benchmarking.

Table 2: Running time results of each experimental case. For c1 results are relative to SCOTCH's mapping time, while for c2, c3, c4, results are relative to partitioning time with KAHIP (original values in Appendix A.1, Table 3)

	Scotch (c1)		IDENTITY (c2)			GREEDYALLC (c3)			GREEDYMIN (c4)			
	qT_{min}^{gm}	qT ^{gm} _{mean}	qT_{max}^{gm}									
16×16 grid	30.2780	29.8388	31.8387	0.95310	1.00480	1.05286	0.97916	1.01791	1.05075	0.95448	1.00681	1.05500
$8 \times 8 \times 8$ grid	18.0226	18.0484	19.5701	0.47495	0.49364	0.51333	0.47525	0.49427	0.51606	0.48712	0.50654	0.52698
16×16 torus	21.1373	21.2507	22.5322	0.61627	0.64089	0.66334	0.61743	0.63765	0.66042	0.64834	0.66524	0.68270
$8 \times 8 \times 8$ torus	13.8136	14.0924	14.3866	0.33254	0.34167	0.35008	0.32952	0.33885	0.34855	0.33412	0.34493	0.35744
8-dim HQ	11.2948	11.4237	11.5842	0.36821	0.37977	0.38916	0.36631	0.37246	0.38005	0.37254	0.38093	0.39196

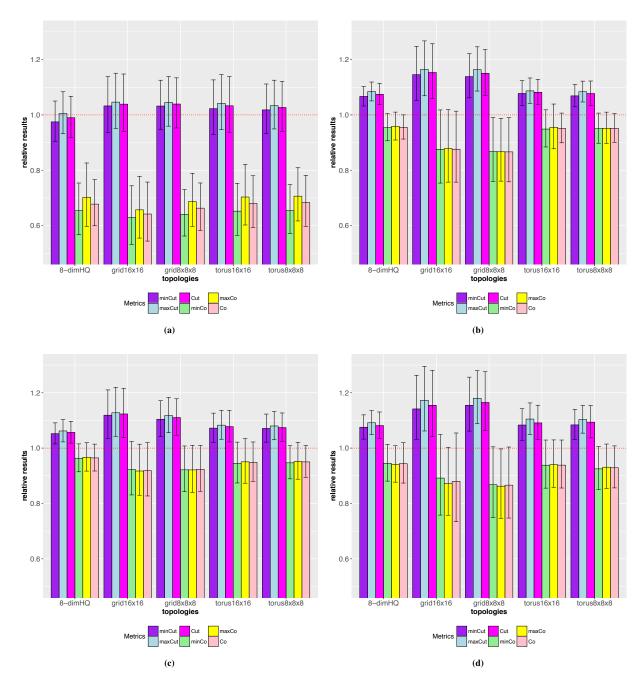


Figure 5: Quality results (*Co* and *Cut*) for experimental case (a) c1 (initial mapping with SCOTCH), (b) c2 (initial mapping with IDENTITY), (c) c3 ((initial mapping with GREEDYALLC)), and (d) c4 (initial mapping with GREEDYMIN).

nature of SCOTCH's mapping approach leaves room for such an improvement.

8 CONCLUSIONS

We have presented a new method, TIMER, to enhance mappings of computational tasks to PEs. TIMER can be applied whenever the

processor graph G_p is a partial cube. Exploiting this property, we supply the vertices of the application graph with labels that encode the current mapping and facilitate a straightforward assessment of any gains/losses of local search moves. By doing so, we are able to improve initial mappings using a multi-hierarchical search method.

Permuting the entries of the vertex labels in the application graph gives rise to a plethora of very diverse hierarchies. These hierarchies do not reflect the connectivity of the application graph G_a , but correspond to recursive bipartitions of G_a , which, in turn, are extensions of "natural" recursive bipartitions of G_p . This property of TIMER suggests to use TIMER as a complementary tool to enhance state-of-the-art methods for partitioning and mapping.

In our experiments we were able to improve state-of-the-art mappings of complex networks to different architectures by about 6% to 34% in terms of Coco. More precisely, for grids we obtained, on average, an improvement of 18% and for tori an improvement of 13% over the communication costs of the initial mappings.

The novelty of TIMER consists in the way it harnesses the fact that many processor graphs are partial cubes: the local search method itself is standard and simple. We assume that further improvements over state-of the art mappings can be achieved by replacing the simple local search by a more sophisticated method.

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A APPENDIX

A.1 Additional experimental results

Table 3: Running times in seconds for KAHIP to partition the complex networks in Table 1 into $|V_p| = 256$ and $|V_p| = 512$ parts, respectively. These partitions are used to construct the starting solutions for the mapping algorithms for cases c2 to c4.

Name	$ V_p = 256$	$ V_p = 512$
PGPgiantcompo	1.457	2.297
as-22july06	11.179	13.559
as-skitter	1439.316	2557.827
citationCiteseer	217.951	367.716
coAuthorsCiteseer	58.120	69.162
coAuthorsDBLP	157.871	233.000
coPapersCiteseer	780.491	841.656
coPapersDBLP	1517.283	2377.680
email-EuAll	22.919	17.459
loc-brightkite_edges	113.720	155.384
loc-gowalla_edges	461.583	1174.742
p2p-Gnutella04	16.377	17.400
soc-Slashdot0902	887.896	1671.585
web-Google	128.843	130.986
wiki-Talk	1657.273	4044.640
Arithmetic mean	498.152	911.673
Geometric mean	142.714	204.697