



Extending Classical Processors to Support Future Large Scale Quantum Accelerators

Invited Talk Abstract

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Extensive research in material science together with outstanding engineering efforts allowed quantum technology to be significantly improved hence enabling continuing scaling of quantum circuit size. In around 10 years, quantum annealing circuits have reached 10^3 qubits and trailing by several years, universal quantum circuits now demonstrate similar trends. From the current trends we can expect that quantum computers will reach thousands of qubits in the next 5-10 years.

However, the term 'quantum computer' carries the confusing impression that it is an independent computational device, whereas it is nothing but a processing unit wrapped up into a classical control system. And quantum circuit scaling itself does not guarantee any practical use without appropriate progress on the part of classical control hardware and software. To operate such a large-scale universal quantum computer with thousands of qubits, extensive classical computational resources will be required.

The reason lies in the quantum nature of such an accelerator and its physical implementation complexity. Regardless of the chosen implementation technology, base qubit state is extremely delicate. It is very sensitive to any kind of noise caused by pure isolation, inappropriate control pulses, measurement, or other qubit interactions. Therefore, the probability of getting false values is unacceptably high.

Many of quantum challenges can be addressed through the classical software approaches. The software stack for quantum computers has to combine algorithm and circuit design tools and simulators, compilers for different levels of programming abstraction to provide fault-tolerant and optimal topological placement, algorithm-dependent calibration roadmap generators, etc.

On the other hand, the control hardware is responsible for efficient execution of the compiled code on the actual quantum hardware and has to support real time system tracking, dynamic error decoding and correction mechanisms. These classical algorithms

will need to keep pace with the high clock rate of the quantum hardware that can reach tens of GHz. For example, decoding quantum error-correction codes is known to be an NP-hard problem.

In turn, control hardware includes multiple layers each of which is responsible for a specific set of tasks, e.g. controllers, digital-analogue and analogue-digital converters, filters, waveform generators, etc. At this early stage of quantum architecture development, there is no clear understanding of where the upcoming challenges will be addressed through the entire stack of complex digital and analogue circuits. However, we expect that control processor will become a crucial part for successful implementation and adoption of future quantum computers.

In our talk, we discuss the challenges that classical processors will face while controlling future large-scale quantum systems. We discuss how these challenges will affect processor micro-architecture to guarantee on time quantum gate execution, continuing qubit state measurement, store and analysis, support massive parallelism and perform advanced bit manipulations on the top of the measured data.

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