# A reduced-precision streaming SpMV architecture for Personalized PageRank on FPGA

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## ABSTRACT

Sparse matrix-vector multiplication is often employed in many data-analytic workloads in which low latency and high throughput are more valuable than exact numerical convergence. FPGAs provide quick execution times while offering precise control over the accuracy of the results thanks to reduced-precision fixed-point arithmetic. In this work, we propose a novel streaming implementation of Coordinate Format (COO) sparse matrix-vector multiplication, and study its effectiveness when applied to the Personalized PageRank algorithm, a common building block of recommender systems in e-commerce websites and social networks. Our implementation achieves speedups up to 6x over a reference floating-point FPGA architecture and a state-of-the-art multi-threaded CPU implementation on 8 different data-sets, while preserving the numerical fidelity of the results and reaching up to 42x higher energy efficiency compared to the CPU implementation.

## **CCS CONCEPTS**

• Theory of computation  $\rightarrow$  *Graph algorithms analysis; Rounding techniques;* • Hardware  $\rightarrow$  Hardware accelerators.

## **KEYWORDS**

FPGA, Graph Algorithms, Approximate Computing

#### **1** INTRODUCTION

Sparse matrix-vector multiplication (SpMV) is a computational element widely employed in machine learning, engineering, and most importantly, graph analytics [11, 23] as real-world graphs present an extremely high degree of sparsity. Personalized PageRank (PPR) [2], a variation of the famous PageRank algorithm ranks the most relevant vertices of the graph with respect to an input vertex. In most cases PPR must be computed with minimal latency, often on graphs with millions of edges, such as domain-specific knowledge bases, e-commerce websites, and social networks communities [13, 15], to find recommended posts in a social network while users interact with it, or recommended items for a given query on an e-commerce platform. Moreover, the precise numerical values produced by the algorithm are rarely useful, as long as the order of the top-ranked vertices is correct (consider the problem of recommending the top-10 products for a user query). Numerical boundedness of PPR makes Field-Programmable Gate Arrays (FPGAs) suitable for computing PPR with throughput beyond traditional architectures, leveraging fixed-point arithmetic that can reduce execution time while preserving the correct ranking, and accelerate convergence.

In this work, we propose a novel FPGA architecture for a streaming edge-centric SpMV that uses Coordinate (COO) format matrices, and apply it to the computation of PPR. Reduced-precision fixedpoint arithmetic is used to maximize performance while reducing resource utilization and preserving the quality of the results. In summary, we present the following contributions:

- An optimized FPGA architecture of SpMV that leverages a COO matrix and reduced-precision arithmetic, which we employ in a novel implementation of PPR (Section 4).
- We validate the practical applicability of our PPR implementation on 8 different graphs against a state-of-the-art multi-threaded CPU implementation and an equivalent 32bits floating-point FPGA architecture, reaching speedups up to **6.8x** and up to **42x** higher energy efficiency.
- Most importantly, we characterize how reduced precision leads to negligible accuracy loss and **2x** faster convergence on PPR, showing the effectiveness of reduced precision for approximate graph ranking algorithms (Section 5).

## 2 RELATED WORK

In this section, we provide an overview of existing research on the optimization of SpMV for different hardware architectures, especially in the context of graph algorithms and PPR.

## 2.1 CPU and GPU Implementations

Leveraging sparse linear algebra for graph processing is the focus of the GraphBLAS project, which aims at defining operations on graphs through the language of linear algebra [11], and it offers early implementations for both CPU and GPU [4, 22]. Highly tuned implementations of PPR exploit the graph data-layout to maximize cache usage [25], or employ multi-machine setups to process trillions of edges [26]. Green-Marl [8] and GraphIt [24] implements PPR using Domain-Specific Languages (DSLs) that abstract the intricacies of graph processing, and optimized to fully exploits the CPU hardware. PPR on GPU is less common: it is worth mentioning nvGRAPH [1] and GraphBLAST [22], that leverage sparse linear algebra to match and possibly outperform CPU implementations.

### 2.2 FPGA Implementations

To the best of our knowledge, no existing work specifically addresses the computation of PPR on FPGA, either using reducedprecision arithmetic or algorithmic optimizations.

However, there have been significant contributions in optimizing SpMV computations on FPGAs, as SpMV represents the main bottleneck of many PageRank implementations. Recent work by Grigoras et al. [7] focuses on compressing the sparse matrix, moving the bottleneck from memory accesses to the decompression of the input data while lowering the storage demand. Umuroglu et al.

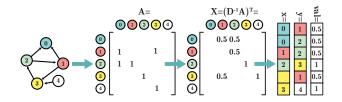


Figure 1: A graph as COO matrix. In X, each value *val* can be seen as the probability of moving from y to x. For example, from vertex x = 0 there is a 0.5 probability of coming from vertex y = 1 and a 0.5 probability of coming from vertex y = 2

[20] leverage local cache hierarchies and pre-processing schemes to maximize the amount of time in which values are kept in a fast local cache. Using data-set partitioning and complex memory hierarchies enable SpMV computations on web-scale graphs, as seen in Shan et al. [18]: clearly, there is a performance trade-off introduced by supporting larger graphs, and simpler design might be more beneficial for smaller data-sets such as the ones in our intended use-case. Reduced-precision arithmetic has not been thoroughly studied in the context of graph ranking algorithms, but encouraging results were shown in numerical analysis and deep-learning [16, 21].

#### **3 PROBLEM DEFINITION**

In this work, we apply a novel SpMV architecture to the computation of Personalized PageRank, an algorithm that provides a *personalized* ranking of the graph vertices, such that vertices that are more *relevant* to an input vertex will have a higher score.

Given a graph *G* with |V| vertices and |E| edges, we represent it using the adjacency matrix **A** and out-degree matrix **D** (a diagonal matrix with the number of out-going edges of each vertex). Define  $\mathbf{X} = (\mathbf{D}^{-1}\mathbf{A})^T$  as the probability of transitioning from a vertex to one of its neighbors<sup>1</sup>, a *personalization vertex v*, and a vector  $\mathbf{p}_t$ of PageRank values, personalized w.r.t. *v*, computed at iteration *t*.  $1 - \alpha$  is the probability of moving to any random vertex, and  $\mathbf{\bar{d}}$  is a *dangling* vector s.t.  $\mathbf{\bar{d}}_i = 1 \Leftrightarrow D_{ii} = 0$ ,  $\mathbf{\bar{d}}_i = 0 \Leftrightarrow D_{ii} \neq 0$ .  $\mathbf{\bar{d}}$  is added to **D** to ensure that the computation is numerically stable [9]. The vector  $\mathbf{\bar{v}}$  is equal to 0 except for the element at index *v*, which is 1. The recurrence equation [3, Section 3] of PPR is

$$\mathbf{p}_{t+1} = \alpha \mathbf{X} \mathbf{p}_t + \frac{\alpha}{|V|} (\bar{\mathbf{d}} \mathbf{p}_t) \mathbf{1} + (1 - \alpha) \bar{\mathbf{v}}$$
(1)

The first term of the right-hand side is a matrix-vector multiplication, while the second and third terms (the *dangling factor* and the *personalization factor*) are obtained with dot-products. The weighted adjacency matrix X is stored in a *sparse format* as it is extremely sparse: in a graph with  $10^6$  vertices and average out-degree 10, only  $10 \cdot 10^6/10^{12}$  (i.e. 0.001%) of the entries of X are non-zero.

Compressed Sparse Column (CSC), a common storage format for sparse matrices [18], can be inefficient for real-world graphs with vertex degrees that follow an exponential distribution, as it limits pipelined architectures that demand precise knowledge of data boundaries. Instead, we employ the COO storage layout (fig. 1), which uses three equally sized arrays, containing, for each entry, its value and its two coordinates. COO simplifies array partitioning, enables burst reads from memory, and pipelined hardware designs, as entries are independent and the architecture is not bound to knowing the degree of each vertex. Instead, CSC-based designs often fail to handle graphs with exponential distribution, especially if stream-like processing is demanded.

We compute  $\kappa$  *personalization* vertices in parallel, to batch multiple user requests. We replace  $\mathbf{p}_t$  with a matrix  $\mathbf{P}_t$  of size  $|V| \times \kappa$ , and  $\bar{\mathbf{v}}$  with a matrix  $\bar{\mathbf{V}}$ . Updating  $\mathbf{P}_t$  requires reading all the edges only once. This optimization boosts the efficiency of a memory-bound algorithm, and enables higher throughput and scalability.

#### **4** IMPLEMENTATION

We present the building blocks of our SpMV architecture and how we integrated it in the PPR computation, our intended use-case.

#### 4.1 Personalized PageRank Implementation

Alg. 1 contains the pseudo-code of the main PPR computation. The input graph is read from DRAM, with edges as packets of size  $P\_SIZE = 256$  to maximize the throughput of memory transactions, and process *B* edges per clock cycle (8, if  $P\_SIZE = 256$  bits and each value is 32 bits). Lines 6-8 of Alg. 1 are the core of PPR, with the SpMV computation further detailed in alg. 2 and fig. 2. The  $\kappa$  entries of the scaling vector are computed as the sum of current PPR values of vertices with no outgoing edges. Values in the *dangling* bitmap are read in blocks with size  $P\_SIZE$ , while **P** is cyclically partitioned to access *B* contiguous values in a single clock cycle. PPR values are stored as reduced-precision fixed-point values. Quantization truncates to zero the fractional bits with precision higher than representable. Other policies (e.g. rounding to the closest representable value) resulted in numerical instability.

4.1.1 SpMV Design. Our SpMV architecture has 4 main steps. First, we read a graph packet from DRAM (lines 4-5 in alg. 2), and store it in local buffers x, y, val to read and update B values at once. While we compute  $\kappa$  PPR vectors in parallel, the edges of the graph are accessed only once. Parallel accesses to  $P_t$  retrieve PPR values for each *personalization* vertex: thanks to UltraRAM, we perform these accesses with low latency, without imposing strong constraints on the graph size. The *B* aggregator cores (lines 12-17) combine *point-wise* contributions to obtain the total contribution of a single vertex, as a packet can contain multiple edges referring to it. Each aggregator considers edges whose end is in the range [x[0], x[0]+B], i.e. the maximum range that can be found in a packet.

4: $\mathbf{P}_1[k] = \bar{\mathbf{V}}[k]$ 5: <b>for</b> $i \leftarrow 0$ , max_iter <b>do</b>	_iter) t PR=1 on pers. vertices
3: <b>for</b> $k \leftarrow 0, \kappa$ <b>do</b> $\triangleright$ Se 4: $P_1[k] = \bar{V}[k]$ 5: <b>for</b> $i \leftarrow 0, max_iter$ <b>do</b>	t PR=1 on pers. vertices
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5: <b>for</b> $i \leftarrow 0$ , max_iter <b>do</b>	
·	
$(\mathbf{D}, \bar{\mathbf{J}})$	
6: $scaling\_vec \leftarrow scaling(P_1, d)$	▷ <i>i.e.</i> $\frac{\alpha}{ V } \mathbf{P}_1 \bar{\mathbf{d}}$
7: $SpMV(coo_graph, P_1, P_2)$	▶ <b>Xp</b> <sub>i</sub> in eq. (1)
8: $\mathbf{P}_1 = \alpha \mathbf{P}_2 + scaling\_vec + (1 - 1)$	$lpha)ar{\mathbf{V}}$
9: Write $P_1$ to output	

 $<sup>^1 {\</sup>rm assuming}$  uniform probability, the probability of moving from a vertex x with outdegree d to a neighbor y is 1/d

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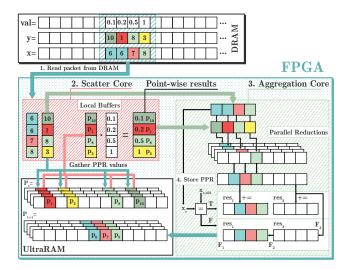


Figure 2: Representation of our SpMV architecture. The *scatter* and *aggregation* cores show the computation for a single vertex, but they are replicated to support  $\kappa$  vertices. Large arrows represent a streaming transfer between cores

The last step adds PPR contributions of the current packet to the PPR arrays stored in UltraRAM. Contributions are stored in a buffer of size 2*B*, with up to *B* non-zero contiguous values. A Finite-State Machine with 2 buffers of size *B* accumulates PPR entries and writes them to output at indices multiple of *B*, ensuring that updates can be performed in parallel as they are aligned to the partitioning factor of  $P_{t+1}$ . Each block of *res*<sub>1</sub> is written on UltraRAM only once to avoid expensive += operations and Read-After-Write (RAW) conflicts in unrolled loops. The 4 main steps of the algorithm, presented here as a single loop (alg. 2, line 2), are implemented as separate modules in a streaming *data-flow* region, enabling aggressive pipelining of loops and better resource allocation.

4.1.2 PPR Buffers Design. Temporary PPR values are stored in UltraRAM (URAM), a type of memory available in recent Xilinx UltraScale+<sup>TM</sup> FPGAs. UltraRAM can be seen as a middle-ground between slow but abundant DRAM and faster, but limited, BRAM. Using a Xilinx Alveo U200 Accelerator Card, we store up to 90MB of data on UltraRAM, corresponding to around 20 million different PageRank values, assuming that the PageRank value of each vertex is stored in 32-bits. In practice, reduced fixed-point precision allows us to store even more vertices, and scale to larger graphs. The maximum number of edges is bound by the available DRAM, and could reach about 5 billion on the 64GB of DRAM available in the Alveo U200 card. Our design can be easily scaled to compute multiple PPR vectors in parallel, if the end-user can provide an upper bound over the number of vertices in its graphs. In our experiments, optimal performance results are achieved if the number of vertices does not exceed 1 million (which is still larger than what is found in many real applications), and 8 to 16 personalization vertices are computed in parallel, using the same hardware resources required for a larger graph that does not consider multiple PPR vertices.

Alg	sorithm 2 COO SpMV						
1:	function SPMV( $coo_graph$ , $P_t$ , $P_{t+1}$ )						
2:	for $i \leftarrow 0 E /B$ do						
3:	I. Process COO in packets of size B						
4:	$x \leftarrow coo\_graph.x[i]; y \leftarrow coo\_graph.y[i]$						
5:	$val \leftarrow coo\_graph.val[i]$						
6:							
7:	<b>for</b> $k \leftarrow 0\kappa$ <b>do</b> $\triangleright \kappa$ personalization vertices						
8:	> 2. Update edge-wise PPR values						
9:	for $j \leftarrow 0B$ do						
10:	$dp\_buffer[k, j] = val[j] \cdot \mathbf{P_t}[k, y[j]]$						
11:	> 3. Aggregate partial PPR values						
12:	for $b1 \leftarrow 0B$ do						
13:	for $b2 \leftarrow 0B$ do						
14:	$agg\_res[k, x[0] \% B + b1] +=$						
	$dp\_buffer[k, b2] \cdot ((x[0] + b1) == x[b2])$						
15:	4. Store PPR values on each vertex						
16:	$x_s \leftarrow \lfloor x[0]/B \rfloor \cdot B$						
17:	if $x_s == x_s$ old then						
18:	for $j \leftarrow 0B$ do						
19:	$res_1[k, j] += agg\_res[k, j]$						
20:	$res_2[k, j] += agg\_res[k, j + B]$						
21:	else						
22:	for $j \leftarrow 0B$ do						
23:	$res[k, j + x_{s_old}] = res_1[k, j]$						
24:	$res_1[k, j] = res_2[k, j] + agg\_res[k, j]$						
25:	$res_2[k, j] = agg\_res[k, j + B]$						
26:	$reset(agg\_res); x_{s\_old} \leftarrow x_s$						

The size of local memory buffers is not a limitation on the size of the graphs: first, our PPR implementation targets graphs encountered in social network communities and e-commerce platforms, whose size does not fill the available FPGA hardware resources [13]; second, there exist partitioning techniques [18, 20] that handles large web-scale graphs. Scalability to web-scale graphs, although not required in our use-case or to validate the performance of our SpMV implementation, is very interesting; these approaches, however, are mostly orthogonal to our design and integrating them would not demand a deep rethinking of our architecture.

### 4.2 Host Integration

Our architecture follows a host-accelerator model in which the *host* (a server) communicates with the *accelerator* (an FPGA) over PCIe. Pre-processing (e.g. loading the graph) is done once at the start and not for each computation of PPR, and it takes a negligible amount of time (< 1% of the execution time). Re-synthesizing the architecture is required to change the fixed-point precision,  $\kappa$  or the maximum number of vertices in URAM, but not for different input graphs.

## **5 EXPERIMENTAL EVALUATION**

Our architecture is implemented on a Xilinx Alveo U200 Accelerator Card with 64 GB of DRAM (77 GB/s of total bandwidth) and equipped with a xcu200-fsgd2104-2-e FPGA offering 960 Ultra-RAM blocks of 288Kb (with 72 bits port width) and 4320 BRAM

Table 1: Summary of graph datasets used in the evaluation

$ \mathbf{V} $	E	Sparsity
$\begin{array}{c} 10^5 \\ 2 \cdot 10^5 \end{array}$	1002178 1999249	$10^{-4}$ $4.9 \cdot 10^{-5}$
$\begin{array}{c} 10^5 \\ 2 \cdot 10^5 \end{array}$	1000000 2000000	$10^{-4}$ 5 · 10^{-5}
$\begin{array}{c} 10^5 \\ 2 \cdot 10^5 \end{array}$	999845 1999825	$\begin{array}{c} 0.99 \cdot 10^{-4} \\ 4.9 \cdot 10^{-5} \end{array}$
128000 81306	443378 1572670	$\begin{array}{c} 2.7 \cdot 10^{-5} \\ 2.3 \cdot 10^{-4} \end{array}$
	$     \begin{array}{r}       10^{5} \\       2 \cdot 10^{5} \\       10^{5} \\       2 \cdot 10^{5} \\       10^{5} \\       2 \cdot 10^{5} \\       128000     \end{array} $	$\begin{array}{cccc} 10^5 & 1002178 \\ 2 \cdot 10^5 & 1999249 \\ 10^5 & 100000 \\ 2 \cdot 10^5 & 200000 \\ 10^5 & 999845 \\ 2 \cdot 10^5 & 1999825 \\ 128000 & 443378 \end{array}$

Table 2: Resource usage, power consumption of our design. Other bit-widths, omitted for brevity, show the same trends

Bit-width	BRAM	DSP	FF	LUT	URAM	Clock (MHz)	10.001
20 bits	14%	3%	4%	26%	20%	220	34 W
26 bits	14%	3%	4%	38%	20%	200	35 W
32 bits, $\mathbf{float}$	14%	48%	35%	89%	26%	115	40 W
Available	4320	6840	2364480	1182240	960		

blocks with 18Kb size each. This FPGA platform is mounted on a server with an Intel Core i7-4770 CPU @ 3.40GHz with 4 cores (8 threads) and 16 GB of DRAM. We compare our PPR implementation against the floating-point implementation in PGX 19.3.1  $^2,\,\mathrm{a}$ powerful toolkit for in-memory graph analytics. Its state-of-the-art implementation of PPR [8] is fully multi-threaded. Experiments with PGX were conducted on a machine equipped with two Intel Xeon E5-2680 v2 @ 2.80GHz with 10 cores (20 threads) each, and 384 GB of DRAM. We analyze 5 versions of our architecture: 26 bits unsigned fixed-point (Q1.25), 24 bits (Q1.23), 22 bits (Q1.21), 20 bits (Q1.19), and a 32-bit floating point version (F32). Lower bit-width negatively impacts the quality of results, while higher precision provides minimal gain (section 5.3.2). The CPU baseline uses 32 bits floating-point arithmetic, and our CPU does not support arbitrary precision. Simulated fixed-precision arithmetic resulted in lower CPU performance, and is not a meaningful comparison. Manually batching multiple requests in PGX through vector properties did not provide a speedup over the fast default implementation of PPR, which is already fully exploiting the CPU [24].

Our experimental setup contains 8 graphs (table 1): 6 are generated using different statistical distributions offered by the Python networkx library<sup>3</sup>, while 2 are real-world graphs from the Stanford Large Network Dataset Collection [13]. Synthetic graphs are consistent in size, edge distribution, and sparsity to real-world graphs used in e-commerce and social network communities [13]; their COO representation has size in line with recent work on sparse matrices on FPGAs [6]. Synthetic graphs with identical sizes highlight how trends are similar across distributions (section 5.1, section 5.3),

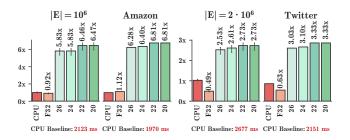


Figure 3: Speedup of our FPGA implementation (y-axis) w.r.t. the CPU baseline, for decreasing bit-widths (x-axis).

and we can extract insights on the convergence and precision of PPR as we change input graph and bit-width.

#### 5.1 Execution time

We measure for each graph the time required to compute the PPR values for 100 random *personalization* vertices, to simulate a realistic batch workload performed by social networks and e-commerce platforms. Time spent transferring results from FPGA to CPU is included, and is negligible compared to the total execution time. All tests are executed with an  $\alpha$  of 0.85, for 10 iterations each (even a low amount of iterations is enough for convergence, see section 5.3.2).

Figure 3 reports the speedups of different fixed-point sizes compared to the CPU baseline and to an equivalent 32-bits floatingpoint FPGA architecture. Reducing bit-width shows a positive correlation with clock speed, and higher speedups. On graphs with around 10<sup>6</sup> edges we obtain up to **6.47x** speedup, thanks to the reduced bit-width and the ability to compute 8 PPR vectors at once. Results for synthetic graphs are averaged, as no difference was observed among distributions. We achieve similar results on realworld graphs, with up to **6.8x** speedup on the highly sparse Amazon co-purchasing network. The time required by the FPGA for 100 random requests ranges from 280 ms for Amazon to 1000 ms for larger graphs, which is in line with the real-time requirement of our use-case. The floating-point FPGA architecture is 6 times slower than the fixed-point designs, with larger DSP usage (48% vs 3%), and negligible accuracy gain compared to 26-bits fixed-point (fig. 4).

The clock frequency is between 200 and 220 MHz, but we can reach up to 350 MHz with lower number of concurrent PPR vertices  $\kappa$ . The clock speed increases sublinearly w.r.t  $\kappa$  above 200 MHz, limiting the benefits of very low  $\kappa$ . On larger graphs the speedups are less significant, as higher URAM utilization negatively impacts the clock frequency due to routing congestion. In our experiments, doubling the size of the PPR buffers lowers the clock speed by around 35-40%. Resources utilization (summarized in table 2 for  $\kappa = 8$ ), is minimal for BRAM, DSPs and registers and is not impacted by fixed-point bit-width and PPR vector size. URAM usage grows linearly with PPR vector size (from 20% to 40% in our experiments).

# 5.2 Energy Efficiency

Our FPGA architecture uses 35W during execution, and increasing the PPR buffer or the fixed-point bit-width does not seem to affect the power consumption. The CPUs consume around 230W, and

<sup>&</sup>lt;sup>2</sup>docs.oracle.com/cd/E56133\_01/latest/index.html

<sup>&</sup>lt;sup>3</sup>networkx.github.io/documentation/stable/

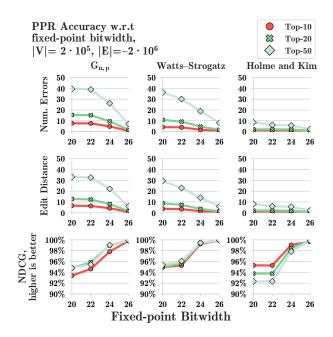


Figure 4: Accuracy metrics for graphs with  $2 \cdot 10^6$  edges, with increasing fixed-point bit-width. Number of errors and edit distance should be low, while NDCG must be close to 100%.

our architecture provides a Performance/Watt gain from **16.5x** to **42x** compared to it (geomean **28.2x**). Even against a faster CPU or a GPU, our architecture is likely to offer higher energy efficiency. Using fixed-point provides **5x** higher energy efficiency over the equivalent floating-point design, which however provides **2.5x-5x** higher energy efficiency than the CPU baseline (geomean **4.3x**).

#### 5.3 Accuracy Analysis

We compared the accuracy of the rankings obtained with fixedpoint precision (after 10 iterations of PPR) with the ones of the CPU implementation at convergence (with at least 100 iterations), using common Information Retrieval (IR) ranking metrics [17]. 100 iterations are enough to reach convergence even in web-scale graphs [12], although 10 iterations would often suffice (fig. 4, fig. 7).

*5.3.1* Accuracy metrics. First, we look at the **number of errors**, i.e. the number of vertices with wrong ranking in the top 10, 20 and 50 compared to the CPU. This metric is very coarse-grained, as a single mistake can greatly affect the ranking: for example, if the correct top-4 values are {2, 4, 8, 6} and we retrieve {4, 8, 6, 2}, this metric reports 4 errors, although only a single value is displaced.

**Edit Distance** counts how many operations are needed to transform one sequence of top-N vertices into another [14]; it handles ordering shifts: in the previous example the edit distance is just 1, as we insert 2 at the beginning and ignore values after the first N.

**Normalized Discounted Cumulative Gain (NDCG)** [10] is commonly used to evaluate recommender systems: it dampens the *relevance* of a vertex by a logarithmic factor such that highly ranked vertices contribute more to the *cumulative gain*. Given a vector of PPR scores,  $rel_i = |V| - i$  is the *relevance* of the *i*-th vertex, and we define Discounted Cumulative Gain (DCG) as in eq. (2). DCG is normalized by the *Ideal DCG* of the CPU implementation.

$$DCG = \sum_{i=1}^{|V|} \frac{rel_i}{log_2(i+1)} \qquad nDCG = \frac{DCG}{IDCG}$$
(2)

5.3.2 Accuracy Discussion. Figure 4 shows how metrics change by lowering the fixed-point bit-width, for each of the  $2 \cdot 10^6$  edges graphs. Figure 5 shows additional accuracy metrics, aggregated on all graphs: *Mean Average Error* (MAE), *Precision* and *Kendall's*  $\tau$ . MAE evaluates how far FPGA PPR values are from the correct ones, while Precision measures the top-N correctness without looking at the vertices order; just 20 bits are enough to retrieve 90% of the best top-50 items. Kendall's  $\tau$  is a ranking metric that penalizes outof-order predictions [19]. Results in fig. 5 are similar to fig. 4, with MAE and Precision mostly unaffected by a larger set of predictions.

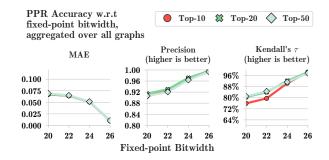


Figure 5: Aggregated accuracy metrics show trends in-line with fig. 4, and even low bit-width provides good predictions

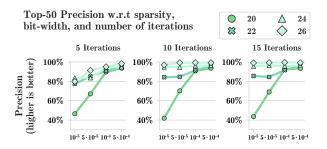


Figure 6: Sparsity does not affect accuracy, except for very low bit-width, and 10 iterations are enough for convergence. Other metrics show similar trends as the top-50 Precision

Increasing bit-width is always beneficial, with diminishing returns. Using 26 bits provides near-to-perfect results, although even 22 or 24 bits provide satisfactory results, with more than half of the vertices being ranked correctly. 22 bits show a top-10 edit distance of 3 and an NDCG value > 95%. With 26 bits, the top-20 edit distance is < 3, i.e. only 3 values in the first 20 are out-of-place. Results are impacted by graph distribution: *Holme and Kim* graphs, for which errors are lower, have dense communities, similarly to real social networks, while the behavior of the other 2 models is more unpredictable. Sparsity has a minor impact on accuracy (fig. 6): very

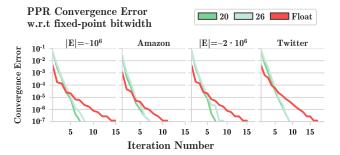


Figure 7: Fixed-point gives 2x faster convergence compared to floating-point. Lines are truncated for error below 10<sup>-7</sup>

low bit-width suffers from high sparsity, but in general results are consistent with Figure 4. We display the top-50 precision due to space limitations, but other metrics show identical behaviors.

Fixed-point arithmetic produces faster convergence (fig. 7). We measure, after each iteration, the Euclidean norm of new and previous PPR values, to evaluate convergence. Less than 20 iterations are always enough for convergence, and even 10 iterations provide an error below  $10^{-6}$  (a common convergence threshold for PPR [1]). Fixed-point arithmetic converges twice as fast compared to floating-point, while preserving accuracy (fig. 4). In real computations, PPR stops when the error is below a threshold: a 2x faster convergence immediately translates to an additional 2x speedup over a floating-point implementation. Lower bit-width provides 10-20% faster convergence in synthetic graphs.

#### 6 CONCLUSION AND FUTURE WORK

We presented a high-performance FPGA implementation of a COO SpMV algorithm that leverages data-flow computation and reducedprecision fixed-point arithmetic. We have shown how our architecture accelerates the PPR algorithm and outperform a state-ofthe-art CPU implementation by up to **6.8x**, with up to **42x** higher energy efficiency. With just 26-bits fixed-point values we guarantee a speedup above 5.8x with negligible accuracy loss, with **2x** faster convergence: average top-10 edit is distance below 1 and NDCG is above 99.9% compared to the CPU, showing how graph ranking algorithms can benefit from approximate computing.

Although the present work focuses on the design of a fixed point COO SpMV for a specific use-case and is not a general-purpose graph engine, we deem valuable to integrate partitioning techniques [18, 20] and support web-scale graphs, and study the optimal trade-off between partitioning overheads and FPGA resource utilization. A comparison against modern GPUs is also very interesting: we omitted detailed GPU analyses as we currently lack high-end GPUs comparable to the Alveo U200. The GTX960 at our disposal is as fast as the CPU baseline using nvGRAPH, although Nvidia claims a 3x speedup using a faster Tesla M40 against a CPU similar to ours [1]. We will also apply our reduced precision SpMV on other use-cases, such as graph embeddings [5].

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