Skip to Secure: Securing Cyber-physical Control Loops with Intentionally Skipped Executions

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ABSTRACT

We consider the problem of provably securing a given control loop implementation in the presence of adversarial interventions on data exchange between plant and controller. Such interventions can be thwarted using continuously operating monitoring systems and also cryptographic techniques, both of which consume network and computational resources. We provide a principled approach for intentional skipping of control loop executions which may qualify as a useful control theoretic countermeasure against stealthy attacks which violate message integrity and authenticity. As is evident from our experiments, such a control theoretic counter-measure helps in lowering the cryptographic security measure overhead and resulting resource consumption in Control Area Network (CAN) based automotive CPS without compromising performance and safety.

1 INTRODUCTION

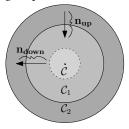
The proliferation of network connectivity has increased the application domain for cyber-physical systems (CPS) in today's connected world. However, increased connectivity manifests security vulnerability in terms of increased number of possible attack surfaces for such systems. Recent results have established that network based *Man-in-the-Middle* type attacks, like false data injection on cyberphysical control systems are quite capable of disturbing closed loop stability as well as degrading the control performance of such systems [25]. In such an attack, an adversary injects false data in the communication medium between the plant and the controller with the intention of driving the system to an unsafe state by changing the set point of the system.

State-of-the-art detection systems: In order to detect such attacks, the most common control theoretic countermeasures put in place are threshold based anomaly detectors that generate an alarm if the estimation error crosses the threshold over a single or multiple control loop iterations. Though such control theoretic primitives can limit the attacks, it has been observed that stealthy attacks are possible even in the presence of such state estimation based lightweight control theoretic intrusion detectors [24]. Hence, the standard way to secure a system against such attack is the use of security primitives like Message Authentication Codes (MACs) [21], Message Encryption [21], Physically Unclonable Functions (PUFs) [8] etc. Some recent efforts also focus on learning based [15, 26] intrusion detection mechanisms. However, the options for implementing such security primitives in CPS is often limited by the available compute resources in the on-board platforms. Hence, there have been proposals [11] for sporadic usage of such Intrusion

Detection Systems (IDS) for securing messages exchanged between software-based controllers and physical plants.

CPS operation under Sporadic IDS: A sporadic IDS can be specified by a pair (n_{up} , n_{down}) such that the IDS is active for n_{up} consecutive control samples and inactive for n_{down} consecutive control iterations, and this behavior repeats in a cycle. As shown in Fig.1, let for a control system, there exists an *initial region C* which is composed of the initial range of plant state values.

Starting from *C*, consider that the preferable operating region for the system is given by an *inner safety region* $C_1(C \subseteq C_1)$ in the absence of any external attacks. The safety guarantee offered by a sporadic IDS is based on the existence of an *outer safety region* $C_2(C_1 \subset C_2)$ which meets the safety requirements of the system, but may not be a preferable operating region for unsatisfactory



operating region for unsatisfactory Figure 1: Sporadic IDS control performance. The IDS parameters, n_{up} , n_{down} can be formally defined as,

 $x[k] \in C_1 \implies \forall i \le n_{down}, x[k+i] \in C_2$ when IDS is off $x[k] \in C_2 \implies \forall i \ge n_{up}, x[k+i] \in C_1$ when IDS is on

where x[k] denotes the plant state at any time instant k. When an IDS is not available for n_{down} consecutive control iterations, stealthy attacks (similar to [11]) which the control system is hoodwinked to think as environmental noise are possible. The period n_{down} should be small enough to ensure that starting from $\in C_1$, such attacks should not steer the system outside C_2 . When the IDS is active for n_{up} consecutive control iterations, no false data injection attack is possible. The period n_{up} needs to be large enough to ensure that the system is brought inside C_1 starting from anywhere $\in C_2$. This ensures that the system duly recovers from the effect of false data injected during the period when IDS was inactive thus nullifying attacker's efforts.

Attack resilience of a system: Attack resilience of an IDS enabled CPS is measured by the value of n_{down}/n_{up} . Let d_{min} be the minimum attack-length, i.e., the minimum number of consecutive control samples required by an attacker to drive the system out of C_2 (starting $\in C_1$) while remaining undetected (thus defining a minimum effort successful attack). We can bound the down-time n_{down} of an IDS as $n_{down} < d_{min}$. This allows us to set a maximum down time of $n_{down} = d_{min} - 1$ in order to stop the attacker before being successful. Thus, increasing d_{min} with suitable choice of CPS parameters in-turn increases the attack resilience (i.e., n_{down}/n_{up}) of the system. Furthermore, the increment in n_{down} proportionally reduces the computational and communication requirement of the IDS. Considering resource-constrained CPS implementation platforms, it is always desirable to go for lightweight provably secure IDS schemes by maximizing down-time (i.e., n_{down}) without sacrificing safety and and performance in the presence of stealthy attacks, which is the focus of this work.

Motivation and Problem statement: Computing control law over falsified sensor measurements can actually drive a CPS towards an unsafe state. Hence, in order to minimize the effect of false data injection in sensor measurements, it may be useful to skip the control law computation in some carefully chosen sampling instants while ensuring that such occasional execution skips do not hamper the desired control performance. The system does not get affected by malicious data injected by the attacker into the communication channel at sampling instants when the control executions are skipped. So, even if the attacker is aware of the positions of skipped executions, it has to try longer to make the system unsafe by fault data injection. When the system is running following some carefully chosen *control skipping pattern* unknown to attacker, the attacker may potentially require longer periods of attack efforts to guess the skip positions and efficiently inject faulty data into the system in order to succeed. In the present work, we motivate employing execution skips as a secure control mechanism. Our proposed framework considers a CPS specification and automatically synthesizes control skipping patterns which maximize the attack resilience without compromising the desired control performance of the system. The synthesis process also provides us an IDS activation schedule with minimized computational cost as a by-product.

Proposed approach and Contributions: The above mentioned goals require setting up and solving a non-linear multi-objective optimization problem. The problem is non-trivial since we want to 1) maximize attack resilience, while also retaining 2) the control performance as much as possible. Note that both these objectives are highly dependent on the positions of execution skips in the control schedule and they do not follow a monotonic relationship. The pattern exhibiting best control performance may lack in attack resilience. Also, the dependence of control performance on the skipping pattern of a control schedule is nonlinear [7]. Hence, formulating a single step optimization framework for maximizing both control performance and attack resilience of a CPS is not a scalable approach. For this reason, we propose a two-step optimization framework. In the first step, we synthesize a set of control skipping patterns that are ranked based on their control performance. In the next step, we analyze the attack resilience of these patterns using Satisfiability Modulo Theory (SMT) based techniques. Higher attack resilience in-turn guarantees less usage of IDS along with the underlying computing and communication platforms. In summary, our contributions can be listed as follows.

(1) We present the first work that motivates the use of intentional *execution skips* as a control-theoretic security measure.

(2) In order to formally analyze the robustness of this measure, we build an SMT based algorithmic framework for synthesizing successful but stealthy false data injection attack vectors.

(3) We leverage this framework for designing sporadic IDS with increased down-time (or more attack resilience) when compared with existing sporadic IDS schemes used with period control implementations (i.e., without execution skips) [11].

(4) Since the pattern search space is exponential in pattern length, we develop a pruning mechanism for classifying control skipping patterns based on their offered performance. This step is instrumental in rendering our method scalable for sporadic IDS design.(5) We establish the usefulness of our approach by considering automotive system examples where sporadic IDS solutions generated by our tool set provided performance and security guarantees similar to previously reported schemes while consuming less communication bandwidth and computational resources.

2 MODEL DESCRIPTION

This section briefly describes the model of the plant and controller, followed by mathematical description of CPS under attack.

2.1 Control System Modeling

A physical plant can be represented as a linear discrete-time invariant system (LTI) having the dynamical equations given as follows.

$$x[k+1] = Ax[k] + Bu[k], \quad y[k+1] = Cx[k+1]$$
(1)
$$\hat{x}[k+1] = A\hat{x}[k] + Bu[k] + L(y[k] - C\hat{x}[k]), \quad y[k+1] = K\hat{x}[k+1]$$

Here x[k] is the value of state variable at k-th iteration, which is being controlled by control input u[k] calculated by the controller based on the estimated state $\hat{x}[k]$. In this work, we consider Kalman Filter [13] for state estimation and Linear Quadratic Regulator (LQR) based optimal control technique for calculating the control input. The control input is received by actuators in plant side and control action can not be exerted beyond the actuator saturation limit. In Eq. 1, the estimated state is calculated using the Kalman Gain, L and output measurement y[k]. Plant outputs are sampled by sensors and transmitted provided they are within supported sensing ranges. The matrices A, B, C, D are system matrices and constant in nature. For a plant-control loop (P, K) with K as the state feedback gain, we define $X[k] = [x^{\mathsf{T}}[k] \hat{x}^{\mathsf{T}}[k] u[k]^{\mathsf{T}}]^{\mathsf{T}}$ as state vector for the augmented system comprising both the plant and estimator states along with control inputs. The augmented system helps analyze the effect of execution skips on the closed loop. The dynamical equation for the augmented system is given by, $X[k+1] = A_1 X[k]$,

where
$$A_1 = \begin{bmatrix} A & 0 & B \\ LC & A - LC - BK & 0 \\ KLC & KA - KLC - KBK & 0 \end{bmatrix}$$
. If the execution of

the controller is intentionally skipped inside a sampling interval [k, k + 1), no new control update is communicated to the plant and state estimation unit in that sampling instance but sensor update is received. Therefore, the plant state is updated using the last communicated control input from previous iteration i.e., u[k + 1] = u[k] and state space equations change as follows.

$$\begin{aligned} \mathbf{x}[k+1] &= A \,\mathbf{x}[k] + B \,u[k], \quad u[k+1] = u[k] \\ \hat{\mathbf{x}}[k+1] &= LC \,\mathbf{x}[k] + (A - LC) \,\hat{\mathbf{x}}[k] + Bu[k] \end{aligned}$$
(2)

Following Eq.(2), during control skips the augmented system progresses with $A_0 = \begin{bmatrix} A & 0 & B \\ LC & A - LC - BK & 0 \\ 0 & 0 & I \end{bmatrix}$ instead of A_1 . Next, we define the notion of *control skipping pattern* as follows.

DEFINITION 1. Control Skipping Pattern : An *l*-length control skipping pattern for a given control loop (P, K), is an *l* length sequence $\rho \in \{0, 1\}^l$ such that it can be used to define an infinite length control schedule $\pi = \rho^{\omega}$, repeating with period *l*, i.e., $\pi[k] = \pi[k + l] = \rho[k\%l], \forall k \in \mathbb{Z}^+$.

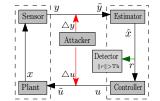
The evolution of the closed loop system according to a control skipping pattern can be exemplified as: for $\rho = 110010$, we have,

$$X[6] = A_1 X[5] = A_1 A_1 A_0 X[3] = \ldots = A_1 A_1 A_0 A_0 A_1 A_0 X[0].$$

2.2 Control Design and Performance Metrics

The control design metric represents the control objective while designing the controller. One such design metric that we use in this work is *settling time*. It is the time needed by the system output to fall and stay around the reference value (e.g., within 2 % error band). Hence, the controller has to be designed in such a way that given settling time requirement is always met. On the other side, the *control performance* is the measure of quality of control (QoC), i.e., how efficiently the design requirement is met. In this work we consider LQR-based controller design technique. So we use *LQR cost function J* as the performance metric given by, $J = \sum_{k=0}^{\infty} (x^T[k]Qx[k] + u^T[k]Ru[k])$, [1], with $Q \succeq 0$ and R > 0 being symmetric weighing matrices capturing the relative importance that the control designer can give to the state deviation and control effort respectively. Lower the LQR cost better the performance.

A significant amount of work exists in the literature addressing the issue of control design and performance in the presence of execution skips [7, 23, 28]. Given the settling time requirement, T_s , we follow Theorem 4.1 of [7] to calculate the *minimum execution rate*, r_{min} , from T_s . This essen-



rate, r_{min} , from T_s . This essen- **Figure 2: CPS attack model** tially means, to maintain T_s , the controller has to be executed at least $\lceil l \times r_{min} \rceil$ times in *l*-length consecutive control samples, i.e., in an *l*-length control skipping pattern, ρ , there has to be at least $\lceil l \times r_{min} \rceil$ number of '1's. On the other hand, control performance varies with relative positions of the execution skips in a pattern (i.e., distribution of '0's over ρ) [10].

2.3 Attack Modeling

A schematic of a cyber-physical system under stealthy false data injection attacks is given in Fig. 2. We consider a stealthy attack scenario where the communication network has been compromised and an adversary can (i) provide false sensor measurements to the controller, denoted by $\tilde{y}[k] = y[k] + \Delta y[k]$ and (ii) tamper with the control input resulting in $\tilde{u}[k] = u[k] + \Delta u[k]$ received by the actuators. Here, $\triangle y[k]$ and $\triangle u[k]$ are the amount of measurement and actuation errors respectively, induced by the attacker at the k-th iteration, and we express this with an attack vector, $\mathcal{A}[k] = [\triangle u^{\mathsf{T}}[k] \triangle y^{\mathsf{T}}[k]]^{\mathsf{T}}$. Under these circumstances, the estimator estimates corrupted $\hat{x}[k+1]$ (i.e., $\tilde{\hat{x}}[k+1]$) to minimize the residue $r[k] = \tilde{y}[k] - C\hat{x}[k]$ (i.e., the difference between the measurement received and the estimated measurement). Due to such a compromised control sample, the plant states are polluted by the attacker-induced errors. As a result, the manipulated states $\tilde{x}[k]$ are driven towards an unsafe region (outside of C_2). We can formalize the state progression in attacked situation using our augmented system with manipulated state vector, $\tilde{X}[k+1] = A_1 \tilde{X}[k] + B_1 \mathcal{A}[k]$

where, $B_1^{\mathsf{T}} = \begin{bmatrix} 0 & L^{\mathsf{T}} & L^{\mathsf{T}}K^{\mathsf{T}} \\ 0 & 0 & I \end{bmatrix}$. In presence of execution skip, B_1^{T} can be replaced with $B_0^{\mathsf{T}} = \begin{bmatrix} 0 & L^{\mathsf{T}} & 0 \\ 0 & 0 & 0 \end{bmatrix}$, causing minimized perturbations during skipped executions. Note that to the plant and controller these false data injections may get disguised as process and measurement noises. Following existing techniques for *physics based attack* detection [9], we assume the following system protection and attack model.

(1) In our protection system model, the threshold-based intrusion detector flags an attack whenever the residue r[k] surpasses the detector threshold given by some constant Th, i.e., ||r[k]|| > Th, which in turn limits the attacker's effort of manipulation (||.|| denotes vector 2-norm). We can also consider the system to be fitted with popularly used χ^2 based attack detectors since detection criteria in such probabilistic detectors can as well be interpreted as non-probabilistic threshold-based detection techniques [11].

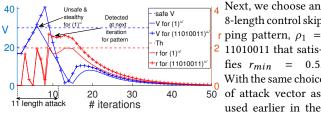
(2) The attacker has full knowledge of the system dynamics and threshold-based detectors present in the system. The attacker can observe the system closely and choose proper false data irrespective of knowing the control skipping pattern. The system supported sensor range and actuator saturation limit impose a bound on attacker's stealthy efforts.

(3) The goal of the attacker is to alter the operating point of the system thereby driving it to an unsafe state $x \notin C_2$ in the least amount of time possible while remaining stealthy. An attack vector of length *d* can be defined as $\mathcal{A}_d = \mathcal{A}[1:d] = \begin{bmatrix} \Delta u_1 & \cdots & \Delta u_d \\ \Delta y_1 & \cdots & \Delta y_d \end{bmatrix}$ The attack vector \mathcal{A}_d launched on a protected control system executing its *k*-th iteration is deemed **1**) *stealthy* if $||r[i]|| \le Th$ for all $i \in [k + 1, k + d + n_{up}]$ where n_{up} is the up-time of the IDS, and 2) successful if $\exists j \in [k + 1, k + d + n_{up}]$ such that $x[j] \notin C_2$, i.e., it violates the safety criterion of the system. Note that we define the stealthiness and success of an attack of length d over a window of $d + n_{up}$ control samples, because an attack of *d*-iterations can drive the system to an unsafe state even after the attack is over. So, we check the safety criteria for a period equal to the attack duration dfollowed by the time n_{up} between the attacker's two consecutive attempts. This setting works because of our additional constraint that during IDS operation for period n_{up} we ensure that the system will converge back inside C_1 .

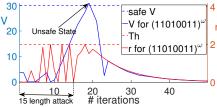
3 A MOTIVATING EXAMPLE

We consider a *trajectory tracking control* (TTC) example to demonstrate the advantage of using control skipping pattern in improving the attack resilience of the system. TTC system regulates deviation (denoted by *D*) of a vehicle from a given trajectory and deviation (denoted by *V*) from a reference velocity by applying proper amount of acceleration as control input. To cope up with the space we refer to Tab. 1 for the system matrices and initial safety regions. Following [7], the settling time criterion of 5 s allows maximum 50% execution skips, i.e., $r_{min} = 0.5$ for this system. The protection system considered in place is a threshold-based anomaly detector having Th = 2. The attacker model is as described in Sec. 2.3.

In Fig. 3a, we consider two possible control schedule scenarios. With the periodic pattern 1^{ω} , there exists an attack vector of length 11 for which the system becomes unsafe at the *6-th* iteration. However, this attack vector is stealthy as the residue is never higher than the threshold. The reason that the attack length need to be much larger than the point of safety violation is because, suddenly stopping the attack after the 6-th iteration will lead to large residue and thereby detection. Hence the attack needs to gradually decrease without drastic modification in system dynamics. In fact, it can be checked that for this system, 11 is the minimum attack length (d_{min}) , i.e. there does not exist any attack vector of length < 11 which is stealthy but successful.



(a) Attack vector for periodic not stealthy on 11010011



With the same choice of attack vector as used earlier in the periodic execution, this time, running the system with the pattern ρ_1 , we observe the following cases. O1. While the 11length attack could

drive the system to

an unsafe state and

remain stealthy for

fully periodic exe-

cution, in case of

execution with the

pattern ρ_1 , it is de-

tected at 9-th itera-

tion just after driv-

ing the system to an

unsafe state at 8-th

Next, we choose an

8-length control skip-

11010011 that satis-

fies $r_{min} = 0.5$.

(b) Stealthy and successful attack for 11010011 with more n_{down}

Figure 3: Plotting V (in blue) in left y-axis and residue r (in red) in right y-axis (in corresponding scales) to demonstrate the effect of stealthy attack on TTC with and without pattern-based execution. V crossing the blue dashed line (safety boundary of V) leads to violation of safety and r crossing the red dashed line (Th) indicates attack is detected.

iteration. This happens because due to the control skips the attacker's efforts in those samples are not affecting the system. This leads to better unbiased estimation in such iterations which may create a large residue resulting detection in future iterations that are under attack.

O2. We also find that no successful but stealthy attack of length d < 15 is possible for this system running with the pattern ρ_1 . System response for this pattern-based execution (ρ_1^{ω}) of the system, with a successful and stealthy attack vector of length d = 15 is depicted in Fig. 3b. The control skips reduce the amount of attack that could have been injected while remaining stealthy. In general, the value of d_{min} is dependent on the choice of pattern because system-behaviour under a control skipping pattern depends on the positions of the control skips and the nature of the system.

O3. Since the minimum attack-length $d_{min} = 15$ in this case, we can set $n_{down} = 14$ increasing the attack resilience (i.e., n_{down}/n_{up}) by $\approx 30\%$ in comparison with the periodic execution ($n_{down}=10)$ for a fixed value of n_{up} . This increment in n_{down} in-turns reduces the computation time of the IDS saving the resource bandwidth.

O4. In general, there may exist multiple patterns that are equally resilient (i.e. with similar d_{min}). Among such patterns with similar resilience, it makes sense to choose the one providing better control performance, e.g. lower LQR cost in our setting. The observations indicate that it is possible for a CPS to be more resilient to false data injection attacks when running with a control skipping pattern when compared with fully periodic execution. However, we need an efficient algorithmic framework in order to search for such performance preserving attack resilient patterns. The next section describes such a framework in detail.

PROPOSED METHODOLOGY 4

As motivated earlier, our framework has two distinct steps which are discussed next.

• *Step-1*: We synthesize a set of control skipping patterns \mathcal{P} , and rank them according to their control performance (ref. Algo. 1). This helps in filtering upfront all the patterns that violate the desired control performance.

• *Step-2*: In this step, we synthesize the set $\mathcal{P}_R \subset \mathcal{P}$ of most attack resilient control skipping pattern(s), which guarantee minimal resource usage and best ranked control performance (ref. Algo. 3). For this, we compute successful yet stealthy attack vectors for control schedules $\in \mathcal{P}$ using Algo. 2.

Synthesizing and Ranking Patterns based 4.1 on Control Performance

Recall that in Sec. 2.2, we already limit the number of allowable execution skips by imposing the constraint of minimum execution rate r_{min} . Yet, for a large *l*, the number of patterns is still very large for testing attack resilience. Moreover w.r.t. resilience, it is important to remember that a pattern under repeated execution is equivalent to any of its cyclic shifts as the attack can start at any point of execution. For example, the patterns 1110 and 0111 are equivalent since one can be derived from another using cyclic shifts. Both represent the same infinite control schedule, i.e. $(1110)^{\omega} = (0111)^{\omega}$. Thus, we need a measure which i) considers any two patterns that are cyclic shifts of each other as equivalent and ii) is also indicative of the control performance of a candidate pattern. Using such a measure to rank patterns provides the following advantage. Patterns whose cyclic shifts are already tested for resilience need not be tested again thus eliminating expensive computation. Since the computation of control performance index J for every pattern requires evaluating a complex quadratic expression, a lightweight equivalent index can help in ranking of patterns w.r.t. performance thus ensuring that our method outputs patterns which are both resilient as well as performance preserving.

In order to model these strategies in the pattern-synthesis approach, we use the correlation between the structure of a pattern (i.e. relative position of skips) and its LQR cost. A well known theory [10] establishes that a pattern having most uniform execution skips (i.e., uniform distribution of '0's) exhibits the lowest LQR cost. The uniformity of binary patterns is defined in literature using the notion of upper mechanical binary word [3]. Following the same we can define the notion of *most uniform skipping pattern* as follows.

DEFINITION 2. Uniform Control Skipping Pattern: An l-length control skipping pattern ρ with number of control execution skips = $\lfloor (1-r_{min}) \times l \rfloor$ (where r_{min} is as discussed earlier), is considered to be

fully uniform when the number of skips in each overlapping q-length sub-sequence of ρ is exactly one, where $q = \lceil l / \{l \times (1 - r_{min})\} \rceil$.

For example, consider $\rho_1 = 101010$ and $\rho_2 = 111000$ which are l = 6 length patterns satisfying $r_{min} = 0.5$. We can claim ρ_1 is a uniform pattern but ρ_2 is not. Because, all 6 overlapping q = 6/3 = 2 length sub-sequences $\langle 10, 01, 10, 01, 10, 01 \rangle$ of ρ_1 contain exactly one '0'(i.e., skip), whereas ρ_2 has only 2 such sub-sequences (3-rd and 6-th) among $\langle 11, 11, \underline{10}, 00, 00, \underline{01} \rangle$. It is understood that the trailing sub-sequences are derived by cyclic rotation of the pattern. With this observation we try to rank the patterns of a given length based on how much they deviate from absolute uniformity. For this we define a function $skipCount(\rho, i, q)$ which outputs the number of '0's in a q-length sub-sequence of ρ starting from $\rho[i]$ (i.e. the *i*-th term of ρ). In case i + q - 1 > l, the sub-sequence under consideration will wrap back to the front, i.e., it will be given by $\rho[i]\rho[i+1]\cdots \rho[l-1]\cdots \rho[(i+q-1)\%l]$. Based on this, we employ the following metric of *non-uniformity* for patterns in our work.

DEFINITION 3. LQR-Distance(): Consider an l-length control skipping pattern ρ with minimum execution rate r_{min} and $q = \lceil l / \{l \times (1 - r_{min})\} \rceil$. For a given ρ , the index LQR-Distance(ρ) is defined as, LQR-Distance(ρ) = $\sum_{i=0}^{l-1} |min(0, skipCount(\rho, i, q) - 1)|$. Given patterns ρ_i and ρ_j , ρ_i is considered more non-uniform than ρ_j if LQR-Distance(ρ_i) > LQR-Distance(ρ_j).

The subtraction of 1 is done since *skipCount* is expected as '1' in all cases for perfect uniformity. Considering the previously used patterns $\rho_1 = 101010$, $\rho_2 = 111000$ (l = 6, q = 2), we have LQR-Distance(ρ_1) = 0, and LQR-Distance(ρ_2) = 2. This gives a measure that among these two patterns with same amount of skip, the control performance of ρ_1 will be better. Also, the measure will be same for all cyclic shifts of a pattern since the definition itself accounts for it. In that way, all patterns with equal length and equal number of execution skips which evaluate to same value of LQR-Distance will be similar in control performance.

We use the measure defined to rank and classify patterns in Algorithm 1. In this algorithm, we consider a user specified pattern length l and number of skips fixed as θ . With this, we first generate all possible *l*-length patterns (Line 3) with θ skips. Then we group patterns with same LQR-Distance in the same set (Line 6). Patterns with cyclic equivalence get automatically grouped with same LQR-Distance value in the data structures called pattern-lists denoted by $s \in S_l$ where S_l is the overall collection of l length patterns with θ skips. For patterns with same LQR-Distance, i.e., in the same pattern-list, we carry out the following pruning operation. For any $\rho \in s$, we eliminate all other patterns which are cyclic shift equivalent of ρ (Line 10) since they are equivalent w.r.t. both performance as well as resilience (as we shall see). Next, we include this pruned set in S' (Line 11). After the pruning is completed for each pattern-list, the collective set is inserted into the final set of patterns \mathcal{P} (Line 12).

4.2 Attack Vector Synthesis

In order to synthesize patterns having best attack-resilience, an important step is to verify the existence of *successful* and *stealthy* attack vectors for patterns under test. We develop a formal approach to synthesize attack vectors for control skipping patterns as outlined

re: pattern length: l ,Exact no. of skips: θ ,	
e: Set of pattern, \mathcal{P} , sorted in ascending order of the LQR (cost
nction Rank_Pattern (l, θ)	
$\mathcal{P}, \mathcal{S}', \bar{\mathcal{S}}_l \leftarrow \Phi;$	▹ Initialized with NULL
$S_l \leftarrow \text{all possible } l \text{ length pattern with } l - \theta \text{ number of }$	'1's; ▶ performance criteria
$q \leftarrow \lceil \{l/\theta\} \rceil;$	▶ the uniformity condition
for each pattern $\rho \in S_l$ do	
$\bar{S}_l[LQR-Distance(\rho, q)] \leftarrow \rho \qquad > \operatorname{grow}$	oup patterns w.r.t. LQR-Distance
for each pattern-list $s \in \overline{S}_I$ do	
for each $\rho \in \mathbf{s}$ do	
for each cyclic shift $\rho' \in \mathbf{s}$ do	
$\mathbf{s} \leftarrow \mathbf{s} \setminus \rho'$	\blacktriangleright omitting cyclic shifts of ρ
$\mathcal{S}' \leftarrow \mathcal{S}' \cup s$	
$\mathcal{P} \leftarrow \mathcal{P} \cup \mathcal{S}';$	
return \mathcal{P} ;	
	e: Set of pattern, \mathcal{P} , sorted in ascending order of the LQR nction RANK_PATTERN(l, θ) $\mathcal{P}, S', \overline{S}_l \leftarrow \Phi;$ $S_l \leftarrow all possible l length pattern with l - \theta number ofq \leftarrow \lceil \{l/\theta \} \rceil;for each pattern \rho \in S_l do\overline{S}_l \lfloor QR - Distance(\rho, q) \rfloor \leftarrow \rho \triangleright gruesfor each pattern-list s \in \overline{S}_l dofor each cyclic shift \rho' \in s dos \leftarrow s \setminus \rho'S' \leftarrow S' \cup s\mathcal{P} \leftarrow \mathcal{P} \cup S';$

in Algorithm 2. We build on earlier work on attack vector synthesis for periodic controllers [14].

Algorithm 2 Attack Vector Synthesis for Pattern-based Execution						
Require: Attack length: d , pattern: ρ , IDS up-time: n_{up} , detector threshold: Th , inner safety region: C_1 , outer safety region: C_2						
Ensure: Attack vector \mathcal{A}_d of length d (if it exists, otherwise NULL)						
1: function SynAttVec(d, ρ, n_{up}, Th)						
2: $x[0] \in C_1; \hat{x}[0] \leftarrow 0; u[0] \leftarrow K\hat{x}[0] \leftarrow 0; y[0] \leftarrow Cx[0];$ > Starting from C_1						
3: $r[0] \leftarrow y[0] - C\hat{x}[0]; \tilde{u}[0] \leftarrow u[0]; \tilde{y}[0] \leftarrow y[0];$						
4: for $k = 1$ to $d + n_{up}$ do						
5: $x[k] \leftarrow Ax[k-1] + B\tilde{u}[k-1]; \hat{x}[k] \leftarrow A\hat{x}[k-1] + Bu[k-1] + Lr[k-1];$						
6: if $k \leq d$ then $\Delta u[k] \leftarrow \text{nondet}(); \Delta y[k] \leftarrow \text{nondet}();$						
7: else $\triangle u[k] \leftarrow 0; \ \triangle y[k] \leftarrow 0;$						
8: if $\rho[k] = 1$ then $u[k] \leftarrow K\hat{x}[k]; \tilde{u}[k] \leftarrow u[k] + \Delta u[k];$						
9: else $u[k] \leftarrow u[k-1]; \tilde{u}[k] \leftarrow \tilde{u}[k-1];$ > Skip Execution						
10: $\tilde{y}[k] \leftarrow y[k] + \Delta y[k]; r[k] \leftarrow \tilde{y}[k] - C\hat{x}[k];$						
11: $\Phi \leftarrow \operatorname{assert}((r[1] \le Th \land r[d+n_{up}] \le Th) \land (x[1] \notin C_2 \lor \lor x[d+n_{up}] \notin C_2));$						
12: if Φ is <i>unsatisfiable</i> then return NULL;						
13: else return $\mathcal{A}_d \leftarrow \begin{bmatrix} \Delta u_1 & \cdots & \Delta u_d \\ \Delta y_1 & \cdots & \Delta y_d \end{bmatrix};$						

The function SYNATTVEC in Algo. 2, symbolically executes the system starting from any initial state x[0] inside the inner safety region C_1 (Line 2) for $d + n_{up}$ control samples following Eqn. (1). In each sample k, we introduce two non-deterministic variables $\Delta u[k]$ and $\Delta y[k]$ to model the actuation and measurement errors introduced by the adversary (Line 6). Attack length is bounded to *d* by setting these variables to zero for each iteration k > d. In case of the skip in *k*-th control execution (i.e., $\rho[k] = 0$), x[k], r[k], y[k]are calculated following Eq. (2) $(u[k], \tilde{u}[k])$ are updated using the last calculated u[k - 1], $\tilde{u}[k - 1]$, in line 9). The function at the end validates an assertion using the SMT solver Z3 [5] to check if any attack of length d that is stealthy over $d + n_{up}$ samples (i.e., until further activation of IDS), violates the safety requirements of the system in any control sample (Line 11). On getting satisfiable solution from the solver, SYNATTVEC() returns a successful attack vector \mathcal{A}_d of length *d* (Line 13). Otherwise it returns NULL. This guarantees that no attack vector of length d exists that remains stealthy over $d + n_{up}$ control samples and successfully violates the safety of the system in any of those samples.

4.3 Synthesizing Attack Resilient Patterns

As described earlier, given a control system, we compute a reduced set \mathcal{P} with fixed length control skipping patterns and fixed number of skips, ranked according to their control performance using Algo. 1. We use the set \mathcal{P} to find a further pruned set of patterns $\mathcal{P}_l \subset \mathcal{P}$ where each $\rho \in \mathcal{P}_l$ has a sporadic IDS specification $\langle n_{up}^{\rho}, n_{down}^{\rho} \rangle$ for a detector threshold *Th*, ensuring the following. **1**) The ranking of the *l* length patterns (w.r.t. descending order of

Algorithm 3 Most Attack Resilient Pattern Synthesis

```
Require: Desired pattern length l, 1-length pattern for periodic control execution: \rho^*, detec-
      tor Threshold: Th, inner and outer safety regions: C_1 and C_2, plant and controller matrices
A, B, C, K, Min. execution rate: r_{min}
Ensure: Set of most attack resilient l length patterns \mathcal{P}_R
1: \theta_{max} \leftarrow \lfloor l \times (1 - r_{min}) \rfloor;

2: for each \theta \in [1, \theta_{max}] do

3: \mathcal{P} \leftarrow \text{RANKPATTERN}(l, \theta);
                                                                     ▶ initializing with maximum number of skips allowed
            n_{up}^{\rho^{\circ}} \leftarrow \text{FINDONTIME}(\rho^*, C_1, C_2); d \leftarrow 1;  
 \triangleright Finding ontime of the IDS, Initializing d
4:
           d^*_{min} \leftarrow \text{MinAttLen}(\rho^*, d, n^{\rho^*}_{up}, Th);
5:
          n_{down}^{\rho} \leftarrow d_{min}^{*} - 1; d_{min} \leftarrow d_{min}^{*}
6:
                                                                                ▶ Initializing with minimum attack length for
           rate_{\rho^*} \leftarrow n_{up}^{\rho^*}/(n_{down}^{\rho^*} + n_{up}^{\rho^*}); rate_{min} \leftarrow rate_{\rho^*};  ▷ Initializing with 1<sup>\omega</sup> IDS
7:
      rate
           for each pattern \rho \in \mathcal{P} do
 8:
                  n_{up}^{\rho} \leftarrow \text{FindOnTime}(\rho, C_1, C_2); d \leftarrow \text{MinAttLen}(\rho, d_{min}, n_{up}^{\rho}, Th);
 9:
10:
                  if d \ge d_{min} then
                       \begin{array}{l} n_{down}^{\rho} \leftarrow d-1; \; rate_{\rho} \leftarrow n_{u\rho}^{\rho} / (n_{down}^{\rho} + n_{u\rho}^{\rho}); \\ \text{if } rate_{\rho} > rate_{min} \; \text{then} \; \mathcal{P} \leftarrow \mathcal{P} \setminus \rho \end{array}
11:
12:
13:
                        else rate<sub>min</sub> \leftarrow rate<sub>\rho</sub>; d_{min} \leftarrow d;
                  else \mathcal{P} \leftarrow \mathcal{P} \setminus \rho
14:
            for each pattern \rho \in \mathcal{P} do
15:
                  if rate_{\rho} = rate_{min} then \mathcal{P}_{l} \leftarrow \rho;
16:
17:
            \mathcal{P}_R[\theta] \leftarrow \mathcal{P}_l
                                                    \blacktriangleright Store l length most attack resilient patterns performance wise
18: return \mathcal{P}_R
19: function MINATTLEN(\rho, d_m, n_{up}, Th)
            d \leftarrow d_m;
repeat d \leftarrow d + 1
20:
21:
                  for i = 0 to |\rho| - 1 do
22
                        \rho' \leftarrow i-times left cyclic shift of pattern \rho;
23:
                        if SynAttVec(d, \rho', n_{up}, Th) \neq NULL then return d - 1;
24:
25:
            until SynAttVec(d, \rho', n_{up}, Th)= NULL
26: function FINDONTIME(\rho, C_1, C_2)
27:
            n \leftarrow 1
28
            for i = 0 to |\rho| - 1 do
29:
                  \rho' \leftarrow i-times left cyclic shift of pattern \rho;
30:
                  repeat
31:
                        x[0] \in C_2; u[0] = 0; r[0] = 0;
32:
                        for k = 1 to n do
                             \begin{array}{l} \hat{x} - 1 & \text{or } k \\ r[k-1] \leftarrow y[k-1] - C\hat{x}[k-1]; \\ \hat{x}[k] \leftarrow A\hat{x}[k-1] + Bu[k-1] + Lr[k-1]; x[k] \leftarrow Ax[k-1] + Bu[k-1]; \\ \end{array}
33:
34:
35:
                              if \rho'[k] = 1 then u[k] = K\hat{x}[k];
36:
                             else u[k] \leftarrow u[k-1];
                                                                                                                              ▹ Skip Execution
37:
                        \Phi \leftarrow \operatorname{assert}(|r[1]| \leq Th \land \cdots \land |r[n]| \leq Th \land x[n] \notin C_1);
38:
                        n \leftarrow n + 1
                  until Φ is unsatisfiable
39:
40:
                  n \leftarrow n - 1
            return n
41:
```

Quality of Control (QoC)) as set by Algo. 1 is maintained in \mathcal{P}_{I} . 2) Given the inner and outer safety regions, C_1 and C_2 , (ref. Fig. 1), starting from anywhere inside C_2 , the system will reach C_1 under a safe scenario with no stealthy attack as guaranteed by an IDS within n_{up}^{ρ} iterations.

3) $(n_{down}^{\rho} + 1)$ is minimum attack length required to drive the system to an unsafe state while remaining stealthy.

tem to an unsafe state while remaining stealthy. 4) Attack resilience, i.e., $(n_{down}^{\rho}/n_{up}^{\rho})$ will be maximum and same for all the patterns in \mathcal{P}_{I} ensuring minimum IDS execution rate, i.e., $n_{up}^{\rho}/(n_{down}^{\rho} + n_{up}^{\rho})$.

We derive such a set \mathcal{P}_l for all allowable number of skips $\theta \in [1, \lfloor l \times (1 - r_{min}) \rfloor]$ (for certain *l* length) and arrange them in increasing order of control skips. The method is outlined in Algo. 3. Here, our goal is to output set of patterns, \mathcal{P}_R , with most attack resilience that would help us design better sporadic IDS schemes with provable security, improved resource utilization ensuring best performance. We define $\rho^* = 1$ as the 1-length pattern representing the periodic execution, i.e., $(\rho^*)^{\omega} = 1^{\omega}$ in order to represent existing IDS schemes in literature.

In Algo. 3, we compute IDS up and down time for any pattern using FINDONTIME() and MINATTLEN() function respectively. FIND-ONTIME() returns the minimum number of iterations required by following the pattern ρ to formally guarantee that the system starting from any state x[k] in the outer safety region C_2 (as a result of successful attack) will be in a state inside the inner safety region C_1 (Lines 26-41). We symbolically simulate attack-free closed loop iterations of the system starting from an initial state $x[0] \in C_2$ according to the pattern ρ' (where ρ' represents a left cyclic shift of the pattern ρ) (Lines 29-31). We use the clause $x[k] \notin C_1$ which implies that the system is not inside the inner safety region C_1 after k iterations (Line 37). This assertion is the negation of our design requirement for the up-time n_{up} of the IDS. If the assertion Φ is found to be unsatisfiable using SMT solver, then our design requirement is valid (Line 39-40). However, if Φ is satisfiable, then we infer that the present IDS up-time, n, is not sufficient to bring the system to the inner safety region C_1 starting from any point in the outer safety region C_2 , and we increase *n* until Φ becomes unsatisfiable (Line 38). We now repeat this procedure to find the maximum value of *n* that satisfies our design requirement over all possible cyclic shifts of the pattern ρ (Lines 30-38). We check for all possible such shifts since the system can start from C_2 while executing any position in the pattern. The value of n thus found is a safe up-time of the sporadic IDS designed using an attack resilient control skipping pattern ρ , i.e. $n_{up}^{\rho} = n$ (Line 41).

The MINATTLEN() function on the other hand computes all possible cyclic shifts of the input pattern as ρ' (Line 23) and calls the function SYNATTVEC() (Line 24) which checks for existence of possible stealthy and successful attack vector of length d (initialized with input length d_m in line 20). If no attack vector of length dexists, we can claim that the system can not be made unsafe with stealthy attack of length d. Hence, we search again for an attack vector by increasing the attack length by 1 (Line 21). Otherwise, on finding a successful and stealthy attack vector of d length, we terminate by decreasing the length by 1 and return the length as minimum attack length (Line 24).

We start Algo. 3 by choosing a certain number of control skips $\theta \leq \theta_{max}$, which is the maximum number of allowed control skips for *l* length pattern, calculated using the length input *l* and minimum execution rate criteria for a system i.e. r_{min} ($\theta_{max} = \lfloor l \times (1 - l) \rfloor$ r_{min} |, Lines 1- 2). For this $\langle l, \theta \rangle$ pair we call RANKPATTERN (l, θ) to get the pruned and Quality of Control (QoC) wise ordered set of *l* length patterns \mathcal{P} . Our aim here is to make the IDS scheme as much sporadic as possible i.e. minimizing the IDS execution rate $(n_{up}/(n_{up} + n_{down})))$ w.r.t. their periodic counterpart by examining all *l* length patterns. So we start our attack resilience analysis with the periodic pattern $\rho^*.$ We derive d^*_{min} i.e., minimum attack length for ρ^* (periodic execution) and update d_{min} with it first. Then we calculate down time for ρ^* , i.e., $n_{down}^{\rho^*} = d_{min}^* - 1$ (Line 5-6). We compute IDS up-time for ρ^* in line 4. Then we initialize $rate_{min}$ with IDS execution rate for periodic execution i.e., $rate_{\rho^*}$ (Line 7). Next, for every pattern $\rho \in \mathcal{P}$, we first calculate the up-time (n_{up}^{ρ}) and minimum attack length (d) for ρ using the functions FINDON-TIME() and MINATTLEN() respectively (Line 9). If d is larger than or equal to d_{min} indicating better attack resilience $(n_{down}^{p}/n_{up}^{p})$ than last found most attack resilient pattern (Line 10), we compute $rate_{\rho}$, the execution rate for the pattern ρ (Line 11). A pattern ρ is removed from \mathcal{P} if $rate_{\rho} > rate_{min}$ since ρ can not reduce IDS utilization when compared to last found best candidate (Line 12). Otherwise, $rate_{min}$ and d_{min} are updated with $rate_{\rho}$ and d respectively (Line 13).

While repeating the above procedure for all patterns ($\forall \rho \in \mathcal{P}$), we pick the patterns with least IDS execution rate ratemin from \mathcal{P} and insert them into \mathcal{P}_l maintaining their actual order (Line 16). This sorted set \mathcal{P}_l has following properties, i.e. $\forall \rho \in \mathcal{P}_l$, (i) $rate_{\rho} = rate_{min}$ among all *l* length patterns with θ number of skips and (ii) all patterns in \mathcal{P}_l are sorted in increasing order of LQR-Distance. We store \mathcal{P}_l derived for all possible skips ($\leq \theta_{max}$) for a fixed length l in \mathcal{P}_R , indexing them with number of skips (Line 17) and finally returning this set (Line 18). In \mathcal{P}_R , the set of patterns with smaller number of skips are better in control performance and patterns with same number of skips are internally sorted (in each entry of \mathcal{P}_R) following uniformity measure. A system running with any of the *l* length control skipping patterns $\in \mathcal{P}_R$ meets the desired performance criteria with best QoC and a sporadic IDS can be designed for this system having a formal guarantee of the security against false data injection attack with minimum IDS activation.

5 RESULTS

We demonstrate the efficacy of our proposed approach considering two systems from the automotive domain. The systems are *Vehicle Dynamic Controller* (VDC) and *Trajectory Tracking Controller* (TTC).

5.1 Case Studies

VDC regulates the lateral dynamics of a vehicle by controlling its side slip (β) and yaw rate (γ) [29]. The control input in this case is the steering angle. For TTC [11], details about the system specifications are given in Sec. 3. For both the systems, system matrices (*A*, *B*, *C*), sampling period (*h*), outer (*C*₂), inner (*C*₁) safety regions of the state variables and detector thresholds (*Th*) are given in Tab. 1. Safety regions are determined following [19, 20].

Table 1: System Specifications

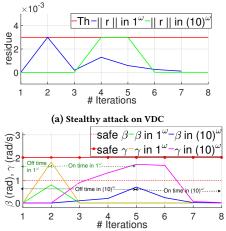
System	Specifications	C_2	C_1	Th
VDC	$\begin{split} A &= [0.4450, -0.0458; 1.2939, 0.4402]; \\ B &= [0.0550; 4.5607]; C = [0,1]; \\ h &= 0.1sec; K = [-0.0987; 0.1420]; \\ L &= [-0.0390; 0.4339] \end{split}$	$ \begin{array}{l} \beta \in [-1,1] \\ \gamma \in [-2,2] \end{array} $	$\beta \in [-0.1, 0.1]$ $\gamma \in [-0.2, 0.2]$	0.003
TTC		$D \in [-25, 25]$ $V \in [-30, 30]$	$D \in [-15, 15]$ $V \in [-18, 18]$	2

For the above systems, we first report in Row 1 of both parts of Tab. 2 the results for sporadic IDS design with fully periodic execution (1^{ω}) similar to [11]. For periodic execution, our method computes IDS up-time $n_{up} = 3, 3$, and minimum attack length $d_{min} = 11, 3$ for TTC and VDC respectively. These are given in Row 1, Col. 4 of both parts in Tab. 2 $(n_{down} = d_{min} - 1)$. Using these, IDS execution rates (rate) of periodic execution are calculated and reported in Col. 5 of Tab. 2. We now apply Algo. 3 considering $r_{min} = 0.5$ for both VDC and TTC as derived from their respective settling time requirements. The value of r_{min} combined with different possible values of l provide us multiple combinations of (l, θ) as given in Col. 2. For each case, Algo. 3 of Tab. 2. If there are multiple such patterns

Table 2: Designed Sporadic IDS schemes for VDC and TTC

Sys.	$\langle \mathbf{l}, \theta \rangle$	pattern	$\langle n_{down}, n_{up} \rangle$	rate	LQR-D
TTC	-	1	10,3	0.2308	-
	10,3	1010011111	15,3	0.1667	3
	10,4	1101011100	14,3	0.1765	1
	10,5	1101001010	13,3	0.1875	1
	11,4	11010111100	15,3	0.1667	2
	11,5	10100101011	13,3	0.1875	1
		10100111010	13,3	0.1875	1
VDC	-	1	2,3	0.6	-
	2,1	10	5,3	0.375	0
	5,2	11010	4,3	0.4286	0
	6,3	110010	5,3	0.375	1
		110100	5,3	0.375	1
		100011	5,3	0.375	2
	10,5	1100101010	4,3	0.4286	1
		1101001010	4,3	0.4286	1
		1000111001	4,3	0.4286	2
	12,6	110001110010	4,3	0.4286	3
		110100111000	4,3	0.4286	3

with same resilience, the algorithm provides them in decreasing order of control performance (i.e. increasing LQR-D for the same (l, θ) in col. 6). For each pattern, the corresponding safe IDS configuration $\langle n_{up}, n_{down} \rangle$ is given in Col. 4 with the IDS execution rate in Col. 5.



For each system, the patterns reported by our automated method as most attack resilient (i.e. requiring lowest IDS usage) are marked in bold. As one may recall, the input *l* and rmin provides the maximum number of skips, i.e. θ_{max} . For TTC, running our method with l = 10, we find the most attack resilient

(b) Higher IDS Off time (n_{down}) for control skipping pattern as $\rho = 1010011111$ (with IDS

rate 0.1667) showing a 27.78% improvement w.r.t. existing periodic IDS with *rate* = 0.2307 (ref. Col. 5, Row 1). For *l* = 11, we have ρ = 11010111100 with similar resilience. For a given *l*, Algo. 3 (Lines 2-17), automatically tries for different values of $\theta \in [1, \theta_{max}]$ and reports only those values which provide better resilience w.r.t. periodic control. So, we do not have entries like (*l*, θ) = (10, 2) and many others. Similarly for VDC, our methodology was tried with different values of *l* and the most resilient solutions are shown in bold resulting in about 37.5% reduction in IDS rate.

For comparison, we consider the effect of a stealthy and successful attack on VDC when it is executing the closed loop following 1^{ω} (periodic) and $(10)^{\omega}$ (best pattern returned by Algo. 3 for l = 2). Our method reveals the the minimum attack length for VDC following 1^{ω} and $(10)^{\omega}$ as 3 and 5 respectively. Fig. 4a shows the residue of the VDC considering an attack scenario which is stealthy since $||r|| \leq Th$ is always satisfied for both 1^{ω} and $(10)^{\omega}$. For the same attack scenario, we plot system states (i.e., side slip β and yaw rate γ) of the VDC in Fig. 4b considering both 1^{ω} and $(10)^{\omega}$. The attack

inflicted during the IDS off time is unable to cross the safety limits (of value 1 and 2 in Y axis) as we activate IDS from 2-nd iteration in case of 1^{ω} and from 5-th iteration in case of $(10)^{\omega}$ depending on their corresponding minimum attack lengths as mentioned earlier. The plot clearly demonstrates that due to the deployment of pattern based execution, the safety of the system is maintained in spite of increasing the down-time of the IDS (from 2 to 5). This validates our principal claim of potential increment in system attack resilience provably improving security by judiciously skipping some control executions. Next, we demonstrate a useful application of the ability to implement provably safe sporadic IDS leveraging control skipping patterns in automotive systems.

5.2 Manifestation on CAN bandwidth

Let us consider an automotive system where the CAN messages are communicated through the bus with a speed of *B* bps at periodicity p_1, p_2, \ldots, p_k such that $p_1 > p_2 > \cdots > p_k$. The number of message types with rate p_i is given by m_i , $i \in \{1, \cdots, k\}$. Assume that IDS is implemented for messages with periodicity $p_{k'}$ and there are $m_{k'} > 0$ number of such types of messages. Similar to [4], we consider a p_1 -length observation window (\geq the largest period) and compute bandwidth consumption in CAN bus for the aforementioned setup through the following steps.

A. We find out the number of messages communicated over the observation window p_1 . For any m_i it is $c_i = \lceil p_1/p_i \rceil \forall i \in [0, k]$. We consider maximum CAN payload for each message, i.e. 64 bits.

B. For each of the m'_k different type of messages, the IDS rate is $rate_i, i \in [1, m'_k]$. If we design the IDS with CMAC/AES-128 (with *a*-bit CMAC) [27] encryption to provide confidentiality and authenticity, payload will be of size (64+*a*) bits. This will convert to $\lceil (64+a)/128 \rceil$ AES blocks or b= $(\lceil (64+a)/128 \rceil \times 128)/64$ CAN frames (CAN payload size=64). In such an arrangement, each CAN frame will be replaced by *b* CAN frames when IDS is active (refer Fig. 5a where b = 4). Hence, over the observation window, each of the $m_{k'}$ messages is transmitted $(1 - rate_i) \times c_{k'}$ times without IDS active and $b \times rate_i \times c_{k'}$ times with IDS active giving a total count of $(1 + (b - 1)rate_i) \times c_{k'}$.

C. Additional 47 bits are added to the payload to form one CAN frame (SOF + Arbitration + RTR + Control + CRC + Acknowledgment + EOF + Interframe Space = 1 + 11 + 1 + 6 + 16 + 2 + 7 + 3 = 47 bits)[4]. Thus, in our consideration, size of each CAN frame is (64+47) bits = 111 bits. Following this, total bandwidth consumption over *observation window* is computed as $T = 111 \times [m_1 + m_2 \times c_2 + ... + \sum_{i=1}^{m_{k'}} (1 + (b - 1)rate_i) \times c_{k'} + ... + m_k \times c_k]/B$. Let the IDS rates for some control skipping pattern, output by Algo. 3 be $rate'_i$, $\forall i \in [1, m_{k'}]$. Since Algorithm 3 ensures if proposed patterns are used $rate'_i < rate_i(\forall i \in [1, m_{k'}])$, the improvement in bandwidth consumption when executing a pattern based schedule compared to a periodic schedule is given as, $(T - T')/T = 111 \cdot \sum_{i=1}^{m_{k'}} ((1 + (b - 1)(rate_i - rate'_i)) \cdot c_3)/T$ considering T' as the bandwidth consumed by pattern based schedule.

Example: Let us consider the following setup of (#message, periodicity): $\langle m_1, p_1 \rangle = \langle 10, 1 \rangle$, $\langle m_2, p_2 \rangle = \langle 20, 0.2 \rangle$, $\langle m_3, p_3 \rangle = \langle 2, 0.1 \rangle (VDC)$, $\langle m_4, p_4 \rangle = \langle 2, 0.1 \rangle (TTC)$ in CAN bus. So, the VDC and TTC both require two types of messages (sensor o/p, control i/p) of period p_3 and p_4 respectively. These are denoted by CAN IDs $1 \cdots 4$ (Fig. 5a).

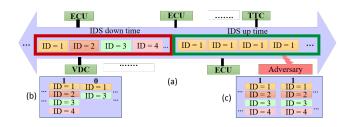


Figure 5: a) CAN Transmissions with sporadic IDS in presence of adversary, b) Message flow for periodic execution, c) Message flow for skipped execution

During skips in the control execution, actuation signals are not communicated as we can see in Fig. 5c, which also frees bandwidth. If the IDS scheme in place uses 128 bit CMAC (i.e. a = 128), it replaces each CAN frame with b = 4 CAN frames when IDS is active (refer Fig. 5a). Following the derived formula for the aforementioned setup, we get 16.25% net improvement in CAN bandwidth consumption using the secure control schedule 10^{ω} for VDC and 1010011111^{ω} for TTC. Considering our methodology to design such pattern based secure control schedules for a significant number of control loops has an additive effect on the bandwidth saving. Thus our methodology helps to design sporadic IDS schemes based on intentional control loop skips which promise better resource utilization in terms of communication bandwidth.

6 RELATED WORK

We provide a brief survey on existing works in the area of secure control which are relevant in the context of the current work. In [17], the authors discuss suitable conditions under which a control system with χ^2 based detectors is stealthily attackable. The performance degradation of such χ^2 detector enabled systems in the presence of stealthy attacks has been quantified in [6]. In [18], the authors report such 'fake disturbance attacks' and their implications in Network Control Systems (NCS) in the presence of deterministic monitoring algorithms. The idea of stealthy attacks on both sensor and actuator sides being able to destabilize automated power generation systems with threshold based detectors has been discussed in [25]. Authors in [2] also discuss security vulnerabilities in automotive CPS domain. Designing resilient control implementations by leveraging secure state estimation techniques, more specifically in the automotive context has been reported in [22]. The idea of sporadically using IDS schemes like MAC computation has been investigated in a different line of works [11, 12, 16], but in the context of periodic control only. In [8], the authors explore the advantage of employing lightweight periodic authentication schemes like Physically Unclonable Functions (PUFs) in the context of cyber physical security as a sporadically available IDS mechanism, again for periodic control. In that work, the periodic availability of the authentication scheme depends on the PUF delay (PUF with high reliability incurs higher delay due to reliability peripherals like error correction, helper data etc). In the current work, we assume that the IDS security primitive is available for n_{up} consecutive iterations followed by an off time for which we are able to establish a guarantee that the performance degradation due to stealthy attacks is inside recoverable limits.

7 CONCLUSION

The present work demonstrates how control skipping patterns can be synthesized guaranteeing desired performance with increased resilience. The safe and resilient patterns generated by the method helped in reducing the computation and communication overhead of IDS schemes employed in Automotive CPS. Integrating our SMT based technique with safe but approximate analysis (e.g. using 'Barrier functions') can help increase the scalability of the approach for applicability in complex industrial test cases. This along with controller synthesis for the joint objective of performance and security are important future extensions possible for this work.

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