

Synthesizing Brain-Network-Inspired Interconnections for Large-Scale Network-on-Chips

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Abstract— Brain network is a large-scale complex network with scale-free, small-world, and modularity properties, which largely supports this high-efficiency massive system. In this paper, we propose to synthesize brain-network-inspired interconnections for large-scale network-on-chips. Firstly, we propose a method to generate brain-network-inspired topologies with limited scale-free and power-law small-world properties, which have a low total link length and extremely low average hop count approximately proportional to the logarithm of the network size. In addition, given the large-scale applications, considering the modularity of the brain-network-inspired topologies, we present an application mapping method, including task mapping and deterministic deadlock-free routing, to minimize the power consumption and hop count. Finally, a cycle-accurate simulator *BookSim2* is used to validate the architecture performance with different synthetic traffic patterns and large-scale test cases, including real-world communication networks for the graph processing application. Experiments show that, compared with other topologies and methods, the brain-network-inspired NoCs generated by the proposed method present significantly lower average hop count and lower average latency. Especially in graph processing applications with a power-law and tightly coupled inter-core communication, the brain-network-inspired NoC has up to 70% lower average hop count and 75% lower average latency than mesh-based NoCs.

Index Terms—network-on-chip, brain-network-inspired, scale-free, small-world, modularity, topology generation.

I. INTRODUCTION

Network-on-chip (NoC) [1] is a promising design paradigm for addressing communication bottlenecks in many-core processors. NoCs replacing point-to-point and shared bus interconnections have been employed to solve complex and large-scale on-chip communication issues because of their scalability, predictability, and modularity [2], [3], [4], [5], [6]. Recently, it is also widely used in wafer-level integration [7] and in-memory computing systems [8], [9], [10],

[11]. In large-scale NoCs, the interconnection topology has a significant impact on power consumption and performance [1], [12]. TrueNorth [8], [13], a high-efficiency in-memory processor, is composed of 4096 neurosynaptic cores tiled in a mesh. Xiao et al. [10] present a scalable in-memory computing-based system where hundreds of vaults are interconnected through a mesh-based NoC. Thousands of cores were integrated in an NoC-based disease diagnosis-on-chip platform for protein folding computation [14]. Cerebras [7], a wafer-scale engine for deep learning, consists of 400,000 programmable computing cores interconnected by a mesh. However, these mesh-based interconnections may be unaccommodated for large-scale network architectures, because NoC with conventional regular topologies generally has an average-hop-count increased, polynomially, with the network size. For example, in a network including n switches connected by mesh, the maximum hop count could be $2n^{1/2}$, which causes an unacceptable global communication latency. As thousands of cores have been integrated into a single chip for enhanced performance and functionality, network topology becomes a key factor in the success of the large-scale NoCs.

From the perspective of low hop count and high energy efficiency of NoC topology, researchers have carried out in application-specific topology and hierarchical topology respectively. Some previous studies [15], [5], [4], [16], [17], [18] have proposed topology generation methods of application-specific NoCs. A series of performance-driven custom topologies were constructed for application requirements. However, the existing generation methods show their effectiveness and efficiency in applications with hundreds of nodes at most due to high algorithm complexity. Other studies have proposed the use of hierarchical topologies, such as dubbed Prism-Mesh[19], CHMesh[20], hierarchical star-mesh [21], and hierarchical ring [22], as attractive solutions to the problem of global long-distance data transmission over large-scale networks, due to its lower average hop count compared with conventional regular topologies. However, for larger network sizes, more high-level switches need to be added to the network, resulting in a large number of switches.

Human brain is a high-efficiency massive parallel computing system combining computing, storage, and communication. Neurobiological studies have shown that the functional network and structural network of human brain are complex, irregular, and high-efficiency communication networks [23]. Although graph theory-based network analysis helps demonstrate the complex organization of human brain networks, how this complexity supports communication processes that are

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fundamental to the brain's computational capacities remains poorly understood [23]. It is generally recognized that these two networks have the properties of scale-free [24], small-world [25], and modularity [26] that to large extent support this high-efficiency system. Networks in which nodes are connected by a power law of node degree distribution are called *scale-free networks* [27]. Such networks have extremely low average communication hop count between any pair of nodes, which is logarithmically (from $O(\ln n)$ to $O(\ln \ln n)$) with network size. Owing to the heterogeneity of the scale-free networks, when failures of nodes occur randomly, most connections between nodes are conserved, so it is robust against structural breakdown. *Small-world networks* [28] have a very low average communication hop count between any pair of nodes, which is usually proportional to the logarithm of the network size. Small-world networks are associated with high global and local efficiency of parallel information processing due to their dense local clustering (modularity). *Modularity* means that the nodes in the network naturally are clustered into tightly connected communities with only sparser connections between them [29]. The modularity of brain networks plays a vital role in promoting stability and flexibility and conserving wiring costs. Therefore, inspired by efficient brain networks, it is of great interest to build an interconnection topology based on these properties for large-scale NoCs to improve the integration scale and reduce interconnection cost. Even better than conventional regular topologies, the brain-network-inspired topology has an extremely lower average hop count between any two nodes, which is logarithmically proportional to the network size. Especially, the brain-network-inspired NoC is more deserving of being explored as a domain-specific solution for graph processing [30], because the large data sets [31] come from social networks, web pages, bioinformatics, and recommendation systems. These large networks of datasets are similar to brain networks and follow a pattern of sparsity and power-law distribution [31].

Earlier research also showed that better network performance can be obtained by only imitating one of the above properties. The work [32] generates scale-free NoC based on the Barabasi-Albert (BA) model [27] without constraints on switch size. The BA model can only generate a scale-free network of fixed degree distribution exponent (≈ 3). The growth models including BA model for scale-free networks have been extensively studied in network science. At every timestep, a new node with several links is added to the initial network which has a small number of nodes. Huge degree nodes (high-radix switches) impose unacceptable costs due to the power and area of the switch increase superlinearly with its size. To improve the applicability of scale-free topology for peer-to-peer networks, Hasan Guclu et al. [33] and Eyuphan Bulut et al. [34] constructed a limited scale-free network topology with the constraint of maximal node degree, which effectively improved the search efficiency of peer-to-peer networks, respectively. Unfortunately, in the previous scale-free topology generation methods, the wiring cost (link length) is ignored due to the lack of consideration for the length of links connecting nodes. The link length has a dominant effect on the overall performance and power consumption of

NoCs. Sourav Das et al. [35] also designed a 3D small-world NoC architecture based on Watts-Strogatz model according to traffic-driven power-law length distribution, but it is only applied to application-specific NoCs containing tens to hundreds of nodes, and its link length does not mathematically obey a power-law distribution. This classical Watts-Strogatz model [28] is built from an initial mesh topology and then every link is rewired with a probability to a randomly chosen node. The rewiring procedure establishes long-range links in the network, which dramatically lowers the average hop count of the topology. Furthermore, inspired by small-world cortical networks with sparse long-range connections [36], the rewiring of links according to the power-law distribution of link length could further lower the wiring cost associated with communications [37], [38], [35].

Mapping tasks on the topology to achieve low power consumption is another key step in NoC design. NoC mapping is an NP-hard problem [39]. In [40], a branch-and-bound algorithm was adopted for application mapping in a regular mesh-based NoC architecture, which minimized the total amount of power consumed in communications. Tosun et al. [41] presented a new integer linear programming (ILP) based application mapping tool for mesh-based NoCs. Wang et al. [42] proposed a metaheuristic algorithm called WOAGA for large-scale mesh-based NoC mapping to achieve low-energy consumption. However, these methods can be very time consuming when the number of tasks reaches several hundred. For neural network applications, Sawada et al. [13] developed a greedy-based algorithm to place tasks one by one on mesh-based TrueNorth based on the Manhattan distance between the current task and the tasks that have already been mapped, which is not suitable for complex task graphs and irregular topologies. A unified flow combining task scheduling and core mapping [43] is proposed to support regular meshes, irregular meshes, and custom NoCs, using mixed integer linear programming (MILP), then a partition-based speedup technique is proposed to accelerate this model, but it is not suitable for large-scale networks due to a non-polynomial complexity of the MILP problem. Another partition-based mapping approach [44] was proposed for large-scale NoCs. The near-convex region of topologies was selected one by one for each subset of cores obtained by min-cut partitioning on task communication graph. However, different from a mesh-like topology, the convex regions formed by adjacent cores are not densely connected regions in the brain-network-inspired topology. Efficient application mapping for the large-scale complex brain-network-inspired NoC topology is a key problem to be solved urgently in this paper.

The irregularity of the topology induced by the brain-network-inspired design makes packet routing quite complicated. Zhang et al. [45] presented a deterministic-path routing algorithm to tolerate many faults in large-scale NoCs. Kinsy et al. [46] developed a bandwidth-sensitive oblivious routing approach to produce application-aware deadlock-free routes. However, these packet routing algorithms did not consider the constraints of both bandwidth and hop count.

In this article, we propose to synthesize efficient brain-network-inspired interconnections for large-scale NoCs, con-

sidering switch size, link length, and power consumption. Different from the conference version [12], this article proposes the topology generation method takes into account the link length constraints to avoid high transmission delays, and further uses a detailed cycle-accurate simulator *BookSim2* under synthetic traffic patterns and extends *BookSim2* to support simulation with specific applications, to evaluate the performance of the brain-network-inspired NoC and the effectiveness of the proposed mapping method. The key technical contributions of this work are listed as follows.

- We propose a method to generate a large-scale brain-network-inspired NoC topology with limited scale-free and small-world power-law properties, which has a low average hop count approximately proportional to the logarithm of network size. Then, a modified Louvain algorithm is performed to extract communities of the brain-network-inspired topologies to realize modularity.
- Considering the communication requirements of different applications and community structure of the topology, we propose an application mapping method, including task mapping based on the modularity of the brain-network-inspired topologies and Lagrangian relaxation-based deterministic deadlock-free routing scheme, to minimize the communication power consumption and hop count for routing.
- Experiments with *BookSim2* show that the generated brain-network-inspired topologies have significantly lower latency and power consumption under many synthetic traffic patterns compared to other previous topologies. For large-scale applications, the resulting NoC designs show better performance, especially in graph processing, with up to 70% lower average hop count and 75% lower average latency than mesh-based NoCs.

In the remainder of this paper, Section II shows an overview. Section III~IV present the topology generation and application mapping of the brain-network-inspired interconnections for large-scale NoCs, respectively. Section V lists experiments, followed by a conclusion in Section VI.

II. OVERVIEW

In this work, the NoC architectures are assumed to support packet-switched communications with source routing and wormhole flow control, and we choose a switch architecture similar to the input-queued switch architecture [47] with a four-stage pipeline for packet header flits. Each core is connected to a switch, and we focus on the network topology between switches, where each node represents a switch.

In our design, we first propose to generate the brain-network-inspired interconnection topology with a low average hop count approximately proportional to the logarithm of network size for large-scale NoCs, then propose to address the large-scale application mapping problem for this brain-network-inspired NoCs. Figure 1 shows the design flow. In the first stage, given power-law distributions, a deterministic growth algorithm is proposed to construct the brain-network-inspired topology with limited scale-free and

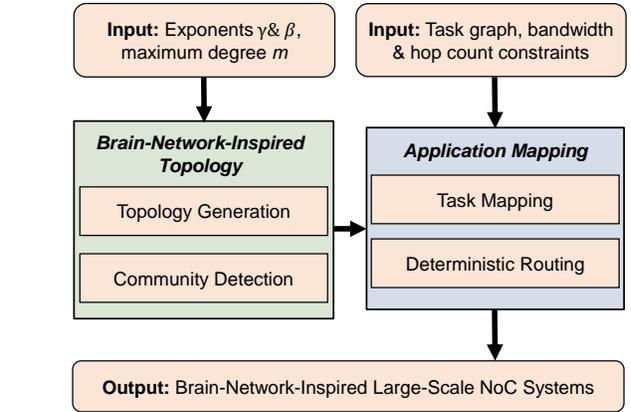


Fig. 1. Design flow.

small-world power-law properties. To obtain a proper brain-network-inspired topology, we evaluate the communication-independent basic power consumption and communication cost of all topologies generated with different power-law distributions of node degree and link length and make a tradeoff. Then, a modified Louvain algorithm is performed to extract communities of the brain-network-inspired topologies to realize modularity. In task mapping of the second stage, given the specific communication requirements of the application, we exploit the modularity of the brain-network-inspired topologies to solve the difficulty in large-scale task mapping. We first propose a k -way partition and simulated annealing based heuristic method to assign the tasks with heavy traffics to the same community in the topology, and then present a detailed task placement method to place each task to a specific core one by one. In the deterministic routing of the second stage, given the constraints of hop count and bandwidth, we develop an application-specific Lagrangian relaxation-based deadlock-free routing scheme on the brain-network-inspired NoC, which statically determines routes for all flows. A detailed cycle-accurate simulator, *BookSim2* [47], is applied to measure latency, power consumption, and hop count metrics that aid a quantitative, well-informed comparison between multiple NoC systems. We extend *BookSim2* to simulate communication architectures with specific applications according to the solution of application mapping. For convenience, key notations used in this paper are listed in Table I.

III. GENERATING A BRAIN-NETWORK-INSPIRED TOPOLOGIES FOR LARGE-SCALE NOCS

A. Topology Generation

Problem statement: Given network size n , maximal switch size constraint m , and maximal link length constraint l_a , we attempt to generate a brain-network-inspired topology $G_s(S, E_s)$ with the properties of limited scale-free and power-law small-world for large-scale NoCs, which has low power consumption and low average hop count between any two nodes approximately proportional to the logarithm of the network size.

In this work, we propose a deterministic growth algorithm by introducing switch size and link length constraints, which is

TABLE I
KEY NOTATIONS USED IN THIS PAPER.

γ	Exponent of power-law distribution of node degree, and $\gamma > 0$
β	Exponent of power-law distribution of link length, and $\beta > 0$
i	Node degree, and $k \leq i \leq m_a$
m	User-defined maximal switch size, and $m > 2k$
m_a	Actual maximal node degree, and $2k < m_a \leq m$
k	Initial node degree, and $k \geq 2$
l_a	User-defined maximal link length
l	Link length, and $0 < l \leq l_a \leq 2(t-1)$
n	Network size, and $t * t = n$
$G_s(S, E_s)$	Brain-network-inspired topology in which each vertex $s_u \in S$ represents a core/switch ($ S = n$), each edge $(s_u, s_v) \in E_s$ represents a link from core/switch s_u to s_v , and the length of link (s_u, s_v) is given by ω_{uv} .
$G_t(T, E_t)$	Task graph in which each vertex $t_u \in T$ represents a task and each edge $(t_u, t_v) \in E_t$ with the weight cr_{uv} represents the communication requirement from task t_u to t_v .
$G_c(C, E_c)$	Core communication graph in which each vertex $c_u \in C$ represents a core/switch and each edge $(c_u, c_v) \in E_c$ with the weight fl_{uv} represents the communication requirement from core/switch c_u to c_v .

different from the semi-deterministic growth algorithm (SDA) [34], to generate a brain-network-inspired NoC topology with limited scale-free and power-law small-world properties, which has a low total link length, low power consumption, and low average hop count between any two nodes approximately proportional to the logarithm of the network size. Given different power-law distributions, the deterministic growth algorithm can generate different topologies. In order to select a proper topology, we evaluate the communication-independent basic power consumption and communication cost of the topology and make a tradeoff. Algorithm 1 shows the key steps of topology generation.

Limited scale-free means that the maximum node degree (switch size) of the network cannot be greater than the user-defined maximal switch size m and the node degree follows a power-law distribution $P(i) \propto i^{-\gamma}$ only if the node degree i is less than m . In addition, the authors [37], [38], [35] have shown that networks with a power-law distribution rather than a uniform distribution of link length can not only result in the small-world property, but also physical realizability and low total link length. Furthermore, while seeking a power-law distribution of node degree in the process of network growth, it is another pursuit of topology generation to realize the power-law distribution of link length, $P(l) \propto l^{-\beta}$, where l is link length. To avoid generating a very long link, which has extremely high transmission delay, there is a user-defined maximal link length l_a , and the power-law distribution of link length exists only if $l < l_a$. Given γ and β , our method generates a network topology deterministically by growth, so we call it deterministic growth algorithm. By varying γ and β , more topologies can be generated.

Power consumption of NoCs, including basic network power consumption and communication cost, is an important index in network topology design. Basic power consumption, including static power consumption and clocking power consumption, is communication-independent. In synchronous design, given the network topology, there is a certain basic power consumption.

To select a proper topology for large-scale NoCs, that is, select a set of γ and β from many combinations, we evaluate the basic power consumption and communication cost of all topologies. Due to the emergence of large-size switches and

long-range links that insert repeaters to reduce interconnect transmission delays, the basic power consumption of the brain-network-inspired topology would be greater than that of the conventional mesh, but due to the lower average hop count between nodes, the communication cost of this topology would be lower. Selecting smaller γ and β may reduce basic power due to fewer high-degree nodes and long-range links, but it would cause a bigger hop count and larger routing path length during communication, which increase communication cost. We vary γ and β by the step size of 0.1, and call the deterministic growth algorithm to generate a topology for each set of γ and β . Finally, we select a proper topology by a tradeoff between the basic power consumption and communication cost of topologies.

Basic power consumption is the sum of power consumed by all switches and physical links with repeaters. The power model [48] is used to estimate the basic (static and clocking) power consumption based on the degree of nodes (switch size) and the length of links. A detailed evaluation of the communication cost for each topology at the actual traffic can be very time-consuming. As a rough estimate, we assume that communication cost comes from communication between every two-node pairs. We make trade-offs between communication-independent basic power consumption and communication cost to get a proper topology with a maximum of *OBJ*, which can be expressed as

$$OBJ = \alpha \cdot \frac{C_{min}}{C_{\gamma\beta}} + (1 - \alpha) \cdot \frac{P_{min}}{P_{\gamma\beta}} \quad (1)$$

where $P_{\gamma\beta}$ and $C_{\gamma\beta}$ represent respectively basic power consumption and communication cost of the topology with a set of γ and β . Since a smaller hop count means less communication cost over switches, and shorter routing path length means less communication cost over physical links, we roughly estimate $C_{\gamma\beta}$ to be $\sum_u \sum_v L_{u,v} \cdot H_{u,v}$, where $H_{u,v}$ and $L_{u,v}$ are respectively the hop count and path length (the sum of the Manhattan distance of links) of the minimum hop path between every two-node pair (s_u, s_v) , $\forall s_u, s_v \in S$. The parameter α is normally set to 0.5, when the basic power consumption of the generated topology is too large to exceed a threshold, such as 1.3 times of that of mesh, we will reduce α to adjust the relative weight until the basic power consumption

Algorithm 1 *Topology Generation*

Require: Network size n , maximal switch size constraint m , and maximal link length constraint l_a

Ensure: Construct a proper brain-network-inspired topology $G_s(S, E_s)$ with limited scale-free and small-world power-law properties

- 1: Create and initialize a set of topologies ST ;
 - 2: **for** $\gamma \leftarrow \gamma_{min}$ to γ_{max} **do**
 - 3: **for** $\beta \leftarrow \beta_{min}$ to β_{max} **do**
 - 4: Call **Deterministic_Growth_Algorithm**(n, m, l_a, γ, β) and obtain a resulting topology $G_{\gamma\beta}$;
 - 5: Calculate $C_{\gamma\beta}$ and $P_{\gamma\beta}$ of $G_{\gamma\beta}$;
 - 6: Add $G_{\gamma\beta}$ to ST ;
 - 7: **end for**
 - 8: **end for**
 - 9: Select a proper topology $G_s(S, E_s)$ with maximal OBJ from ST according to Equation 1;
-

of the selected topology is below this threshold. Since the basic power consumption and the rough communication cost have different units of measurement, for more accurate assessment, C_{min} and P_{min} are respectively minimum communication cost and basic power consumption over all possible cases of topologies for the normalized process.

1) *Deterministic Growth Algorithm:* Similar to the growth algorithms of complex network models, our deterministic growth algorithm starts with an initial simple topology and adds new nodes in sequence from near to far from the partial network until all nodes have been added. Algorithm 2 shows the key steps of the deterministic growth algorithm. Indeed, in the growth process, the establishment of every link deterministically makes the topology tend to be scale-free and small-world. During the growth, we first keep the power-law distribution of node degrees of topologies to achieve the scale-free property as much as possible. In addition, links are established under the constraint of link length and tend to be power-law distributions of length.

In general, the initial small topology can be any small connected topology, and the form of the initial small topology has little influence on the power-law distributions of the final large-scale topologies. In this design, we employ a small mesh as the initial topology as shown in Figure 2.

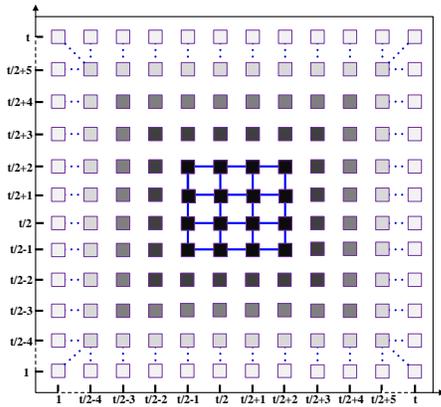


Fig. 2. On-chip floorplan with an initial mesh topology.

Initial Setup: The NoC design consists of a 2-D grid of $t \times t (= n)$ cores. We build a two-dimensional coordinate system on the plane of the chip, each core has a unique coordinate. The Manhattan distance of all possible links is within the range $[1, 2t - 2]$. The degree of all nodes is within $[k, m]$. The interconnection starts with a small-scale topology

consists of black cores and blue edges at the center of the chip plane.

Growth Strategy: During the growth process, each remaining new node is added orderly by connecting k different nodes of the partial topology, and these k nodes of the partial topology are determined one by one for the new node, while ensuring the expected power-law distributions for node degree and link length. Except for the nodes of the initial topology, the remaining new nodes are connected to the network through k links, and the nodes of the initial topology only account for a small proportion of all nodes. The initial degree of new nodes is k and each newly established bidirectional link will increase the total degree by 2, so the average degree of all nodes in the final network topology is almost $2k$. In Line 6-14, we first determine the expected degree of the node of the partial topology to connect the new node, according to the deviation of the power-law distribution of degrees between before and after connecting the new node to a node with each possible degree, and these nodes with the expected degree are considered as candidates. When the new node connects a node with degree u of the partial topology, it can make the node degree distribution closer to the power law, that is, there is a smaller deviation from the ideal power-law distribution, then u is called the expected degree.

According to [34], the average degree of all nodes is assumed to be $2k$ in the topology, and m_a is the actual maximal node degree, and node degree has a power-law degree distribution $P(i) \propto i^{-\gamma}$, $k \leq i < m_a \leq m$, so $m_a > 2k$ and the frequency f_i of nodes with degree- i derived can be written as

$$f_i = \frac{m_a - 2k}{i^\gamma \sum_{j=k}^{m_a-1} \frac{m_a-j}{j^\gamma}} \quad \text{for } k \leq i < m_a \quad (2)$$

$$f_{m_a} = 1 - \sum_{j=k}^{m_a-1} f_j \quad (3)$$

So given m, k , and γ , we can obtain the expected degree distribution. In addition, in order for all frequencies f_i , $k \leq i \leq m_a$, to be positive, the following inequality must be satisfied [34]:

$$2k \cdot \sum_{j=k}^{m_a-1} i^{-\gamma} \geq \sum_{j=k}^{m_a-1} i^{-\gamma+1} \quad (4)$$

The initial value of m_a equals m , when this inequality is not met, we reduce m_a until it is met. Hence, $m_a \leq m$, and the maximum node degree does not exceed the user-defined constraint of switch size.

Algorithm 2 *Deterministic_Growth_Algorithm*(n, m, l_a, γ, β)

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 $m_a = m$ ;
2: while the inequation 4 does not hold do
     $m_a - -$ ;
4: end while
   for degree  $i \leftarrow k$  to  $m_a$  do
6:   Calculate  $f_i, freq[i], n[i]$ , and  $score[i]$ ;
   end for
8: Construct an initial simple small topology in the center of the chip plane;
   for each new node  $NN$  that has not been yet connected to the topology in sequence from near to far from the partial topology do
10:  for  $lc \leftarrow 1$  to  $k$  for  $NN$  do
     $D_{min} = \infty, i_{exp} = 0$ ;
12:    /**To determine the desired degree of existing nodes for scale-free property.**/
    for degree  $i \leftarrow k$  to  $m_a$  do
14:      Calculate the difference of absolute deviation  $D(i)$  according to Equation 6;
      if  $D_{min} > D(i)$  &&  $n[i] \neq 0$  then
16:         $D_{min} = D(i), i_{exp} = i$ ;
      end if
18:    end for
     $DI_{max} = 0, N_{dir} = 0$ ;
20:    for each node  $EXN$  of the partial topology do
      if the degree of  $EXN$  equals  $i_{exp}$  && no existing link between the these two nodes then
22:        /**Establish a new link to satisfy link distribution of power-law small-world property.**/
        Calculate the Manhattan distance  $l$  between  $NN$  and  $EXN$ ;
24:        if  $l > l_a$  then
          Continue;
26:        end if
        Calculate the deviation  $DI(l) = P_{expected}(l) - P_{actual}(l)$ ;
28:        if  $DI_{max} < DI(l)$  then
           $DI_{max} = DI(l), N_{dir} = EXN$ ;
30:        end if
      end for
32:    end for
    Update  $freq[i], n[i]$ , and  $score[i]$ ;
34:    Connect  $NN$  to  $N_{dir}$  by a new link;
   end for
36: end for

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The next step is to determine what degree of nodes to connect to minimize the deviation of the resulting degree distribution from the expected power-law degree distribution. The deviation of degree- i nodes' expected count and current count in the topology is shown as

$$d(i) = n[i] - score[i] - freq[i] \quad (5)$$

where $n[i]$ and $score[i]$ denote the current node count and expected count of degree- i at a given node count, respectively, and $freq[i] = f_i/k$ is the expected increment in degree- i node count with only one edge addition to a new node. When connecting to the node with degree- i , the deviation of degree- i and degree- $(i+1)$ varies. Consequently, the total difference of absolute deviation of all degrees, between before and after connecting to the degree- i node, can be computed as

$$D(i) = (|d(i+1) + 1| + |d(i) - 1|) - (|d(i+1)| + |d(i)|) \quad (6)$$

The total difference may be negative, and the smaller the value, the smaller the overall deviation. Therefore, if the new node connects the degree- i_{exp} node with the smallest total difference, then i_{exp} is the expected degree, and connecting the node with degree- i_{exp} can adhere the power-law distribution of node degree as much as possible. Note that when there is only one node with expected degree in the partial topology, we connect the new node to this node directly. But it is more likely to have a batch of candidates that satisfy this term.

Subsequently, in Line 16-25, only one node of candidates is selected to connect the new node according to the deviation

between the expected and the actual distribution of link length. To further satisfy a power-law distribution of link length, we select one of these candidates whose length to this new node has the maximum deviation between the expected count and current actual count.

The expected probability of link length can be expressed as

$$P(l) = \begin{cases} \frac{l^{-\beta}}{\sum_{L=1}^{l_a-1} L^{-\beta}} & , 1 \leq l \leq l_a - 1 \\ 1 - \sum_{L=1}^{l_a-1} P(L) & , l = l_a \end{cases} \quad (7)$$

where l is computed by the Manhattan distance from the new node to the target node in the coordinate depends on the mainstream metal Manhattan routing (i.e., only allow horizontal and vertical connections). To constrain the length of links ($l \leq l_a$) and preserve the proportion of long links, we set the expected probability of link length l_a to the probability of links whose length is not less than l_a when there is no length constraint, $P(l_a) = 1 - \sum_{L=1}^{l_a-1} P(L)$. If there are still multiple nodes satisfying both degree and link length conditions, the existing node with the minimum coordinate is finally selected.

Finally, the new node is greedily and deterministically connected to a node of the partial topology, which makes the network topology most adherent to the limited scale-free and small-world power-law properties. Note that the k nodes connected to each new node must be different, and when connecting an existing node to the current new node, we make sure that there are no existing links between the current new

node and the existing node. Repeat the above steps until all nodes are added to the network, and finally we obtain a brain-network-inspired topology.

Example: Figure 3 illustrates the process of this method. Nodes $A \sim P$ and the blue edges form an initial topology, and the remaining new nodes $[1, 1] \sim [6, 6]$ are added to the network one by one in order. Each new node connects 2 nodes of the partial topology initially. Node $[1, 1]$ is added first, at this point, $D(2)$, $D(3)$, and $D(4)$ are respectively 2.0, 0, and -2.0, so F , G , J , and K with degree 4 can be selected as candidates. The Manhattan distance from node $[1, 1]$ to F , G , J , and K are 4, 5, 5, and 6, respectively. The deviation between the expected count and current actual count of link with length 4 is the largest, so node $[1, 1]$ is connected to F as shown in Figure 3(a). Then the second node of the partial topology will be selected for node $[1, 1]$, and $D(2)$, $D(3)$, and $D(4)$ are respectively 2.0, 0, and -0.6, so node G , J , and K with degree 4 can be selected as candidates. The deviation between the expected count and current actual count of link with length 5 is the largest, so node $[1, 1]$ is connected to G as shown in Figure 3(b). In the same way, we establish two links for node $[1, 2]$ in Figure 3(c) and node $[1, 3]$ in Figure 3(d), respectively. Repeating the same process until the topology is generated for all remaining nodes.

B. Community Detection

Communities are sets of highly interconnected nodes in networks, and the nodes within different communities are only sparsely connected. A fast greedy Louvain algorithm [49] is the most popular method to detect the modularity of complex networks and does not change the topology structure. In this stage, to avoid oversized communities, which will degrade the usefulness of partition, we modify Louvain algorithm [49] to detect communities of the brain-network-inspired topology by introducing a community size constraint. $G_s(S, E_s)$ is the input, but the weight of each edge is given by $1/\omega_{uv}$.

Louvain algorithm is an iterative method in which modularity, which measures the density of links inside communities as compared to links between communities and has been used to compare the quality of the partitions [49], is the optimization objective. Each community initially includes a node of the topology. In each iteration, each community is assumed to be in turn merged into its neighboring communities, and then the community is merged into the neighboring community with the largest modularity gain. Ultimately, modularity does not increase, and each community detected contains tightly connected nodes in the topology. To avoid oversized communities, in iterations, if a community is merged with one of its neighboring community and the overall size is greater than TD , this case would be ruled out. However, limiting the community size can result in a decrease in modularity and partition quality. Therefore, when setting TD for topologies of different sizes, it is necessary to ensure that the modularity of community detection cannot be significantly reduced.

Examples of community detection for brain-network-inspired topologies with 4096 nodes and 6400 nodes are shown in Figure 4. The modularity of the partition is a scalar value

between -1 and 1. For these two topologies, after the Louvain algorithm is executed, the topology will be divided into several communities and even some communities have 300 to 500 nodes. When TD is as low as 150, the modularity does not decrease significantly, otherwise it will degrade the partition quality.

Finally, all vertices $s_u \in S$ are divided into several communities by the modified Louvain algorithm, and we obtain the set of communities $CM = \{cm_x | \sum_x |cm_x| = |S| \wedge |cm_x| \leq TD, x = 1, 2, \dots, N_M\}$ and the number of communities N_M .

Within the framework of network science, high-degree nodes that are positioned to make strong contributions to global brain network function are generally referred to as hubs [50], [51], [52]. We regard that these hubs act as key feature nodes and reflect the location of all nodes in their communities, which will play an important role in the subsequent application mapping process. We adopt the basis of hub classification [50], [51], [52] based on the network's community structure in brain network research. To classify hubs for each community, each node's participation index P [50], [52] which expresses its distribution of inter- versus intra-community connections is calculated. P of node s_u is defined as

$$P_{s_u} = 1 - \sum_{s=1}^{N_M} \left(\frac{\kappa_{ux}}{i_u} \right)^2 \quad (8)$$

where N_M is the number of identified communities, i_u is the degree of node s_u , and κ_{ux} is the number of edges from node s_u to nodes within community cm_x . Smaller P means that the more edges of the node are connected to nodes in the same community. In the study of brain networks, when participation coefficient $P < 0.3$, high-degree nodes (at least one standard deviation above the network mean) are defined as provincial hubs which have the vast majority of links within their module [50], [52]. Therefore, in each community, we classify high-degree nodes according to this criterion as hubs. If there are no nodes in the community that meet the above conditions, we select the three nodes with the highest degree as hubs in this community. We define the set of hubs in community cm_x as $HB_x = \{hb_1, hb_2, \dots\}$, $x = 1, 2, \dots, N_M$.

C. Complexity Analysis

In summary, topology generation has running time $O(|S|^2 + |S| + |E|)$ ($= O(|S|^2)$), where $|S|$ is the number of nodes, and $|E|$ denotes the total number of edges in the brain-network-inspired topology. Meanwhile, the complexity of community detection [49] and hub classification [50] for complex topologies has been proved within $O(|S| + |E|)$.

IV. APPLICATION MAPPING

A. Task Mapping

Problem statement: Given a task graph $G_t(T, E_t)$ and a large-scale brain-network-inspired topology $G_s(S, E_s)$, we attempt to map all $|T|$ tasks to the cores of this topology and ensure low communication power and low communication hop count.

Drawing on the modularity of the brain complex network, we exploit community structures to improve the solution

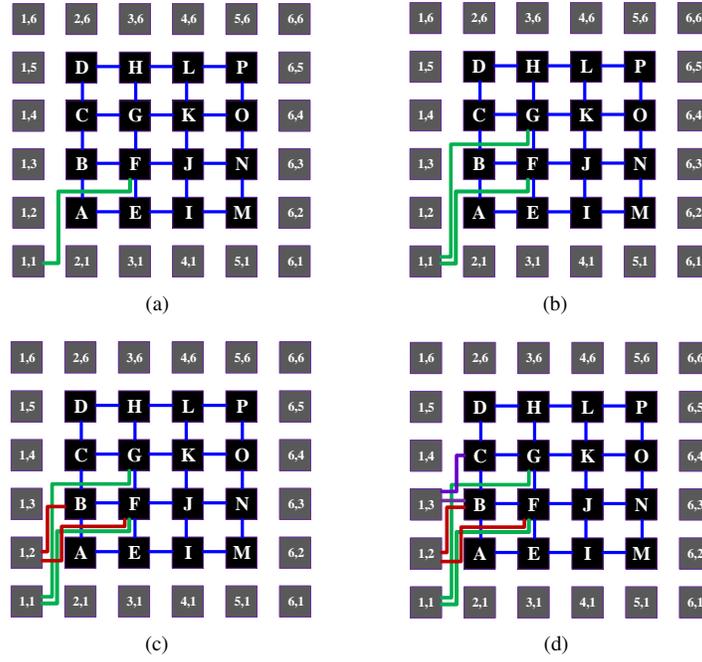


Fig. 3. An example of deterministic growth algorithm.

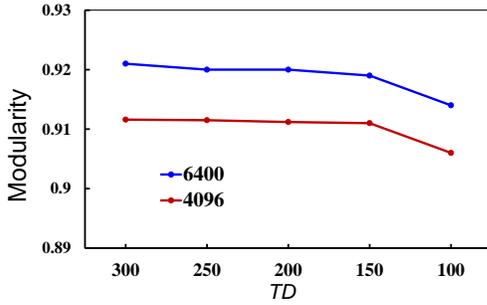


Fig. 4. The modularity w.r.t. TD .

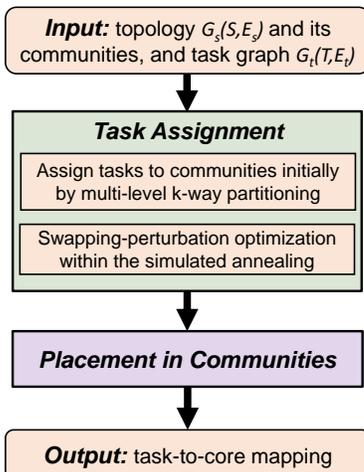


Fig. 5. Flow of task mapping.

quality in large-scale task mapping. The detailed flow is shown in Figure 5. The brain-network-inspired topology has been decomposed into several communities of densely interconnected nodes in the community detection stage. We first propose a k -way partition and simulated annealing based heuristic method to assign the tasks with heavy traffics to the same community in the topology. Then, according to the tasks-to-community assignment, we present a detailed task placement method to place each task to a specific core one by one. The hubs of the community to which unmapped tasks are assigned are introduced to evaluate the communication cost between the current task and the unmapped tasks, to further improve the quality of the mapping.

1) *Task Assignment*: Firstly, according to the task graph $G_t(T, E_t)$, we perform the multilevel k -way partitioning algorithm to initially assign tasks into N_M communities. If the given number of tasks is less than n , we add some spare tasks without traffic into the graph. To ensure that the number of tasks matches the size of each community, the community detection results including the number and size of each community are used as the inputs of partitioning. We define N_M subsets of tasks as sub_x , and ensure $|sub_x| = |cm_x|, x = 1, 2, \dots, N_M$.

Furthermore, a perturbation method within the simulated annealing is to randomly choose two tasks in two different communities, swap them, and create a new partitioning for exploring a superior task-to-community assignment solution. According to [35], $o = (r \cdot h + d) \cdot cr$ is used to roughly evaluate the communication cost of each flow, where r denotes the number of switch stages, h is the hop count of each flow, and d is the Manhattan distance between the source node and sink node of each flow. Low o means low communication hop count and power consumption. Since the specific location

of tasks is not determined, to obtain a superior partitioning solution, during the partitioning process the hubs in each unmapped community are regarded to integrate the external communication requirements of tasks within this community. We define O as the communication cost to evaluate the quality of task partitioning. The objective can be expressed as follows:

$$\begin{aligned} \text{Minimize } O = & \\ \sum_x (r \cdot h_x + d_x) \cdot cr_x + \varphi \cdot \sum_x \sum_{y, y > x} (r \cdot h_{xy} + d_{xy}) \cdot cr_{xy} & \end{aligned} \quad (9)$$

where h_x and d_x are average hop count and average Manhattan distance every two cores within community cm_x , respectively, cr_x is total communication requirements within community cm_x , h_{xy} and d_{xy} are average hop count and average Manhattan distance every two hubs between community cm_x and cm_y , and cr_{xy} represents communication requirements between these two community. A penalty factor $\varphi (> 1)$ of costs between communities allows source-sink pairs to be placed within the same community as much as possible. After this stage, all tasks are initially assigned into communities.

2) *Placement in Communities*: According to the tasks-to-community assignment, a detailed task placement method is proposed to place each task one by one into a specific core of the community to which it is assigned. We adopt a greedy strategy to place tasks on the core with the least communication cost, and we use the hubs, which play a global key role in topology, to evaluate the communication cost between the current task and the unmapped tasks to further improve the quality of the mapping.

The task with the largest amount of communication is processed first, and it is placed on the hub node with the largest degree in the community to which it has been assigned. Subsequently, every time an unprocessed task that communicates the most with the processed tasks is selected for the next mapping. To minimize the communication cost, the task is placed on each unoccupied available core of the community to which it is assigned, and the communication cost is calculated, the task is placed on the core with the lowest communication cost. In particular, for some tasks that are not placed to the specific cores but do communicate with the task being processed, the communication cost between the current task and the unmapped tasks cannot be calculated, but it affects the quality of the placement. Note that for the sake of more accurate placement, the hubs in the community where the unprocessed tasks are allocated assume all its traffics, that is, simply place the task on these hubs.

During the detailed task placement, if there is currently maximum traffics between task t_u and the tasks that has been placed, and t_u is assigned to community cm_x , we will try to place t_u on each core $s_a \in cm_x$ and then calculate the communication cost $cost_{uv}^{s_a}$ of all flows in $G_t(T, E_t)$. The

objective can be expressed as

$$\text{Minimize } \sum_{t_v: (t_u, t_v) \text{ or } (t_v, t_u) \in E_t} cost_{uv}^{s_a} \quad (10a)$$

$$cost_{uv}^{s_a} = \begin{cases} (r \cdot h_{ab} + d_{ab}) \cdot cr_{uv}, & \text{if } t_v \text{ has been placed;} \\ (r \cdot H_{ax} + D_{ax}) \cdot cr_{uv}. & \text{otherwise.} \end{cases} \quad (10b)$$

where cr_{uv} is the communication requirement of flow (t_u, t_v) in E_t , if t_v has been placed in core s_b , h_{ab} and d_{ab} are respectively the hop count and Manhattan distance between core s_a and s_b . Otherwise, H_{ax} and D_{ax} indicate respectively the average hop count and average Manhattan distance between core s_a and all hubs hb_z of the community cm_x where c_b is assigned, respectively. The preliminary routing flow paths are allocated by Dijkstra's shortest-path algorithm. If there is a minimum communication cost when t_u is placed on s_a , s_a is marked as unavailable. Repeat until all tasks are processed.

Finally, according to the task-to-core mapping solution, we construct a core communication graph G_c : $G(C, E_c)$ is a directed graph, where $C = \{c_x | 1 \leq x \leq |S|, c_x \text{ represents a core or switch}\}$, and $E_c = \{(c_x, c_y) | \text{there is a traffic flow } (c_x, c_y) \in E_c \text{ for each flow } (t_u, t_v) \in E_t \text{ if task } t_u \text{ and } t_v \text{ are respectively assigned to core } s_x \text{ and } s_y\}$.

B. Deterministic Routing

Problem statement: Given a core communication graph $G_c(C, E_c)$ and a brain-network-inspired topology $G_s(S, E_s)$, we attempt to route all $|E_c|$ flows with minimization of the power consumption and hop count under the following constraints:

- the *hop count* constraint LC^{xy} for each communication flow $(c_x, c_y) \in G_c(C, E_c)$,
- and the *bandwidth* constraint cr_{cap} for physical links of $G_s(S, E_s)$.

We propose a Lagrangian relaxation-based deadlock-free routing algorithm to generate deterministic routing tables of-line. The routing problem as a multicommodity flow problem is an NP-hard problem [53], in which all individual commodities share a common facility. Therefore, to find a high-quality solution, rather than decomposing it into independent single-commodity flow problems to allocate routing paths one by one, it is more preferable to coordinate all communication flows to do path allocation [53].

With wormhole flow control, deadlocks can happen during routing of packets due to cyclic dependencies of resources (such as buffers) [16], [54]. Given a network topology, we preprocess to break such cyclic dependencies by prohibiting certain turns to guarantee deadlock-free packet routing. We use the turn prohibition (TP) algorithm presented in [54], [55] to find the set of turns PTS that need to be prohibited to break cycles, and at most 1/3 of all turns would be prohibited. When allocating the routing path, the paths are not allowed to go through the turns prohibited in PTS .

For deadlock-free routing on the brain-network-inspired NoC, minimizing communication power consumption and hop count is the optimization goal. In $G_s(S, E_s)$, vertex $s_u \in S$

denotes a switch node and edge $(s_u, s_v) \in E_s$ represents a link that connects s_u to s_v . Let t_{uv}^{xy} and p_{uv}^{xy} represent flow (c_x, c_y) across (s_u, s_v) and its communication power, respectively. p_{uv}^{xy} is defined as

$$p_{uv}^{xy} = (J_{s_v} + J_{l_{uv}}) \cdot cr_{xy} \quad (11)$$

where cr_{xy} denotes the communication requirement of flow (c_x, c_y) , J_{s_v} and $J_{l_{uv}}$ point the energy consumed by the switch s_v and link (s_u, s_v) for sending one bit of data, respectively. Communication hop count is introduced into the objective function as a penalty. ξ is a constant as the hop penalty factor for each link. Then, the routing path allocation problem can be modeled as an ILP formulation:

$$\text{Minimize} \quad \sum_{(c_x, c_y) \in E_c} \sum_{(s_u, s_v) \in E_s} (p_{uv}^{xy} + \xi) \cdot t_{uv}^{xy} \quad (12a)$$

s.t.

$$\text{Unit flows:} \quad \sum_{s_v: (s_u, s_v) \in E_s} t_{uv}^{xy} - \sum_{s_v: (s_v, s_u) \in E_s} t_{uv}^{xy} = \begin{cases} 1 & \text{if } s_u = s_k; \\ 0 & \text{if } s_u \in S - (s_k, d_k); \\ -1 & \text{if } s_u = d_k; \end{cases} \quad (12b)$$

Hop count constraints:

$$\sum_{(s_u, s_v) \in E_s} t_{uv}^{xy} \leq LC^{xy}, \quad \forall (c_x, c_y) \in E_c; \quad (12c)$$

Bandwidth constraints:

$$\sum_{(c_x, c_y) \in E_c} cr_{uv}^{xy} \cdot t_{uv}^{xy} \leq cr_{cap}, \quad \forall (s_u, s_v) \in E_s; \quad (12d)$$

$$t_{uv}^{xy} = 0 \text{ or } 1. \quad (12e)$$

For large-scale flows, the ILP based method is very time-consuming. We propose a Lagrangian relaxation-based method to solve the multi-commodity flow problem. Lagrangian relaxation is a solution technique that incorporates hard constraints of bandwidth and hop count into the objective using Lagrange multipliers and punishes the objective if they are not satisfied. The original problem is transformed to the Lagrangian subproblem:

$$\text{Min} \quad \sum_{(c_x, c_y) \in E_c} \sum_{(s_u, s_v) \in E_s} (p_{uv}^{xy} + \xi + \mu_{uv} \cdot cr_{uv}^{xy} + \mu^{xy}) \cdot t_{uv}^{xy} - \sum_{(s_u, s_v) \in E_s} \mu_{uv} \cdot cr_{cap} - \sum_{(c_x, c_y) \in E_c} \mu^{xy} \cdot LC^{xy} \quad (13a)$$

$$\text{s.t.} \quad (12b) \text{ and } (12e). \quad (13b)$$

Since none of the constraints in this problem contains the flow variables for more than one of the commodities, the problem decomposes into separate least-cost path problems, one for each commodity. The problems are done by applying Dijkstra's shortest path algorithm [53], and only those paths that have turns not prohibited by *PTS* can be selected. Then we solve the Lagrangian multiplier problem by using subgradient optimization [16].

C. Complexity Analysis

Task mapping can be done in $O(N_M \cdot \log N_M + |S|^2 / N_M + (|E| + |S| \cdot \log |S|))$ ($= O(|S|^2 + |E|)$), where N_M represents the number of communities (parts) acquired at the community detection stage. The TP algorithm has been proven to be able to complete in $O(|S|^2 \cdot m_a)$ [54]. The time complexity of counting the shortest routing path of $|E_c|$ flows in $G_c(C, E_c)$ is $O(|E_c| \cdot [|E| + |S| \cdot \log |S|])$.

V. EXPERIMENTS

The proposed synthesis method has been implemented in the C++ language and run on a Linux 64-bit workstation with Intel 2.0 GHz CPU and 64 GB memory. We first verify the performance of the brain-network-inspired topology generated by the proposed method, i.e. the average hop count, power consumption, etc., and then verify the application mapping method with large-scale applications including real-world communication networks and synthetic applications. We use conventional mesh and torus as well as some irregular large-scale topologies for comparison experiments. Since the average node degree of large-scale mesh topology is around 4, for a fair comparison, we assume that both of them use the same average degree of switches, that is, the same total number of links, and the initial degree of each new node k is 2 and two new physical links are established.

A. Experimental Setup

1) *Configuration of Our Model*: In the experiments, we set the operating frequency at 1 GHz and the data width for the NoC links (flit size) as 32 bits. The switches for this validation have 2 virtual channels (VCs) on each port. Each virtual channel can hold up to 4 flits. The power model [48] is used to estimate the power dissipation of the switches and physical links under 32-nm technology, whose technology parameters were extracted from the process model of the International Technology Roadmap for Semiconductors (ITRS) [56]. We use the model [48] to search for the optimal (size and number of) repeaters for each link and to calculate the power consumption.

2) *Testcase*.: Two real-world communication networks and synthetic applications are used to evaluate the proposed application mapping method. A real large network dataset collection [57] is provided by Stanford for large-scale graph processing. A network with ground-truth communities, *email-Eu-core*, and Internet network, *p2p-Gnutella08*, are used in the performance evaluation of NoC designs. For graph processing in NoC-based distributed systems, such as in-memory computing architectures [9], [10], [11], the large-scale graph data is mapped to (stored in) many cores (vaults), iterating the vertices or edges of the graph in the current vault may require access to its adjacent vertices or edges in other vaults. Then application traffic is extracted from memory access dependencies between vaults caused by the scatter-gather operation [58]. Benchmark *G_3700* & *G_4096* are constructed by combining the task graphs generated by Task Graphs For Free [16]. The NoC architecture can also solve the interconnection communication between neurosynaptic cores as the basic processors. *VGG16*'s first two fully connected

layers [59] is abstracted as a benchmark *VGG16*, where network pruning is first performed to remove the trivial connections between neurons, and these synapses are partitioned into several fixed-size clusters. Between each partition, the number of connections translates into communication requirements. In addition, the article [5] provides benchmarks containing 30 to 70 tasks. We merge all benchmarks and repeat them 20 times to form a large-scale case (*D_3980*) with relatively local communication, which is different from the above global communication cases. Table II shows the detailed parameters of these benchmarks. Besides, Max-BW and Min-BW are the maximum and minimum communication requirements, respectively.

TABLE II
THE DETAILED PARAMETERS OF ALL BENCHMARKS.

Benchmarks	Task count	Flow count	Max-BW	Min-BW
<i>G_3700</i>	3,700	6,301	100	10
<i>G_4096</i>	4,096	7,108	100	10
<i>D_3980</i>	3,980	5,300	300	2
<i>VGG16</i>	4,096	10,308	64	2
<i>email-Eu-core</i>	1,005	25,571	15	1
<i>p2p-Gnutella08</i>	6,301	20,777	30	1

3) *Simulation Configuration of BookSim2*: A detailed and flexible cycle-accurate simulator *BookSim2* [47] is used to verify communication architecture performance, and it has been integrated with the power model [48] to calculate the total network power consumption. *BookSim2* features a modular design and offers a set of configurable network parameters in terms of topology, routing algorithm, flow control, and switch microarchitecture. Two extra routing algorithms, bandwidth-sensitive oblivious routing algorithm (*BSOR*) [46] and Lagrangian relaxation-based routing algorithm are also introduced into the tool. We set all LC_k and all f_{cap}^{ij} to 12 and $4000MB/s$, respectively.

We present a detailed evaluation of brain-network-inspired topology (BNIT), torus, and mesh for power and performance using four synthetic traffic patterns [1], [47], including uniform, shuffle, bitcomp, and randperm. The simulator's cycle time is a flit cycle, and the injection rate is specified in average packets per flit cycle per node. However, it does not provide a way to simulate a real application. To further verify routing algorithms and the performance of these communication architectures of which tasks have been mapped into cores, we operate a new customizable traffic pattern by mapping its communication graph into a customized deterministic table-based traffic. We transform the communication requirement cr_{xy} (MB/s) of flow $(r_x, r_y) \in G_r(R, E_r)$ into the packet injection rate $inject_rate_{xy} \in (0 \sim 1)$ of that. $packet_size$ denotes the number of flits per packet. The packet injection rate is expressed by

$$inject_rate_{xy} = \frac{cr_{xy}}{cr_{cap} \cdot packet_size} \quad (14)$$

Such table-based traffic allows specifying the source and destination pairs of packets along with the packet injection rate of each flow.

The complete list of configuration parameters used in the setup is summarized in Table III. In the synthetic traffic pattern and the application simulation, the packet size is 5 and 10 flits, respectively. More specifically, the transmission delays of each pipeline stage of switches and physical links are directly configured in the simulator. As technology scales, global link delays due to wiring parasitics tend to dominate over gate delays in VLSI, which may make long-range links in NoC severely constrained by the link delay. When repeaters are judiciously employed, the delay of transmitting signals on the global link can be reduced effectively by more than an order of magnitude [56], [60]. In our model, we assume that the distance between the adjacent switches is 0.1 mm . The delay (in ns) of physical links is extracted using RC delay models from [48].

B. Topology Analysis

1) *Effect of γ and β* : An example with $n = 4096$ (same with TrueNorth [8]), $l_a = 15$, and $m = 15$ is presented. We vary respectively β from 1.0 to 3.0 and γ from 0.5 to 2.5, including those that occur most frequently in brain networks [61]. In addition, to satisfy the inequality 4, the value of m_a is shown in Table IV. Figure 6 shows the *OBJ* value (equation 1) of BNIT generated by the proposed method for each γ and β . We can see that when $\gamma = 0.7$ and $\beta = 1.4$, the *OBJ* has the maximum value, and a proper network topology can be obtained and shown in Figure 7. In Figure 8, we show the degree distribution of BNIT constructed by our algorithm. The actual degree distributions perfectly match with the expected degree distributions with $\gamma = 0.7$. Based on the preferential implementation of the scale-free property, we further make the edge length distribution tend to the power-law small-world property. Figure 9 shows that the overall trend of the actual link length distribution and the expected link length distribution are close, even if there is a small deviation in some intervals.

Subsequently, each link of brain-network-inspired topology has a specific length, and the length should be guaranteed during topology metal routing. An existing method, bounded-length maze routing algorithm [62], can be used to solve the metal routing problem of this topology.

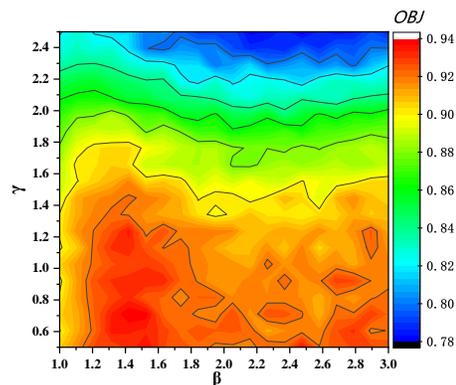


Fig. 6. Variation of *OBJ* w.r.t. exponent γ & β .

TABLE III
CONFIGURATION PARAMETERS FOR SIMULATION EVALUATION.

Configuration Parameter		Value
Network	Topology	BNIT & Torus & Mesh
	Synthetic Traffic	Uniform & Shuffle & Bitcomp & Randperm
	Operating Frequency	1 GHz
	Warm-up Period	30k cycles
	Simulation Period	100k cycles
	Packet Size	5 or 10 flits
	Flit Size	32 bits
Switch	Switch Type	Input-queued Architecture
	Flow Control	Wormhole
	Number of VCs per Port	2
	VC Buffer Size	4 flits
	Switch Pipeline Stages	4
VC Allocator/Switch Allocator/Routing Delay		1 cycle

TABLE IV
THE VALUE OF m_a WHEN γ IS VARIED FROM 0.5 TO 2.5 AND m IS 15.

γ	0.5 ~ 0.6	0.7 ~ 1.0	1.1 ~ 1.3	1.4 ~ 1.5	1.6	1.7	1.8	1.9	≥ 2.0
m_a	7	8	9	10	11	12	13	14	15

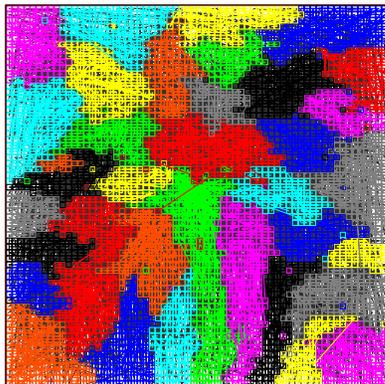


Fig. 7. Final topology of 4096 (64*64) nodes. For easy identification, the colors of the regions and links represent the communities to which they belong.

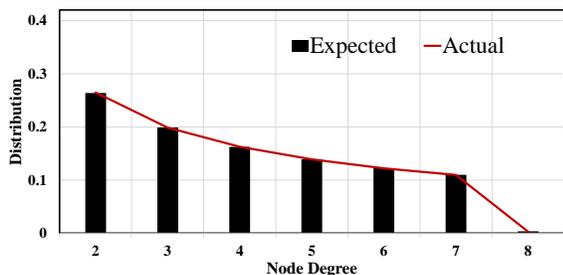


Fig. 8. Degree distribution of nodes of BNIT with $\gamma = 0.7$ and $n = 4096$.

2) *Effect of m and l_a* : m and l_a are respectively the user-defined maximal switch size and maximal link length. As shown in Table V, **#hop** is the average minimum hop count between every two nodes. P and C represent respectively the basic power consumption, including static power and clocking power, and rough communication cost. The total link length **#WL** is defined as the sum of the lengths of all links, and

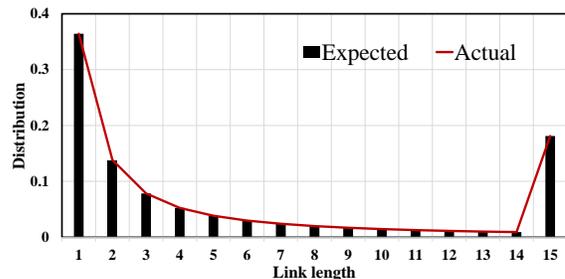


Fig. 9. Link length distribution of BNIT with $\beta = 1.4$ and $n = 4096$. The unit of link length is the distance between adjacent rows or columns in the coordinate.

the unit of length is the distance between adjacent rows or columns. When the topology generation is accompanied by larger m and l_a , the generated network topology may have lower average hop count.

TABLE V
DIFFERENT m AND l_a CORRESPOND TO THE PARAMETERS OF THE TOPOLOGY WITH 1024 NODES.

m	l_a	#hop	P	C	#WL
10	10	8.03	4.58	1.4E4	1233
10	15	7.33	4.65	1.4E4	1503
15	10	8.03	4.58	1.4E4	1233
15	15	7.33	4.65	1.4E4	1503
15	20	7.06	4.71	1.4E4	1754
15	30	6.96	4.82	1.7E4	2212

3) *Comparison with Conventional Regular Topologies and Irregular Topologies*: Compared to mesh, BNIT presents an extremely lower average hop count proportional to the logarithm of the network size (is called small-world), which Figure 10(a) confirms. Meanwhile, when the network size is greater than 100, the average hop count of BNIT is 35% to 90% lower than that of Mesh. When the network size is less than

100, although the two are very close, the average hop count of BNIT is still smaller than the mesh's. So BNIT generated by the proposed method is more suitable for networks with a size larger than 100.

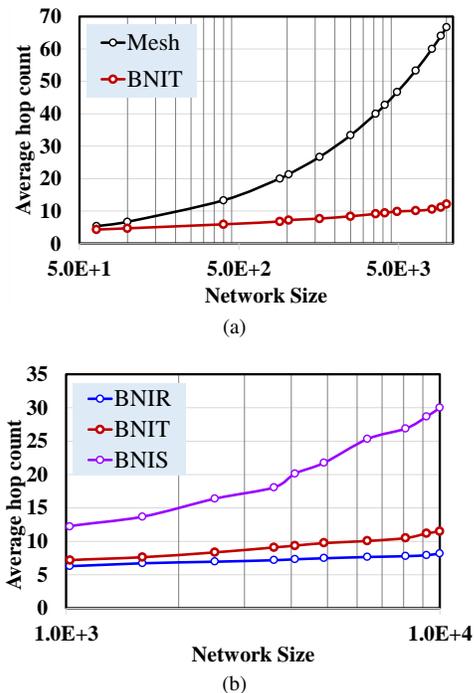


Fig. 10. Scaling of the average hop counts as a function of the network size. (a) The contrast between mesh and BNIT. (b) The contrast between BNIR, BNIT, and BNIS.

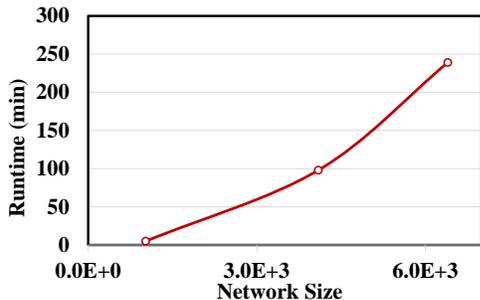


Fig. 11. Runtime of topology generation and community detection.

In Figure 10(b), legend BNIR and BNIS mean respectively that the random establishment without consideration of link length (SDA [34]) and the greedy selection of nodes with the shortest link length, rather than the pursuit of power-law distributions of link length in *Line 23 ~ 30* of Algorithm 2. Brain-network-inspired topologies with power-law length distribution (BNIT) have at least 50% lower average hop counts than BNIS. The advantage of BNIT's low average hop count will be highlighted as the network size increases. The average hop count of BNIR is slightly lower than that of BNIT. Figure 11 shows the runtime of the topology generation and community detection.

BA network based on growth and preferential attachment [33] is implemented to construct a scale-free peer-to-peer

network with fixed exponent γ . Here, we migrate this model to generate a scale-free BA topology for NoC. As shown in Table VI, the experimental results were derived from different-scale conventional regular topologies and irregular complex topologies, and n is set to 1024, 4096, 6400, and 9216, respectively. #link is the number of links of topologies.

Different from the mesh of $t \times t$, torus also has $2t$ long-range links across the plane in addition to short links of one unit length. The communication cost of torus is higher than that of mesh. This is because the routing path allocation is based on the minimum hop count, many node pairs would choose the path through the crossed long-range links to reduce the hop count between every two nodes, which results in greater communication cost.

Compared to mesh and torus, BNIT generated by the proposed method reduces the average hop count by about 80%, and reduces rough communication cost by about 70%, although the basic power is slightly increased by around 20%. As the network size increases, the average hop count of BNIT is getting lower and lower compared with mesh and torus. The number of links of all topologies is indistinguishable. Since the initial degree of the nodes in BNIS, BINR, and BNIT is the same, they have the same number of links. Compared with the topology (BNIR) generated by SDA, BNIT can reduce communication cost and basic power consumption by about 50% and 40%, respectively, and by employing only a small fraction of the long-range links, BNIT has approximately 85% lower the total link length. Compared with mesh, although the average hop count of BNIR is reduced by at least 70%, it will result in an even doubling of the basic power consumption and a 50-fold increase in the total link length. In addition, BNIR has fewer short-distance links, which may cause the communication between adjacent nodes to pass through some long-distance links. Therefore, compared with BNIT, it requires more power consumption in link transmission, which increases communication cost. Due to the lack of a proper amount of long-range links, BNIS has a higher average hop count and rough communication power consumption than BNIT, which is the same as shown in Figure 10(b). Despite the low average hop count and communication cost, the BA model [32] is not flexible, such as the fixed exponent in the power-law degree distribution, no switch size constraint (high-radix switches), and no link length perception (many long-range links), and the basic power consumption of the generated topology is even up to 3 times that of mesh. Therefore, this kind of inflexible generation of BA model is unaccommodated to NoC.

4) *Performance Validation under Different Traffic Patterns Using BookSim2*: Figure 12 shows the power evaluation for different-scale mesh, torus, and BNITs at four different traffic patterns using *BookSim2*. Label "×" indicates that communication congestion occurs in the network simulation. Power consumption covers basic power and communication power consumption, which includes *wire power*, *read&write power* of buffers, *crossbar power*, and others. With a low injection rate (0.0001 ~ 0.001), basic power consumption dominates the communication architecture, so the total power of BNIT is about 20% higher than others on account of some high-radix switches and long-range links.

TABLE VI
COMPARISON BETWEEN MESH, TORUS, AND BNIT WITH DIFFERENT NETWORK SIZES.

Topology	Metric	BNIT	BNIR (SDA)	BNIS	BA model	Torus	Mesh (base.)
1024	#hop	7.33 -66%	6.32 -70%	12.24 -43%	5.59 -73%	17.02 -20%	21.33 1
	<i>C</i>	1.4E4 -53%	3.0E4 0%	2.1E4 -30%	2.0E4 -30%	3.2E4 +7%	3.0E4 1
	<i>P</i>	4.65 +19%	6.05 +54%	4.49 +15%	8.02 +69%	4.03 +3%	3.92 1
	#link	2040 +3%	2040 +3%	2040 +3%	2040 +3%	2048 +3%	1984 1
	#WL	1503 ×3.8	7313 ×18.4	755 ×1.9	7048 ×18.0	794 ×2.0	397 1
4096	#hop	9.37 -78%	7.34 -83%	20.14 -53%	6.46 -85%	33.00 -23%	42.67 1
	<i>C</i>	5.4E5 -72%	1.3E6 -31%	9.4E5 -51%	8.4E5 -55%	2.0E6 +5%	1.9E6 1
	<i>P</i>	19.53 +24%	31.69 +101%	18.68 +19%	40.03 +131%	16.15 +3%	15.73 1
	#link	8184 +1%	8184 +1%	8184 +1%	8184 +1%	8192 +2%	8064 1
	#WL	8720 ×5.4	5.9E4 ×36.9	3480 ×2.2	5.7E4 ×35.0	3226 ×2.0	1613 1
6400	#hop	10.97 -80%	7.68 -86%	26.31 -51%	6.71 -87%	40.30 -24%	53.30 1
	<i>C</i>	2.0E6 -73%	2.3E6 -68%	4.3E6 -41%	2.7E6 -63%	7.7E6 +5%	7.3E6 1
	<i>P</i>	30.60 +24%	55.09 +124%	28.16 +15%	66.95 +163%	25.24 +3%	24.59 1
	#link	12792 +1%	12792 +1%	12792 +1%	12792 +1%	12800 +1%	12640 1
	#WL	1.4E4 ×5.5	1.2E5 ×45.8	4696 ×1.9	1.1E5 ×44.0	5056 ×2.0	2528 1
9216	#hop	11.35 -82%	7.95 -88%	30.66 -52%	6.94 -89%	49.00 -23%	64.00 1
	<i>C</i>	4.7E6 -78%	1.2E7 -46%	1.3E7 -38%	7.2E6 -65%	2.3E7 +10%	2.1E7 1
	<i>P</i>	45.66 +29%	87.48 +147%	40.56 +14%	104.4 +193%	36.34 +3%	35.43 1
	#link	18424 +1%	18424 +1%	18424 +1%	18424 +1%	18432 +1%	18240 1
	#WL	2.3E4 ×6.3	2.0E5 ×54.8	6762 ×1.9	1.9E5 ×52.8	7296 ×2.0	3648 1

With the increase of injection rate, the power consumption of mesh and torus is gradually larger and larger than that of BNIT, which mainly comes from more power consumption generated by frequent *read&write* of buffers and traversal of crossbars. When the injection rate reaches 0.002 and above, *read&write power* and *crossbar power* of mesh, which even account for about 25% of total power consumption, are about 4 times that of BNIT.

Packet latency often has a direct impact on overall performance. Figure 13 depicts the normalized average communication latency of different-scale mesh, torus, and BNIT at four different traffic patterns. In all cases, BNIT shows an average latency of at least 55% lower than mesh and torus. For the deterministic packet routing, the lower average hop count of the routing paths makes sense and is reflected in network latency.

In summary, under these traffic patterns with non-local communication, when the injection rate is slightly higher, BNIT presents lower power consumption and average communication latency, which depends on the lower average hop count between any two nodes. Hence, BNIT can be a promising solution for realizing global communication with strong coupling between cores.

C. Performance Validation of Large-scale Applications Using *BookSim2*

Table VII and VIII depict the full evaluation of topologies with 1024 (32 * 32), 4096 (64 * 64), and 6400 (80 * 80) cores, respectively. We execute the greedy-based mapping algorithm [13] and WOAGA [42] on mesh, torus, and BNIT for comparison. Executing the proposed application mapping can directly provide average communication hop count

#hop, success percentage #suc, and runtime #RT. Average latency #latency, basic power consumption #PB, communication power consumption #PC, and total power consumption #PT are derived from a cycle-accurate NoC simulation using *BookSim2*. The units of power consumption and average latency are respectively watts and cycles.

In Table VII and VIII, success percentage means that the percentage of routing paths satisfying the constraints of hop count and link bandwidth. BSOR [46] is used to allocate the routing path for each flow. Compared with other “topology+method”, in most cases, the generated brain-network-inspired NoC design has a significantly lower average hop count, lower average latency, lower communication power consumption, and significantly higher success percentage for the different-scale benchmarks, even though our mapping method takes less runtime. As shown in Table VII, in addition to the application of *D_3980*, on average, the brain-network-inspired NoC reduces the average hop count by 64%, average latency by 32%, and communication power consumption by 14%, respectively, and increases success percentage by 84%, compared with mesh-based NoC. Besides, the total power consumption has increased by 20% on average, due to the higher basic power consumption. In particular, for graph processing applications with a power-law and tightly coupled inter-core communication in Table VIII, the brain-network-inspired NoC architecture has up to 70% lower average hop count and 75% lower average latency than mesh-based NoC, and the overall power consumption only increased by 10%. In addition, for *D_3980*, which is composed of many small benchmarks, the traditional regular NoC may be more suitable, due to only local communication within each benchmark.

Although the brain-network-inspired topology has a very

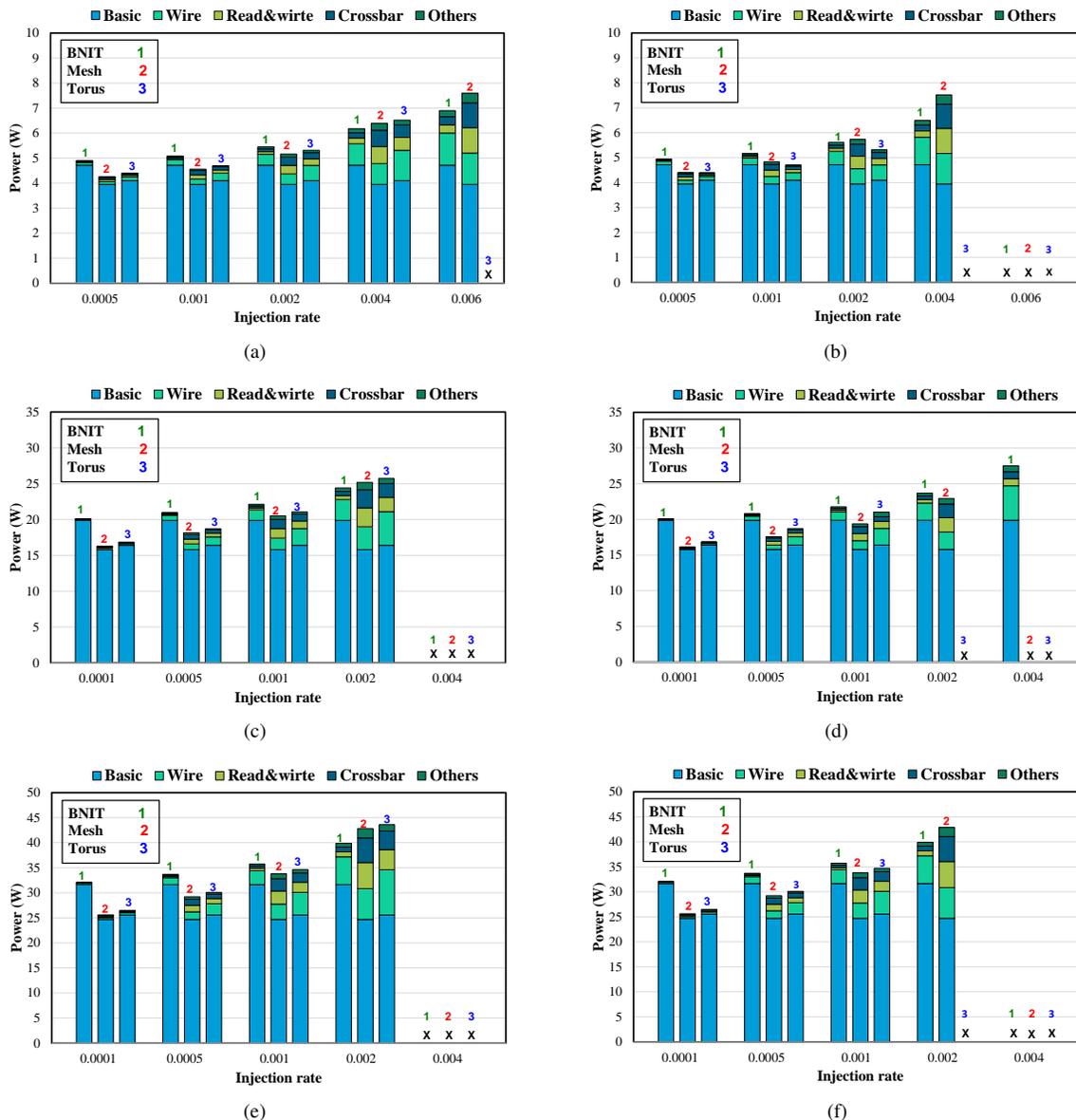


Fig. 12. Power evaluation for mesh, torus, and BNIT with 1024 cores at (a) uniform and (b) bitcomp traffic patterns, with 4096 cores at (c) uniform and (d) shuffle traffic patterns, and with 6400 cores at (e) uniform and (f) randperm traffic patterns.

low average hop count, the mapping method will also obviously affect the overall communication performance of the communication architecture. On the whole, by comparing the three task mapping methods, the proposed method is superior than others in all metrics and is suitable for BNIT. Specifically, compared to the greedy-based method [13] and WOAGA [42], our mapping method can obtain about 3% and 28% lower average hop count, and 10% and 35% lower communication power consumption, respectively.

Figure 14 depicts the hop count distribution of the routing paths using different topologies and mapping methods to process G_{4096} as shown in Table VII. Mesh and torus have a very low success percentage, only around 50%, and the hop count of most communication flows is very high and far beyond the constraint of hop count. Thanks to the advantage of the extremely low average hop count of BNIT, almost all

flows in NoC with any one of the three mapping methods have a small hop count for routing, which also enables lower network communication latency.

In summary, the generated brain-network-inspired NoCs have great advantages in three aspects, including the extremely low average hop count, low average latency, and high success percentage, for global communication. When there are a large number of communication flows and strong inter-core coupling, the lower communication power consumption of BNIT can compensate for its higher basic power consumption compared with mesh, and thus achieving a small increase in total power consumption. This also echoes the experiment results on BNIT under synthetic traffic patterns in Section V-B4. The cycle-accurate simulations of applications demonstrate the effectiveness of this brain-network-inspired NoC for large-scale interconnections, especially as a promising

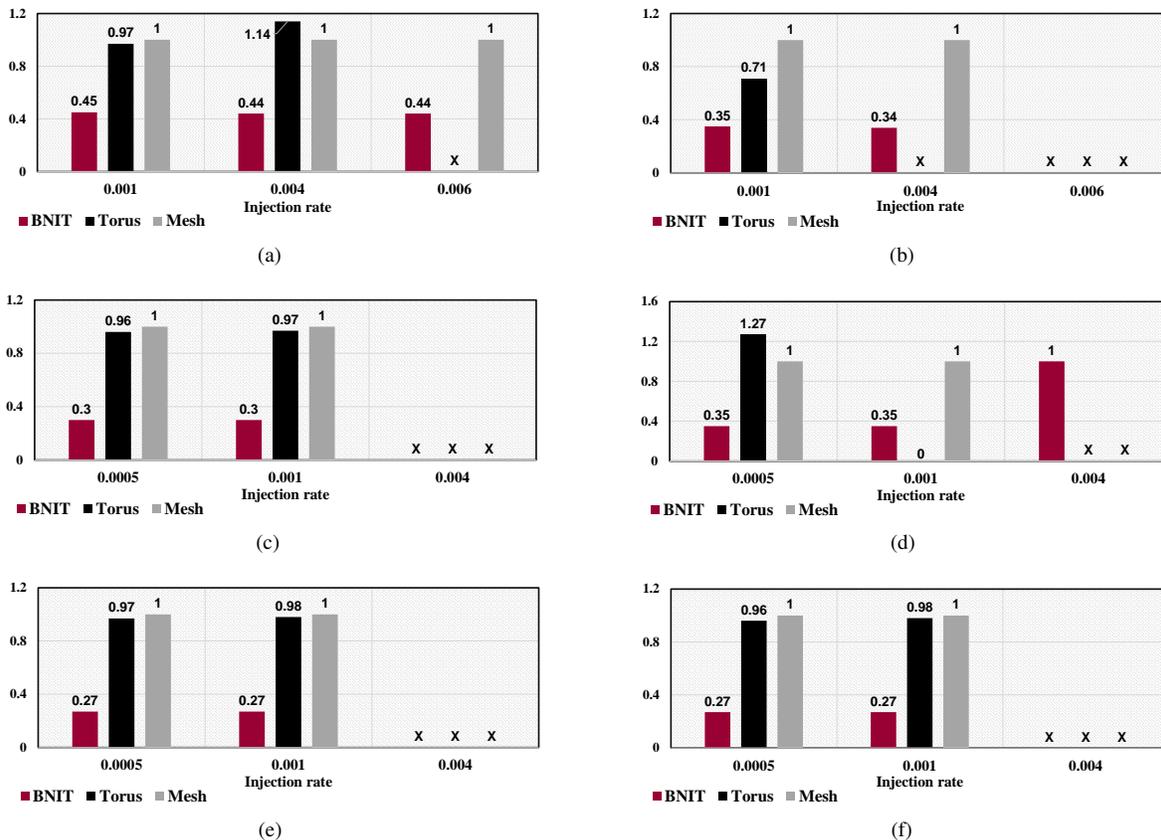


Fig. 13. Normalized average communication latency for mesh, torus, and BNIT with 1024 cores at (a) uniform and (b) bitcomp traffic patterns, with 4096 cores at (c) uniform and (d) shuffle traffic patterns, and with 6400 cores at (e) uniform and (f) randperm traffic patterns.

domain-specific solution for graph processing applications.

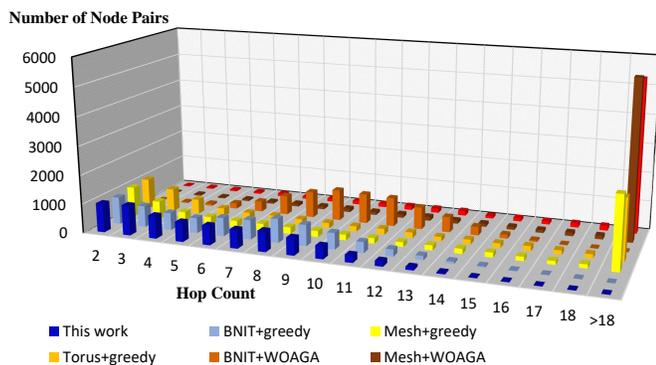


Fig. 14. The hop count distribution of the routing path using different "topology+method" to process G_{4096} as shown in Table VII.

In Figure 15, we can see that for the four benchmarks, compared with BSOR [46], the communication power consumption based on the proposed Lagrangian relaxation method is reduced by about 7% on average under a similar average hop count, and all routing paths meet the hop count and bandwidth constraint. The results show the effectiveness of our routing algorithm.

VI. CONCLUSIONS

Regular interconnection topologies are simple and easy to implement, but they are not suitable for large-scale NoCs

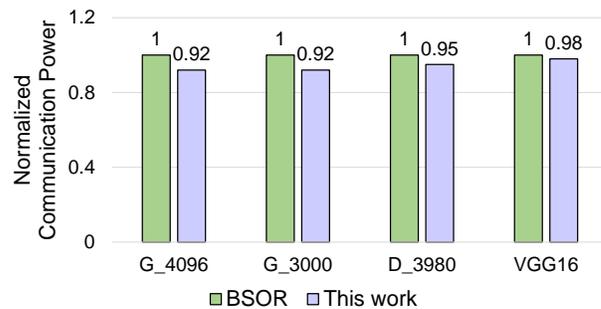


Fig. 15. Normalized communication power of BSOR compared with the proposed routing algorithm for different benchmarks.

because of its extremely high average hop count and latency. In this paper, we propose to generate efficient brain-network-inspired interconnections for large-scale NoCs and address the large-scale application mapping problem for the brain-network-inspired NoC design. The simulation results show that, compared with conventional regular NoCs, the resulting brain-network-inspired NoC is a better solution to provide extremely low average hop count and low average latency for large-scale NoCs with global communication, especially in graph processing applications. In the future, we will further exploit to generate brain-network-inspired interconnections for large-scale NoCs on 3D ICs for higher integration and power efficiency.

TABLE VII
COMPARISON OF NETWORK PERFORMANCE WITH LARGE-SCALE APPLICATIONS USING *BookSim2*.

Network size	Benchmark	Topo.+ method	#hop	#latency	#PB	#PC	#PT	#suc	RT (s)
64 * 64(4096)	G_4096	This work	6.26 -61%	45.0 -43%	19.8 +26%	3.9 -11%	23.7 +17%	96.5% +86%	380 -2%
		BNIT+greedy	6.65 -59%	49.0 -38%	19.8 +26%	4.5 +2%	24.3 +21%	96.0% +85%	424 +9%
		Mesh+greedy	16.23 1	79.6 1	15.8 1	4.4 1	20.2 1	51.9% 1	389 1
		Torus+greedy	13.5 -17%	119.8 +51%	16.2 +2%	7.2 +63%	23.3 +15%	57.3% +10%	417 +7%
		BNIT+WOAGA	10.25 -37%	70.7 -11%	19.8 +26%	8.0 +81%	27.8 +38%	79.5% +53%	3251 ×74
		Mesh+WOAGA	38.70 +138%	- -	15.8 0%	12.7 +189%	28.5 +41%	13.0% -75%	2888 ×64
		Torus+WOAGA	28.14 +73%	- -	16.2 +2%	13.6 +210%	29.8 +47%	14.3% -72%	3096 ×70
	G_3700	This work	6.00 -62%	43.8 -44%	19.8 +26%	4.8 -12%	24.6 +16%	97.0% +87%	342 -4%
		BNIT+greedy	6.40 -59%	47.9 -39%	19.8 +26%	5.4 +1%	25.2 +19%	96.8% +86%	387 +9%
		Mesh+greedy	15.79 1	78.6 1	15.8 1	5.5 1	21.3 1	52.0% 1	356 1
		Torus+greedy	18.12 +15%	96.0 +22%	16.2 +2%	10.7 +96%	26.8 +26%	47.2% -9%	401 +13%
	VGG16	This work	5.62 -69%	30.5 -8%	19.8 +26%	2.2 +48%	22.0 +28%	99.3% +80%	353 -5%
		BNIT+greedy	5.68 -68%	36.0 +8%	19.8 +26%	2.5 +68%	22.3 +29%	99.3% +80%	396 +7%
		Mesh+greedy	17.92 1	33.3 1	15.8 1	1.5 1	17.3 1	55.2% 1	370 1
		Torus+greedy	12.56 -30%	59.2 +78%	16.2 +2%	2.7 +82%	18.9 +9%	57.3% +3.8%	394 +6%
	D_3980	This work	3.67 -7%	31.8 +18%	19.8 +26%	2.0 +65%	21.8 +29%	99.8% +5%	358 -4%
		BNIT+greedy	3.68 -7%	32.3 +20%	19.8 +26%	2.2 +82%	22.0 +30%	99.8% +5%	401 +8%
		Mesh+greedy	3.95 1	27.0 1	15.8 1	1.2 1	17.0 1	94.8% 1	372 1
		Torus+greedy	5.70 +44%	59.2 +119%	16.2 +2%	2.6 +177%	18.8 +15%	99.5% -9%	410 +10%

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TABLE VIII
COMPARISON OF NETWORK PERFORMANCE WITH GRAPH PROCESSING APPLICATIONS USING *BookSim2*.

Network size	Benchmark	Topo.+ method	#hop	#latency	#PB	#PC	#PT	#succ	RT (s)
32 * 32(1024)	<i>email-Eu-core</i>	This work	6.40 -48%	50.3 -75%	4.7 +20%	2.5 -10%	7.2 +8%	100% +70%	4 -20%
		BNIT+greedy	6.65 -46%	61.5 -70%	4.7 +20%	2.7 -6%	7.4 +9%	100% +70%	4 -20%
		Mesh+greedy	12.36 1	207.4 1	3.9 1	2.8 1	6.7 1	58.8% 1	5 1
		Torus+greedy	12.36 0%	215.5 +4%	4.1 +3%	3.8 +36%	7.9 +16%	69.5% +18%	5 0%
		BNIT+WOAGA	7.78 -37%	65.8 -68%	4.7 +20%	3.3 +17%	8.0 +19%	99.2% +69%	383 ×76
		Mesh+WOAGA	20.5 +66%	- -	3.9 0%	36.8 +66%	4.7 +28%	8.61% -65%	196 ×39
		Torus+WOAGA	15.44 +25%	- -	4.1 3%	5.3 +86%	9.4 +38%	35.1% -40%	251 ×50
80 * 80(6400)	<i>p2p-Gnutella08</i>	This work	8.17 -70%	57.4 -64%	30.9 +26%	7.4 -23%	38.0 +12%	92% +237%	1351 -2%
		BNIT+greedy	8.28 -69%	59.7 -63%	30.9 +26%	7.8 -18%	38.7 13%	92.3% +238%	1940 +40%
		Mesh+greedy	26.92 1	161.1 1	24.6 1	9.61 1	34.2 1	27.3% 1	1382 1
		Torus+greedy	30.46 +13%	228.0 +42%	25.2 +3%	16.9 +76%	42.2 +23%	20.2% -26%	1865 +35%
		BNIT+WOAGA	11.00 -59%	75.6 -53%	30.9 +26%	11.0 +15%	41.9 +23%	69.5% +155%	12350 ×80
		Mesh+WOAGA	50.91 +89%	- -	24.6 0%	19.9 +107%	44.5 +30%	6.7% -75%	10581 ×67
		Torus+WOAGA	37.82 +41%	- -	25.2 +3%	21.8 +127%	47.1 +38%	7.3% -73%	11974 ×77

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