Efficient Data Race Detection of Async-Finish Programs Using Vector Clocks

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Abstract

Existing data race detectors for task-based programs incur significant run time and space overheads. The overheads arise because of frequent lookups in fine-grained tree data structures to check whether two accesses can happen in parallel.

This work shows how to efficiently apply vector clocks for dynamic data race detection of async-finish programs with locks. Our proposed technique, *FastRacer*, builds on the FastTrack algorithm with per-task and per-variable optimizations to reduce the size of vector clocks. FastRacer exploits the structured parallelism of async-finish programs to use a coarse-grained encoding of the dynamic task inheritance relations to limit the metadata in the presence of many concurrent readers. Our evaluation shows that FastRacer substantially improves time and space overheads over FastTrack, and is competitive with the state-of-the-art data race detectors for async-finish programs with locks.

CCS Concepts: • **Software and its engineering** → **Software testing and debugging**; **Runtime environments**; **Multiprocessing / multiprogramming / multitasking**.

Keywords: Concurrency bugs, data races, happens-before, dynamic program analysis, task parallelism, async-finish

1 Introduction

The task-based programming abstraction helps write efficient and portable parallel code without having to think of low-level threads. Tasks execute in parallel as hardware-agnostic logical units of work, and programmers only specify the dependencies among the tasks. An accompanying runtime schedules tasks to threads and provides performance features like work-stealing to load-balance the execution. Cilk [8, 23], X10 [11], Habanero-Java [10], and Java Fork-Join [30] are popular task-based frameworks.

Task-based programs are susceptible to concurrency errors such as atomicity violations [62] and data races [3, 19, 47, 48, 58]. A *data race* occurs when two accesses, with at least one write, from different tasks are incorrectly synchronized. The presence of data races in shared-memory programs often indicates the presence of other concurrency errors [20], and can affect an execution by crashing, hanging, or corrupting data [28]. Data races are hard to detect and fix since they may occur nondeterministically under specific thread interleavings, program inputs, and execution environments. Data races have led to several real-world disasters [31, 42, 45]; such high-profile failures are a testament that data races are present even in well-tested code.

The problem. There exists prior work to detect data races in task-based programs [3, 12, 19, 36, 47, 48, 58, 63, 64]. Most analysis utilize the series-parallel structure of execution of task-based programs to check whether accesses can potentially execute in parallel (called *series-parallel maintenance*) [3, 19, 48, 58, 63]. Prior techniques are either serial (e.g., [12, 19, 47]) or are difficult to parallelize (e.g., [3]), detect races only in a given schedule (e.g., [21]), continue to incur high run-time overheads (e.g., [36, 48, 63]), require tight coupling with the runtime scheduler for good performance (e.g., [58]), or do not support lock-based synchronization (e.g., [3, 48, 58]).

Our approach. In this work, we focus on efficient detection of *per-input apparent data races in task-based programs with async-finish semantics.*[1] For a given application and an input, per-input races include races observed in the current schedule as well as other schedules with possibly

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[1]Apparent data races occur because of the usage of parallel task constructs and ignore the per-schedule dynamic interleavings [40]. Feasible data races consider the nondeterministic timing variations during execution.

permuted memory operations, ignoring schedule-sensitive branches [63]. While prior work has *ignored* how to optimize vector clocks for efficient race detection of task-based programs, we *argue* that analyses based on vector clocks are generic, inherently parallel, and have better data locality than tree-based data structures for series-parallel (SP) maintenance. However, a naïve application of vector-clock-based analysis to tasks results in prohibitive memory and run-time overhead [48, 63].

This paper presents *FastRacer*, a vector-clock-based data race detector for async-finish programs. FastRacer avoids the redundancy in *per-task* vector clocks by using auxiliary immutable data structures to maintain space- and time-efficient lossless vector clock representations correctly. FastRacer exploits the structured parallelism in async-finish programs to optimize the space requirement of *per-variable* metadata in the presence of many concurrent readers. Prior work has shown that a careful selection of only two "concurrent read" accesses is sufficient for detecting read-write data races for async-finish programs [48, 63]. FastRacer uses coarse-grained encoding of dynamic task inheritance relationships to identify the two accesses (for both reads and writes) necessary for race detection, and uses vector clocks to check whether two accesses can race.

We evaluate the performance and correctness of FastRacer on C++ applications that use Intel TBB [49] for task parallelism and compare with prior work [21, 58, 63]. Our evaluation shows that the run time and memory overhead of Fast-Racer is substantially lower compared to state-of-the-art data race detectors that target async-finish programs.

Contributions. This paper makes the following contributions:

- To the best of our knowledge, this work is the *first* to show the viability of using vector clocks for efficient dynamic analysis of task-based programs;
- a race detector called FastRacer that detects per-input apparent races in async-finish programs with locks,
- publicly available implementations of FastRacer and related techniques, and an evaluation that shows Fast-Racer significantly outperforms prior work.

2 Background and Motivation

This section briefly reviews data race detection of multi-threaded programs using vector clocks. We also discuss closely related prior work on race detection of async-finish programs.

2.1 Race Detection with Vector Clocks

Many race detectors for multithreaded programs use vector clocks to track happens-before (HB) relations in an execution [9, 21, 46, 55]. Each thread maintains a scalar clock that is incremented at *synchronization release* operations (e.g., lock release, monitor wait, thread fork and join, and volatile write). Each thread T also maintains a vector clock **C** of size n,

where there are n threads in the application. The clock entry $C_T(U)$ records the clock of thread U when thread T last synchronized with U. A dynamic analysis updates per-variable vector clock metadata whenever a thread accesses a shared data or a lock variable. Vector clock operations require $\mathcal{O}(n)$ time and storage to monitor an execution with n threads.

Algorithm 1 FastTrack analysis at synchronization operations

1: **procedure** SPAWN   ▷ Thread T spawns U
2:   U.vc ← T.vc ∪ {T.epoch}
3:   T.epoch ← T.epoch + 1   ▷ Increment T's scalar clock
4:   U.epoch ← U.epoch + 1
5: **procedure** JOIN   ▷ Thread T joins with U
6:   **for all** <t,c> in U.vc **do**
7:    T.vc[t] ← max(U.vc[t], T.vc[t])
8: **procedure** ACQUIRE   ▷ T acquires lock L
9:   **for all** <t,c> in L.vc **do**
10:    T.vc[t] ← max(L.vc[t], T.vc[t])
11: **procedure** RELEASE   ▷ T releases lock L
12:   L.vc ← T.vc
13:   T.epoch ← T.epoch + 1
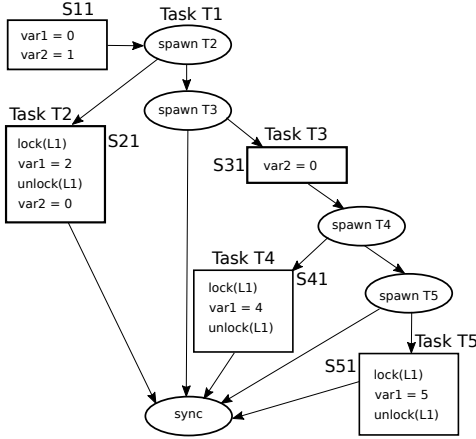14: **function** CHECKHB(c@u,T)   ▷ Check HB between epoch
15:   **return** c@u ⪯ T.vc

FastTrack. The *FastTrack* algorithm tracks a single last writer and, in many cases, a single last reader [21]. The total order on writes in a data-race-free program allows FastTrack to store only the *last* write information. FastTrack stores the write metadata as an epoch c@T, which is a tuple consisting of the writer thread identifier T and the value of T's clock (say c) at the time of the write. The read metadata alternates between epoch and vector clock forms. An epoch representation suffices when there is a single reader or the current read happens after all previous reads. When there are concurrent readers, the read metadata is a vector clock (denoted by vc). Algorithm 1 shows the pseudocode for the dynamic analysis performed by FastTrack at synchronization operations. Before each access to a shared variable x by a thread T, FastTrack checks whether the current access by T happens after the previous write and all previous reads to x (CheckHB, Algorithm 1). A data race is reported if the current access by T is concurrent with the last accesses. The shared data and lock variable metadata are updated upon a thread access. FastTrack is popularly used as the basis for dynamically sound and precise[2] data race detection of multithreaded programs [2, 9, 16, 43, 55, 60].

2.2 Race Detection for Async-Finish Programs
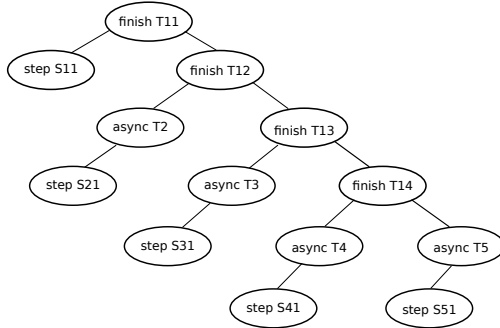
Frameworks like X10 [11] and Habanero Java [10] support structured task parallelism with async-finish semantics. The statement "async {t}" creates a new child task t that can run in series or in parallel with its parent task. The statement "finish {t}" causes the current task to wait for all the

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[2]*Sound* means no false negatives, and *precise* means no false positives.

(a) An async-finish program with tasks T1–T5, shared variables var1 and var2, and a lock variable L1.

(b) The DPST for the program in Figure 1a.

Figure 1. An async-finish program and its DPST.

recursively-created tasks within the block t. The async-finish model is terminally-strict, which means each join edge goes from the last instruction of a task to *any* of its ancestors in the inheritance tree [47]. In the following, we discuss dynamic data race detection techniques for async-finish programs.

SPD3. SPD3 [48] uses a *dynamic program structure tree* (DPST) to capture the semantics of an async-finish program. A DPST consists of step, finish, and async nodes. A step node represents the maximal sequence of instructions without any task management. An async node represents the spawning of a child task by a parent task. The descendants of an async node execute asynchronously with the remainder of the parent task. A finish node is created when a parent task spawns a child task and waits for the child, and its descendants, to complete. A finish node is thus the parent of all async, finish, and step nodes executed by its children or their descendants. Figure 1 shows an async-finish program and the corresponding DPST. All executions of a data-race-free async-finish program with the same input result in the same DPST [48].

The operational semantics of async-finish programs imply a left-to-right computation order of sibling nodes belonging to a common parent task. Thus, a DPST node's children are

also ordered left-to-right to reflect the computation order in their parent. On a variable access, SPD3 searches for the *lowest common ancestor* (LCA) of the current access (i.e., a step node) and the last access stored in the variable's metadata. SPD3 reports a race if the left child of the LCA, which is an ancestor of the step node representing the last access, is an async node that indicates *concurrent* execution of the last access and the current task. The DPST allows SPD3 to maintain one metadata location for writes and two locations for reads in shadow memory.

PTRacer. PTRacer extends SPD3 by detecting apparent races in async-finish programs with locks [63]. PTRacer maintains two metadata locations each for reads and writes to a shared variable. The metadata per variable is proportional to the number of different locksets (i.e., set of locks held by the tasks at any time) with which the variable is accessed, which is reasonable in practice because variables are usually accessed with similar locking patterns.

PTRacer selects two "last read" ("last write") accesses from multiple parallel accesses with the same lockset to maintain constant metadata, such that any future write which can race with any one of the parallel reads (writes) will race with either one of the two chosen "last readers" ("last writers"). PTRacer makes these choices by selecting step nodes with the highest LCA among all parallel step nodes. PTRacer detects *all* races for a given input even in the presence of lock-based synchronization. Consider the shared variable var1 which is updated by the parallel tasks T2, T4, and T5 in Figure 1a. The step nodes corresponding to these accesses are S21, S41, and S51, respectively. Since, S21 and S51 have the highest LCA in the corresponding DPST, PTRacer will store these two accesses and discard the access information for S41.

The race analysis in PTRacer is similar to SPD3. PTRacer will report a race on var2 for the example in Figure 1 because the left child of the LCA of step nodes S21 and S31 is an async node. SPD3 will report false races on the variable var1.

PTRacer uses the DPST to maintain a constant amount of per-variable metadata independent of the number of tasks executing the program. Furthermore, PTRacer performs frequent lookups in the DPST to check whether two accesses can happen in parallel. However, the DPST can be deep for programs with a recursive pattern of task creation and large because of many step nodes. These lead to high run time and memory overheads. PTRacer uses an array-based representation of the DPST and caches LCA lookups to improve the performance of LCA. However, the DPST and the LCA computation continue to be a significant bottleneck for several benchmarks, as we show in Section 5.2. Thus, there is a need for *more efficient* techniques to help detect data races in async-finish programs.

3 FastRacer: Efficient Dynamic Data Race Detection for Async-Finish Programs

The thesis of this work is that vector clocks can provide better data locality for series-parallel (SP) maintenance in task-based programs compared to tree-based data structures used in prior work (e.g., [48, 58, 63]). We present *FastRacer*, a novel algorithm that integrates the benefits of vector-clock-based analysis *and* exploits structured parallelism of async-finish programs to limit the amount of per-variable metadata.

Task-based programs create more, often orders of magnitude, parallel tasks than threads in multithreaded programs. For example, the benchmark nearestNeigh creates up to $\sim 3 \times 10^6$ tasks (Table 2). Race detectors like FastTrack use per-thread and per-variable vector clocks to capture the clock values of all the threads in the system. While this representation works fine for multithreaded programs where the number of concurrent threads is comparatively small ($\sim$#cores), it is impractical for task-based programs and leads our FastTrack implementation to run out of memory on several benchmarks (Section 5.2). Storing only non-zero entries in a vector clock does not help since several concurrent tasks potentially access shared read-only variables. Furthermore, maintaining vector clocks proportional to the number of threads can detect only feasible data races and misses races among concurrent tasks [24]. In the following, we discuss novel ideas to solve these challenges.

Algorithm 2 FastRacer analysis at synchronization operations

1: **procedure** SPAWN   ▷ Task T spawns task U
2:     **if** size(T.rw_vc) > THRESHOLD **then**
3:        T.ro_vc ← REF({T.ro_vc ∪ T.rw_vc})
4:        T.rw_vc ← ∅
5:     **else**
6:        U.ro_vc ← T.ro_vc
7:        U.rw_vc ← T.rw_vc
8:     U.rw_vc ← U.rw_vc ∪ {T.epoch}
9:     U.joined ← T.joined
10:    U.lockset ← T.lockset
11:    U.IVC ← T.IVC ∪ {getClock(U.epoch)}
12:    T.epoch ← T.epoch + 1
13:    U.epoch ← U.epoch + 1
14: **procedure** JOIN   ▷ Task T joins with U
15:    T.joined ← T.joined ∪ {getTaskId(U.epoch)}
16: **function** CHECKHB(c@u,T)
17:              ▷ Check HB between epoch c@u and T's access
18:    **return** c@u $\preceq$ T.rw_vc **or** c@u $\preceq$ T.ro_vc **or** u ∈ T.joined

---

3.1 Adapting Vector Clocks for Task Parallelism

We analyzed the performance of FastTrack and found that operations on task vector clocks incur high time and space overhead. For example, the task join operation is a bottleneck because it requires comparing and merging *all* the clock values in the child and the parent tasks' vector clocks. Naïvely merging the vector clocks is not required since most vector clock entries remain unchanged during the lifetime of a task.

Tracking read-only clock entries. The first insight in FastRacer is that *most* vector clock entries for a task remain unchanged during the lifetime of the task, and the clock values continue to be the same as in the parent task. Thus, maintaining per-task copies of the clock entries is mostly redundant.

In FastRacer, a task vector clock is partitioned into a read-only (denoted by ro_vc) and a read-write portion (denoted by rw_vc). Child tasks in FastRacer maintain a reference to the ro_vc of their parents instead of maintaining redundant copies. During a spawn operation (Algorithm 2), FastRacer first checks if the size of rw_vc is greater than a threshold. If yes, then FastRacer merges ro_vc and rw_vc of the parent task into a new ro_vc for the child task and rw_vc of child task is kept empty. Otherwise, the child ro_vc points to the parent ro_vc and the parent's rw_vc is copied to the child's rw_vc. Avoiding needless copies and redundant operations on the read-only portions of vector clocks helps reduce space overheads *and* improve performance. In the common case, most vector clock entries of a task remain unchanged, i.e., the size of rw_vc is small. Complete vector clock copies happen only when the size of rw_vc is greater than THRESHOLD.

Optimizing vector clock join. An access to a shared variable by a parent task after joining with a child task always happens after the child's accesses, since the accesses are synchronized by the join operation. The second insight is that FastRacer does not need to store the clock values of the child tasks *after* the join operation. Instead, tracking the set of all child tasks that have joined with the parent task suffice.
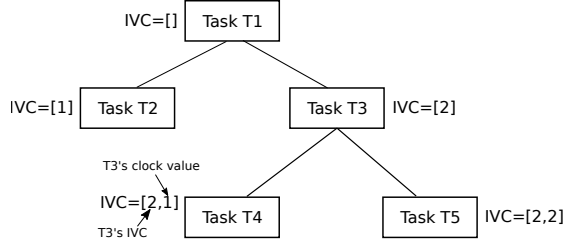
Each task in FastRacer maintains the set of child tasks that have already joined with it in a joined data structure. No vector clock join occurs when a task T joins with task U, instead, the child task is added to the joined of the parent task (Algorithm 2). When a parent task spawns a new child task, the parent joined is copied to the child joined. The size of task vector clocks reduces significantly due to the joined optimization. Note that a trivial implementation of joined may not give performance benefits over FastTrack. We use efficient set implementations based on the Union-Find data structure, which reduces the overhead of set operations.

Vector clock caching. The vector clocks for a few tasks can be large even after the optimizations. FastRacer uses explicit attributes to cache recently used vector clock values to avoid the cost of looking up the map data structure representing vector clocks. FastRacer indexes into the vector clock map when the thread id is not among the most recently used.

3.2 Specializing for Async-Finish Programs

It can be expensive to maintain all concurrent readers of a shared variable in task-based programs. FastRacer uses coarse-grained tracking of task inheritance relationships to

Figure 2. The inheritance tree for program in Figure 1a.

select relevant accesses from parallel readers/writers,[3] which allows maintaining constant per-variable metadata per-lockset (i.e., the set of locks held by the task).

Maintaining constant per-variable metadata. FastRacer models the parent-child relationship among different tasks with a *task inheritance* tree. The nodes represent tasks, and edges represent the creation of child tasks by the parent. Figure 2 shows the inheritance tree for the program shown in Figure 1a (ignore the IVC labels for now). FastRacer uses the inheritance tree to *efficiently* select two accesses out of multiple concurrent accesses with the same lockset, such that any racy future access that races with any one of the concurrent accesses must be racy with either one of the two chosen last accesses. For parallel tasks accessing a variable with the same lockset, FastRacer stores the access history of the two tasks with the highest LCA in the inheritance tree. Consider the three accesses to var1 from tasks T2, T4, and T5 in Figure 1a. In the inheritance tree shown in Figure 2, task nodes T2 and T4 (or T5) have the highest LCA, and so FastRacer stores the access histories from T2 and T4 and discards T5. Any later access to var1, which is not parallel with both T2 and T4, will not be parallel with T5. So, discarding T5's access information is correct.[4] The metadata stored per shared variable in Fast-Racer is proportional to the number of the different locksets with which the variable has been accessed.

The primary difference between a DPST and FastRacer's inheritance tree is in the *granularity* of the nodes. While a DPST decomposes a task into several unsynchronized regions represented by step nodes, an inheritance tree has just one node per task. The coarser modeling makes the inheritance tree much smaller and shallower than the DPST. Unlike a DPST, there is no left-to-right ordering in an inheritance tree. While PTRacer uses DPST to check the concurrency between two accesses and select accesses with the highest LCA, Fast-Racer only does the latter with the inheritance tree. FastRacer uses vector clocks for data race detection to compensate for the coarser modeling and loss of ordering between the nodes (Section 3.3).

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[3]When tasks use locks, two writes can happen in parallel but do not constitute a race if they are protected by the same lock.

[4]In async-finish semantics, a task must join with its ancestor, either immediate or recursive. In case a parent task calls join, all children tasks within this join scope, either immediate or recursive, join with it.

Inheritance vector clock. Instead of building an inheritance tree, FastRacer encodes the inheritance relations in a per-task array of clock values called *Inheritance Vector Clock* (IVC) for better performance. An IVC is an immutable vector clock that contains the clock values of all the reachable parents of a task T at the time of the creation of T. An IVC identifies the unique path in the inheritance tree from the root task to T, since a task spawn increments the scalar clock of the caller task. Whenever a parent task creates a child task, FastRacer copies the parent's IVC to the child and appends the parent's clock value at the end of child IVC. In Figure 2, the IVC of the parent task T3 is copied to the child task T4 and the current clock of T3 (assumed to be one) is appended.

Both IVC labeling and the Offset-Span (OS) labeling [36] schemes compute a unique label from the label of the immediate predecessor, and guarantee that the length of a task's label will always be proportional to the depth of the task in the inheritance tree. However, there are two differences. First, the IVC of a task, once created, is immutable. Unlike OS labeling, any further task join operations do not modify the IVC. Second, the Span part of OS labeling can only be assigned after the task graph is complete, i.e., OS labels cannot be computed while building the task graph. Intuitively, IVC labels are more similar to the Offset part, with the constraint that they do not get updated at join operations. Whereas prior work uses OS labels for race detection [24, 36], FastRacer uses IVC labels to identify two accesses out of multiple parallel accesses having the highest LCA in the inheritance tree.

Computing tasks with the highest LCA. To compute the highest LCA among three parallel tasks, FastRacer iterates over the IVCs of all the tasks simultaneously and stops at the first point of difference. After that, FastRacer chooses the task with a different clock value and any one of the other two. If all the three clock values are different, any two out of three tasks can be chosen. If FastRacer reaches the end of an IVC for any task T, it indicates that T must be the parent of the other two in the inheritance tree, and so, FastRacer chooses the parent task T and any one from the other two. The tasks so chosen will have the highest LCA in the inheritance tree (see Lemma 3.2). The computation overhead depends on the sizes of the IVC, which is equal to the height of the inheritance tree. Since an inheritance tree is much shallower compared to a DPST, the computation is relatively efficient.

In Figure 1a, the accesses to var1 from three parallel tasks, T2, T4, and T5, are with the same lockset {L1}. The IVCs of the corresponding task nodes, shown in Figure 2, are IVC_{T2}=[1], IVC_{T4} = [2,1], and IVC_{T5} = [2,2]. To select two out of the three accesses, FastRacer iterates over the three IVCs simultaneously. The first point of difference is at the first entry itself: $IVC_{T2}[0]$=1, $IVC_{T4}[0]$=$IVC_{T5}[0]$=2. So, FastRacer selects a task with a different clock value, i.e., T2 and any one of other two, say T4 (or T5). For the example in Figure 2, tasks T2 and T4 (or T5) indeed have the highest LCA in the inheritance tree.

(a) Metadata maintained in FastTrack.

```
1  class PerVariableMetadata {
2    epoch wr_md, rd_md; // Write and Read epoch
3    map<taskid, clock> rd_vc; // Read vector clock
4  }
5  class PerLockMetadata {
6    map<taskid, clock> vc;
7  }
8  class PerTaskMetadata {
9    epoch epoch;
10   map<taskid, clock> vc;
11 }
```

(b) Metadata maintained in FastRacer.

```
1  class PerVariableMetadata {
2    PerLockMetadata lock[];
3  }
4  class PerLockMetadata {
5    set<lockID> lockset;
6    epoch rd1, rd2;  // Reader 1 and 2 metadata
7    IVC* rd1_ivc, rd2_ivc; // IVC of Reader 1 and 2
8    epoch wr1, wr2;  // Writer 1 and 2 metadata
9    IVC* wr1_ivc,wr2_ivc; // IVC of Writer 1 and 2
10 }
11 class PerTaskMetadata {
12   epoch epoch;
13   map<taskid, clock> ro_vc; // Rd-only vector clock
14   map<taskid, clock> rw_vc; // Rd-wr vector clock
15   set<taskid> joined; // All joined child tasks
16   set<lockId> lockset; // Locks held by the task
17   int IVC[];
18 }
```

Figure 3. Comparison of metadata state maintained in Fast-Track and FastRacer.

3.3 Detecting Data Races

FastRacer extends the FastTrack algorithm (Section 2.1) to detect races and update metadata.

Metadata. Figure 3 compares the metadata maintained in FastTrack and FastRacer. Given a task T, FastTrack uses a vector clock for storing the epoch values of *all* other tasks (line 10, Figure 3a). The attributes ro_vc, rw_vc, and joined in PerTaskMetadata in Figure 3b correspond to the optimizations introduced in Section 3.2. While FastTrack uses vector clocks to track lock operations, FastRacer uses the lockset mechanism [52]. Every task in FastRacer maintains and updates lockset at lock acquire and release operations.

The per-variable state in FastRacer is an array of lock metadata. Each lock metadata stores the access history of the variable with the distinct set of locks held before the access. Every per-lock metadata contains four access history entries, two each for reads and writes, which contain the epoch value and a reference to the IVC of the task at the time
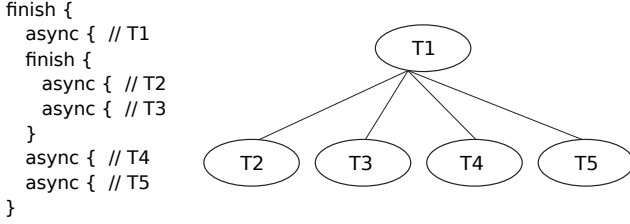
of access. Storing references to the IVCs suffice since they remain unchanged during the lifetime of a task.

Race checks. When a shared variable is accessed, Fast-Racer iterates over all the lock metadata corresponding to distinct locksets with which the shared memory variable has been accessed. An empty intersection of the lockset of the current access and the lock metadata implies potentially parallel accesses. If the two locksets are disjoint, FastRacer checks if the epoch values stored in the access history happens before the current access using vector clocks (CHECKHB, Algorithm 2). If there is no such relationship, it implies that the prior access is concurrent with the current access. Finally, FastRacer reports a data race if one of the two accesses is a write.

Before accessing a shared variable x, FastTrack compares the current task's vector clock with the epoch(s) stored in x's access history to determine if the current access to x happens *after* the past accesses (CHECKHB, Algorithm 1). FastRacer, apart from the vector clock entry check, also checks if the tasks present in x's access history belong to joined of the current task. If all the tasks are present in joined, FastRacer infers that the current access happens *after* prior accesses. Since the vector clock is spread across ro_vc, rw_vc, and joined, CHECKHB (Algorithm 2) checks the HB relation against all of them.

Metadata updates. FastRacer updates the read metadata corresponding to the current lockset if a read does not race with prior writes. FastRacer checks if any of the read epochs in the lock metadata corresponding to the current lockset happens before the current task's access. If yes, then Fast-Racer updates that access entry with the current task's epoch and IVC. Otherwise, there are three parallel reads, and Fast-Racer needs to select two with the highest LCA. FastRacer iterates over the IVC of all three access entries and stops either at the first point of difference or if one of the IVCs end. FastRacer stores the access history of the task corresponding to the selected IVC and any one of the other two. Using any one of the other two works since, in both the cases, the two chosen tasks will have the highest LCA in the inheritance tree (Section 3.2). Figure 4 shows an example of how FastRacer updates the read metadata. Assume tasks T2, T3, and T4 all read a shared variable x and task T5 writes x. After the reads from T2 and T3, the two readers stored for the variable x are T2 and T3, because both these tasks can run in parallel. Since task T4 is spawned by T1 after T1 synchronizes with T2, so the read by T4 happens after the read of T2. The read metadata entry of T2 is replaced by T4. Next, when T5 writes x, Fast-Racer checks the access with all previous reads and reports a read-write race between the accesses from T4 and T5. The steps performed by FastRacer on a write access are similar.

Synchronization operations. During a spawn operation (Algorithm 2), FastRacer checks if the size of rw_vc is greater than a threshold. If yes, FastRacer merges ro_vc and rw_vc of

```
finish {
  async { // T1
  finish {
    async { // T2
    async { // T3
  }
  async { // T4
  async { // T5
}
```


Figure 4. An async-finish program with five tasks T1–T5 and the corresponding inheritance tree.

the parent task into a new ro_vc for the child task and rw_vc of the child is kept empty. Otherwise, the child ro_vc references the parent ro_vc, and the child rw_vc is copied from parent rw_vc. Thereafter, FastRacer copies the parent's joined and lockset to the child's joined and lockset, respectively. In case of a join operation, the joined of the parent task is updated to contain the id of the child task.

A task's vector clock is not updated in case of lock acquire and release operations. Instead, FastRacer uses PTRacer's mechanism to deal with lock operations. Each task maintains a lockset. When a task T acquires a lock L, the lockset of T is updated to contain lock L. In case of a lock release, L is removed from the lockset. When T accesses a shared variable x, the lockset is copied to the variable metadata. During a race check, FastRacer checks for the intersection of the locksets from the metadata history to infer a data race. In practice, variables are accessed with the same set of locks, and hence maintaining access metadata for different sets of unique locks is reasonable. Furthermore, metadata update operations depend on the size of the IVC, but we find that the maximum depth of the inheritance tree is small (≤ 30 for our benchmarks).

3.4 Characterizing FastRacer

Race coverage. While FastTrack's race coverage is limited to the observed schedule, FastRacer can detect per-input apparent races like PTRacer. Although both FastTrack and FastRacer use vector clocks to track happens-before (HB) relations among accesses, FastRacer can detect races in *other* schedules due to the following algorithmic differences with FastTrack.

- FastTrack stores per-thread vector clocks. The races reported by FastTrack can vary across schedules since many tasks can map to a single thread, and the exact sequence of tasks mapped may vary across schedules. FastRacer stores vector clocks per task, and is not impacted by the mapping of tasks to threads.
- FastTrack tracks the HB relations to establish order among synchronization operations, which is sensitive to the order of lock operations and varies across schedules. FastRacer uses the lockset technique to track synchronization operations and stores two reads and two

writes per lockset in per-variable metadata. The metadata structure enables FastRacer to detect races irrespective of the order of lock operations, so the number of races reported is the same across schedules.

Correctness. The following two lemmas help prove the correctness of FastRacer. We discuss the proofs in the Appendix.

Lemma 3.1. *Storing access entries of only two tasks such that their LCA is the highest is sufficient. A future access to the variable, which is racy with any of the existing parallel accesses, must be racy with any one of the two access entries with the highest LCA.*

Lemma 3.2. *The IVC correctly computes the two tasks with the highest LCA among three parallel tasks.*

4 Implementation

Our implementation extends the PTRacer artifact.[5] A static compiler pass using LLVM 3.7 instruments load and store instructions in C++ programs, and inserts function calls to execute the appropriate dynamic race detection analysis. The implementation uses Intel Threading Building Blocks (TBB) [49] for task parallelism. The public implementation of PTRacer reports wrong race results for the benchmarks fluidanimate, kmeans, streamcluster, and sort (see Section 5.1). We found an implementation error was corrupting the DPST built by PTRacer, and there was a race while updating a global array data structure used for LCA hashing. After fixing these issues, the race reports were the same across all the tools. Our modifications have minimal ($\leq 1\%$) impact on the performance of PTRacer, and we use our fixed version for the evaluation. Our prototype implementation of FastRacer extend the same static compiler pass to ensure all the prototypes do the same work. We have also reimplemented the FastTrack algorithm [21, 22].

Race detection for fork-join programs. Utterback et al. propose a parallel and asymptotically optimal algorithm called WSP-Order for race detection of fork-join programs [58]. The algorithm uses two order maintenance (OM) data structures to maintain two total orders of all *strands* in the computation. A strand is a sequence of instructions that contain no parallel primitives and executes sequentially. A strand x logically precedes strand y if and only if x precedes y in both orderings. These orderings are sufficient to determine SP relationships. The two OM data structures support constant-time operations like insert and query, and *most* concurrent updates do not need synchronization. However, large parts of the OM data structure are updated during relabel operations and hence require synchronization. Since relabel operations are serialized, the algorithm modifies a work-stealing task scheduler to prioritize the operations. Furthermore, workers blocked on an insert

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[5] https://github.com/rutgers-apl/PTRacer

or a query operation help with the relabel instead of being idle. Note that the WSP-Order algorithm does not support lock-based synchronization and requires tight coupling with a work-stealing scheduler for good performance [58].

The public implementation of WSP-Order is called C-RACER.[6] Since the original implementation uses the Batcher runtime [1], we reimplement C-RACER with Intel TBB in LLVM for a fair comparison. An important contribution in the original C-RACER work is the parallelization of the relabel operations. We have not implemented task scheduler support for parallel relabel operations, relabels in our implementation are serial. The total time taken in the serial relabel operations is small in our experiments. The run time of the benchmarks we report for C-RACER *does not* account for the time taken for the relabel operations, which is a lower bound (Section 5.2). Note that our reimplementation can also differ in performance from the original implementation because of differences in the schedulers.

We reuse eighty unit test cases from the PTRacer artifact and designed new test cases to check the correctness of our FastTrack, FastRacer, and C-RACER implementations. The unit tests include both racy and non-racy programs, *with and without* locks. All the prototypes pass the unit tests. Our implementations are publicly available.[7]

5 Evaluation

This section compares FastRacer with the closest prior work, FastTrack [21], PTRacer [63], and C-RACER [58].

5.1 Experimental Setup

Benchmarks. We reuse twelve TBB-based applications used by PTRacer for our evaluation. These include four applications, blackscholes, fluidanimate, streamcluster, and swaptions, from the PARSEC benchmark suite [4], five geometry and graphics applications, convexHull, delRefine, delTriang, nearestNeigh, and rayCast, from the PBBS benchmark suite [56], and three applications, karatsuba, kmeans, and sort, from the Structured Parallel Programming book [35]. We left out the PARSEC application, bodytrack, because of a compilation error, and ignore the C-RACER benchmarks because they use Cilk-5 [58].

The benchmarks follow spawn-sync semantics where a child task joins with its immediate parent (async-finish semantics are more general) and do not use locks, so we were able to run C-RACER successfully for all the benchmarks.

Evaluation platform. The experiments execute on an Intel Xeon Gold 5218 system with one 16-core processor with hyperthreading disabled, 128 GB DDR4 primary memory, running Ubuntu Linux 20.04.3 LTS with kernel version 5.11.0.

5.2 Performance Results

Figure 5 reports the performance of C-RACER, PTRacer, and FastRacer for all the benchmarks (arranged alphabetically). Every bar averages ten trials and is normalized to the baseline, which runs the unmodified benchmarks without instrumentation. Smaller bars mean better run times. By default, the TBB scheduler creates c threads and multiplexes the tasks to the c threads, where c is the number of cores in the system. The results in Figure 5 are with 16 threads.

Our reimplementation of C-RACER incurs an overhead of 10.66X over the unmodified applications. The average performance slowdown incurred by PTRacer is 7.70X, while it is 6.41X for FastRacer. FastRacer shows substantial improvement for multiple benchmarks like convexHull, delTriang, fluidanimate, kmeans, and rayCast. The better performance of FastRacer is due to improved locality from vector clocks compared to cache-unfriendly tree traversals in C-RACER and PTRacer. On average, FastRacer outperforms both C-RACER and PTRacer by 1.66X and 1.20X, respectively.

We cannot directly compare C-RACER results to the original work [58] because of differences in the implementation, benchmarks, and evaluation infrastructure. However, we reemphasize that our C-RACER results do not include the cost of relabel operations. The original PTRacer work reports an average slowdown of 6.7X, compared to 7.70X in our experiments. In addition to the differences in the evaluation platforms and bug fixes, different execution times of the benchmarks in the absence of perfect scaling will lead to different relative overheads. We have verified that our modifications have minimal ($\leq 1\%$ difference) impact on the performance of PTRacer.
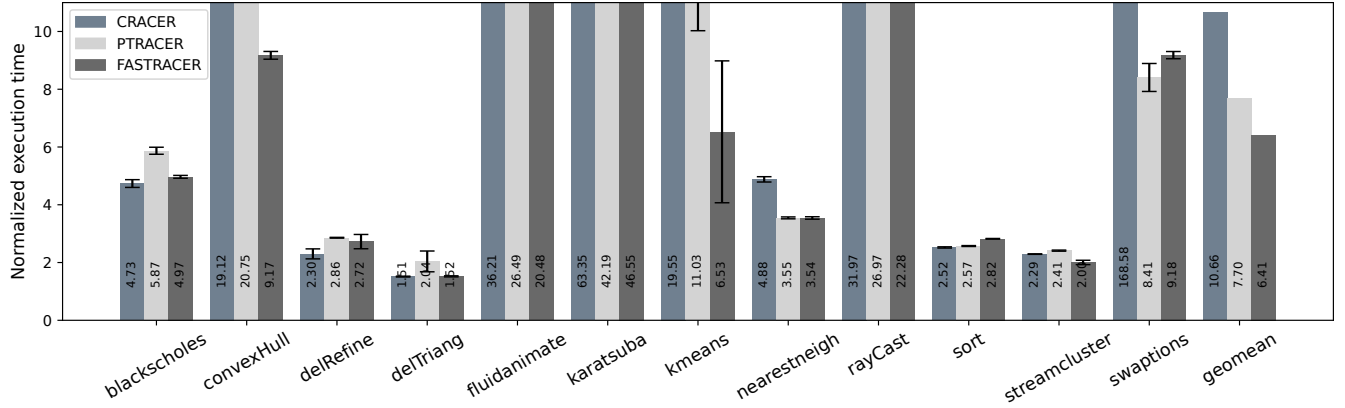
FastTrack successfully executed with four benchmarks that required less memory, blackscholes, fluidanimate, karatsuba, and sort, and got killed on the other benchmarks. The overhead of FastTrack for the four benchmarks is 50.26X, and FastRacer outperforms FastTrack by 4.62X. Given that FastRacer builds on FastTrack, this result shows that the task and variable vector clock optimizations proposed in FastRacer are effective in reducing both run time and space overheads.

Memory overhead. Table 1 compares the peak memory requirement of each benchmark with the four techniques, as reported by the Massif tool in Valgrind [39]. Column 2, *UM*, shows the memory requirement of the unmodified application, while *FT*, *CR*, *PT*, and *FR* stand for FastTrack, C-RACER, PTRacer, and FastRacer, respectively. The results show that using IVCs for encoding task inheritance in FastRacer compared to the fine-grained DPST structure in PTRacer provides significant memory savings in maintaining per-task metadata, especially for fluidanimate, karatsuba, kmeans, sort, and swaptions. C-RACER usually requires the least memory since it maintains order maintenance structures, but has high performance overhead compared to FastRacer.
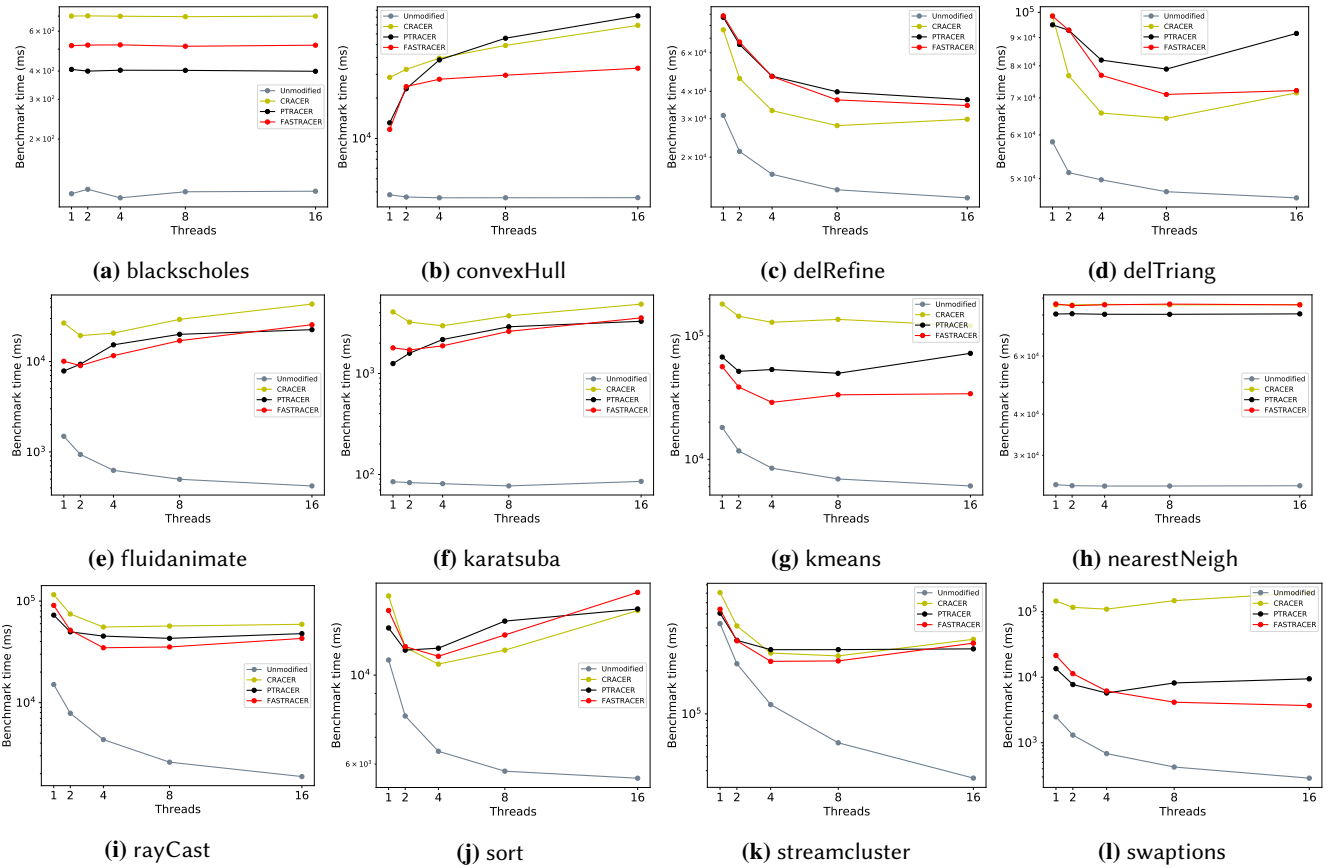
Figure 5. Performance comparison of the different techniques normalized to the unmodified execution time of the benchmarks.

(a) blackscholes   (b) convexHull   (c) delRefine   (d) delTriang

(e) fluidanimate   (f) karatsuba   (g) kmeans   (h) nearestNeigh

(i) rayCast   (j) sort   (k) streamcluster   (l) swaptions

Figure 6. Scalability results of the benchmarks on the Intel Gold platform described in Section 5.1.

Scalability. Figure 6 shows the scalability plots of the benchmarks as we vary the number of threads (in powers of two) used by the TBB scheduler. Other experimental setup are the same as in Figure 5. The *Unmodified* configuration in the figure shows that most applications scale well, excepting blackscholes, convexHull, and karatsuba. FastRacer scales better than PTRacer for delTriang, kmeans, and swaptions, for the

range of thread counts we have evaluated. The scaling behavior of C-RACER, PTRacer, and FastRacer are very similar for the remaining benchmarks.

Platform sensitivity. We evaluate the sensitivity of the optimizations by re-running experiments on an Intel Xeon Silver 4114 system with two ten core processors (twenty 2.0 GHz

	UM	FT	CR	PT	FR
blackscholes	0.62	9.64	10.38	54.78	48.03
fluidanimate	0.51	69.93	0.58	9.17	2.04
streamcluster	0.84	-	1.17	22.76	6.91
swaptions	0.19	-	0.98	17.34	3.87
convexHull	1.69	-	2.97	19.94	12.71
delRefine	3.71	-	6.25	125.37	125.39
delTriang	3.63	-	8.19	113.69	106.77
nearestneigh	2.19	-	5.60	106.86	125.26
rayCast	1.28	-	4.08	18.37	14.35
karatsuba	0.02	0.86	0.18	9.34	2.81
kmeans	0.11	-	2.52	15.82	5.99
sort	0.15	18.96	0.20	9.87	2.40

Table 1. Comparison of the memory overhead (in GBs).

	# Tasks ($\times 10^3$)	ACC ($\times 10^6$)		Data Races		
		RDs	WRs	CR	PT	FR
blackscholes	0.20	90	50	21	21	21
fluidanimate-r	1.60	26	0.7	40	40	40
streamcluster-r	180	363	13	80	80	80
swaptions	960	77	77	0	0	0
convexHull	8.50	30	0	0	0	0
delRefine	1000	15	0	0	0	0
delTriang	790	30	20	0	0	0
nearestNeigh	2800	51	8	0	0	0
rayCast	1900	160	0	0	0	0
karatsuba	1.98	3.4	0.8	0	0	0
kmeans-r	35	570	10	75	75	75
sort	0.70	11	0.06	1024	1024	1024

Table 2. Run-time statistics across different benchmarks.

cores in total) with hyperthreading turned off, 128 GB primary memory, running Ubuntu Linux 18.04.6 LTS with kernel version 4.15.0. The rest of the methodology is the same as Figure 5. C-RACER, PTRacer, and FastRacer incur overheads of 11.60X, 9.44X, and 6.85X, respectively. Although, the overheads on the multi-socket Xeon Silver platform are slightly greater compared to the Xeon Gold platform, the general trend is the same. FastRacer outperforms both C-RACER and PTRacer by 1.69X and 1.38X, respectively. The study confirms the effectiveness of the proposed optimizations *across* different platforms.

FastRacer outperforms prior work on the *same* set of benchmarks as used in PTRacer. Given the generic nature of the optimizations, we expect a similar qualitative trend for benchmarks where threads join with arbitrary ancestors (e.g., async-finish semantics). More importantly, FastRacer disproves the assumption made in *all* prior work that vector-clock-based analysis is not suited for task-based programs.

5.3 Data Races and Run-time Statistics

Table 2 summarizes the run-time statistics. The data is the average from 10 trials with a statistic-collecting configuration. Columns 2–4 in the table show the average number of tasks spawned by the benchmarks and the number of read and write accesses instrumented by the static compiler pass in LLVM. Columns 5–7 show the number of data races reported by the different tools. To stress-test the correctness of our implementations, we introduced data races in a few benchmarks that already did not have known races. The suffix "-r" denotes benchmarks that have been modified to introduce races for evaluation. All the tools are expected to report the same number of races for a given application with a fixed input. C-RACER (CR), PTRacer (PT), and FastRacer (FR) report the same violations for all the benchmarks. Please note that the evaluation includes our fixes to PTRacer (Section 4).

6 Related Work

In the following, we discuss other related work that has not already been discussed.

Race detection for task-based programs. Mellor-Crummey exploited the structural property of fork-join programs to show that tracking two readers and a single writer per memory location is sufficient for sound data race detection [36]. Since then, there has been much work to design race detection algorithms to utilize the serial-parallel (SP) structure of programs with constant space overhead for metadata [12, 19]. ESP-bags is an extension to SP-bags that supports the finish construct in async-finish programs [47]. However, these approaches constrain the program to execute serially in depth-first order, which does not scale. TARDIS does not keep track of the SP relationships among program strands [32]. Instead, TARDIS maintains log-based access sets and lazily detects races by checking for overlapping intersections of access sets of logically parallel sub-computations at join points.

Race detection for multithreaded programs. Static analysis can potentially detect all *feasible* data races across all possible executions (i.e., no false negatives), but usually do not scale to large programs and suffer from false positives, which developers loathe [7, 37, 38]. Dynamic analyses have the potential to be sound and precise for the *observed* executions. Many dynamic data race detection analyses track the happens-before relation to infer data races [9, 46, 54, 55, 60]. *Lockset* analysis reports data races when a locking discipline is violated, but can report false races [13, 41, 52, 59]. Hybrid techniques integrate both HB and lockset analysis [41, 65], but continue to suffer from the disadvantages of both techniques. Other techniques sacrifice soundness for performance by sampling memory accesses [5, 9, 17, 34] or require hardware support to speed up the race detection analysis [14,

44, 61]. Prior analyses have also explored detecting a subset of data races that arise due to conflicts among overlapping regions [6, 15, 33]. Data race detection analyses have also been proposed for parallel programming models such as OpenMP [2, 24] and GPUs [16, 26, 27].

Improve race detection coverage. Recent work has explored exposing as many true races as possible by observing one or a few dynamic executions. The idea is to explore different valid interleavings to maximize detecting data races that can occur across schedules. Many techniques perturb the execution in an attempt to break spurious HB relations [18, 25, 53]. *Predictive* techniques aim to detect data races that can occur in other correct reorderings of memory accesses by observing one dynamic execution. Such techniques use partial order relations that are weaker than HB to allow reconstructing other valid memory reorderings [29, 50, 51, 57].

7 Conclusion

Whereas prior work has overlooked the possibility of using vector clocks for task-based programs [48, 58, 63], FastRacer shows how to achieve competitive performance with a curated set of optimizations. FastRacer introduces novel optimizations that reduce the metadata redundancy and alleviate the performance bottlenecks with task vector clocks. FastRacer also exploits the structured execution of async-finish programs to limit the per-variable metadata overhead by using a coarse-but-efficient encoding of task inheritance relationships. FastRacer shows substantial performance improvements over FastTrack, and outperforms state-of-art approaches C-RACER and PTRacer. FastRacer's proposed vector clock optimizations allow for efficient dynamic data race detection for task-based async-finish programs.

Acknowledgments

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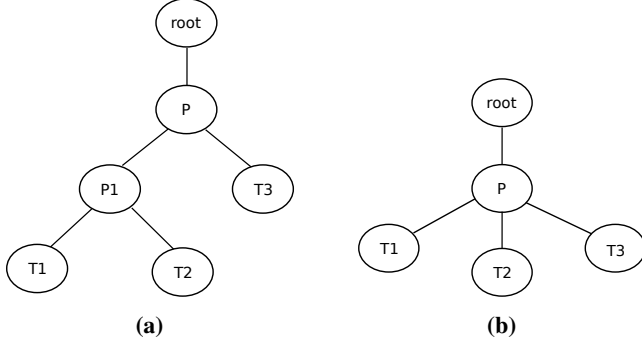
A Appendix

A.1 Correctness of FastRacer

Lemma A.1. *Storing access entries of only two tasks such that their LCA using the inheritance tree is the highest is sufficient. That is, a future access to the variable, which is racy with any of the existing parallel accesses, must be racy with any one of the two access entries with the highest LCA.*

Proof. Let tasks T1, T2, and T3 be three tasks that access shared variable var in parallel with the same lockset. Let the two tasks with the highest LCA in the inheritance tree be T1 and T2, their LCA be task P, and T3 be any task other than T1 and T2. All the parallel tasks, including T1, T2, and T3 must be immediate or recursive children of P, i.e., P is the common ancestor of all T1,T2 and T3. An immediate child means that the task has been spawned by P and a recursive child means that the task has been spawned by some other task which itself is an immediate or recursive child of P.

Let us assume that in the future, another task T accesses the shared variable var and the access is racy with task T3,

Figure 7. Different cases possible during LCA computation.

but not with T1 and T2. This implies the access to var by T *happens after* both T1 and T2. Since T1, T2, and T3 have the same lockset, and T is racy with T3, so the intersection of their locksets must be empty. This implies that we have two non-racy accesses from tasks T1 and T to var even when the accesses are not protected by the same lock. This can only happen if T1 and T are ordered by task management constructs. That is, one of the following must hold: (i) T1 accesses var, and then spawns T, either immediate or recursive, or (ii) T1 is present in joined of T. By a similar argument, one can draw a similar conclusion for T2, i.e., one of the following must hold: (i) T2 accesses var and then spawns T, either immediate or recursive, or (ii) T2 is present in joined of T.

Upon careful observation, one can see that constraints for T1 and T2 can hold simultaneously if and only if both T1 and T2 are present in joined of T. Other possibilities lead to contradictions. This can only happen if some common ancestor P' of tasks T1 and T2 calls join, in which all children tasks within join scope of task P' will join with it, and which then spawns task T copying joined from P' to T (P' can be T itself). Since tasks T1 and T2 have the highest LCA in the inheritance tree, and P' is the common ancestor of T1 and T2, P' must be the ancestor of T3 as well. Therefore, T3 will be under join scope of P' and so should be present in the joined of P' after join call, and therefore to task T joined as well, like T1 and T2.

Sice T3 would be present in joined of T, current access by T will have happens *after* relationship with T3's access and so would be non-racy. But we had assumed that T3 access is racy with current T access, leading to a contradiction. This proves our lemma that any future access to the variable, which is racy with any of the existing parallel accesses, must be racy with at least one of the two access entries with the highest LCA.

□

Lemma A.2. *The inheritance vector clock (IVC) correctly computes the two tasks with the highest LCA among three parallel tasks.*

Proof. Consider three parallel tasks T1, T2, and T3 in an inheritance tree (Figure 7). We need to consider the following two cases.

Case 1. LCA(T1, T2), LCA(T2, T3), and LCA(T1, T3) are the same (Figure 7a). Here, any pair of tasks chosen from the set {T1,T2,T3} will have same LCA, and so the claim holds.

Case 2. Without loss of generality, let LCA(T2, T3) be strictly higher than LCA(T1, T2) (Figure 7b). Let LCA(T1, T2) = P1 and LCA(T2, T3) = P. Then, P will be the ancestor of P1. By the structure of IVC, the IVC of a task contains the IVC of its ancestor as a prefix. So, the IVCs of tasks T1 and T2 will have the IVC of P1 as a prefix, and the IVC of tasks P1 and T3 will have the IVC of P as a prefix. The IVCs of these tasks are as follows:

- $IVC(P1) = IVC(P) + [a \ldots b]$
- $IVC(T1) = IVC(P1) + [x_1 \ldots x_n] = IVC(P) + [a \ldots b] + [x_1 \ldots x_n]$
- $IVC(T2) = IVC(P1) + [y_1 \ldots y_m] = IVC(P) + [a \ldots b] + [y_1 \ldots y_m]$
- $IVC(T3) = IVC(P) + [z_1 \ldots z_m]$

Here, $x \ldots y$ represents an array of clock values and $IVC(X)$ represents inheritance vector clock of task X. Since, LCA(T2, T3), i.e., P is strictly higher than LCA(T1,T2) i.e., P1, $IVC(P)$ cannot be equal to $IVC(P1)$ and so $[a \ldots b]$ cannot be empty. Also, either $[z_1 \ldots z_m]$ is empty (i.e., P and T3 are the same) or $z_1 \neq a$, otherwise P cannot be the LCA of T2 and T3.

While comparing the IVCs of tasks T1, T2, and T3, the first point of difference is after $IVC(P)$. If $[z_1 \ldots z_m]$ is empty, then the IVC of T3 will end first and so Fast-Racer will choose T3 and any one of other two tasks (say T2). Otherwise, we will have z_1 in $IVC(T3)$ and a in $IVC(T1)$ and $IVC(T2)$. Since $z_1 \neq a$, the first point of difference has T3's clock value as different. So, again FastRacer will choose T3 and any one of other two (say T2). In both cases, FastRacer chose T3 and T2 out of the three tasks. Since IVC(T2,T3) = P is the highest LCA across all tasks in the set {T1,T2, T3}, so the claim holds.

The tasks T1, T2, and T3 can be chosen randomly, and the above cases allow for any possible permutation.

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