Model-Based Performance Analysis of the HyTEG Finite Element Framework

Dominik Thönnes dominik.thoennes@fau.de Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU) Chair for System Simulation Erlangen, Germany

Ulrich Rüde ulrich.ruede@fau.de Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU) Chair for System Simulation Erlangen, Germany **CERFACS** Toulouse, France

about the actual performance of the code and can even be misleading since a slow code will typically scale quite nicely. The reason is

that if shared resources are only utilized to a minor extent, there

are more reserves for parallel execution. If the shared resources are

already highly utilized by a sequential program, achieving good

scaling is harder. This paper lays out the basis for performance

engineering by thoroughly analyzing the computational kernels of

the HyTEG [13] simulation framework, specifically looking at the

ABSTRACT

In this work, we present how code generation techniques significantly improve the performance of the computational kernels in the HyTeG software framework. This HPC framework combines the performance and memory advantages of matrix-free multigrid solvers with the flexibility of unstructured meshes. The PYSTENCILS code generation toolbox is used to replace the original abstract C++ kernels with highly optimized loop nests. The performance of one of those kernels (the matrix-vector multiplication) is thoroughly analyzed using the Execution-Cache-Memory (ECM) performance model. We validate these predictions by measurements on the SuperMUC-NG supercomputer. The experiments show that the performance mostly matches the predictions. In cases where the prediction does not match, we discuss the discrepancies. Additionally, we conduct a node-level scaling study which shows the expected behavior for a memory-bound compute kernel.

CCS CONCEPTS

• Computing methodologies → Modeling and simulation.

KEYWORDS

Analytical Performance Modeling, Code Generation, Stencil Codes, Matrix-Free

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INTRODUCTION AND METHODOLOGY

This article will deal with the question: How do we determine the performance of a program? This question has no straightforward answer, but the answer is rather manifold. In high-performance computing (HPC), the relevant metrics are single-core performance and multi-core performance or scaling. These aspects must be considered in combination because looking only at scaling tells little

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Sparse Matrices

single-core performance.

Operations on matrices are a fundamental building block in numerical algorithms, and they often form the basis for solving computational problems where matrices with huge dimensions can be involved. Generally, a matrix is a rectangular array arranged in rows and columns. These dense matrices quickly reach the memory limits. For example, if a problem consists of 10⁸ unknowns, a dense matrix that describes the connection between these points would reach a size of $10^8 \cdot 10^8 * 8 B = 80 PB$, which is more than any supercomputer can provide. Sparse matrices form an important subclass when most elements are zero. This sparsity is exploited by omitting the zero entries when storing the matrix, which can dramatically reduce the amount of memory required. The simplest version uses a list where each element contains the row, column, and value of a matrix entry (Coordinate list (COO)). The memory footprint can be further optimized using a compressed format like the compressed row storage (CRS)[5] format. The CRS uses a list to store the column indices of each matrix entry in the matrix. The row indices of the matrix entries are not stored explicitly but only at the start of a new row in the column list. The memory required for the column is reduced from #matrix entries to #matrix columns using the compressed format.

1.2 Hybrid Tetrahedral Grids

The HyTeG software framework was developed in the TERRANEO project [7] as successor of HHG [9]. The fundamental concept is to use an unstructured grid of triangles or tetrahedra and perform a uniform grid refinement in each of these. This concept combines the advantages of unstructured grids for mesh flexibility and structured grids for performance. The refinement process leads to a structured grid within each triangle. Figure 1 illustrates the process with Figure 1a showing the initial mesh and Figure 1b the mesh after two refinement steps.

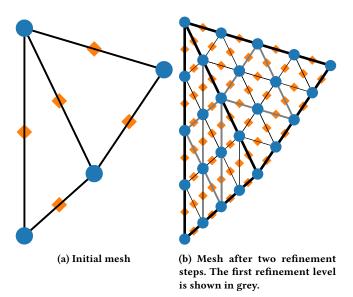


Figure 1: Refinement process for a mesh consisting of two triangles. Degrees of freedom are shown as blue circles on vertices and orange rectangles on edges.

This structure enables the usage of matrix-free methods and provides a natural basis for multigrid methods. As in multigrid terminology, we refer to the meshes obtained from the refinement steps *levels*. For example, a grid on level five is constructed by performing five refinement steps. In this article, we focus on two-dimensional grids only, even though HyTeG is capable of three-dimensional computations as well.

The framework utilizes degrees of freedom (DoF) located on the vertices and the edges of the triangles. Figure 1 shows blue circles for DoF located at the vertices and orange diamonds for DoF at the edges. This arrangement allows, for example, to use finite elements with a \mathbb{P}_1 or \mathbb{P}_2 discretization.

One technical detail worth mentioning here is that the connection to all neighbors is alike in the case of DoF located at the vertices. This is not the case for DoF located at the edges. In contrast, there are three groups for each side of the triangle. We refer to these groups as X, Y, and XY, as shown in Figure 2. The connections to the neighboring DoF are again the same within one of these groups. These connections are also known as *stencils*, which contain the corresponding weights to couple one DoF to its neighbors. In an *unstructured grid*, these stencils are typically different from each other. A structured grid is created within each triangle by using regular refinement.

The similarity within each group of DoF means that the stencils, i.e. the matrix rows, are also identical for each group. Therefore, only four individual stencils are needed within each triangle, one for the vertex DoF and one for each of the different groups of edge DoF. In contrast to a matrix that explicitly describes and stores the connections between all DoF, a so-called *matrix-free* storage is naturally obtained when each stencil is constant.

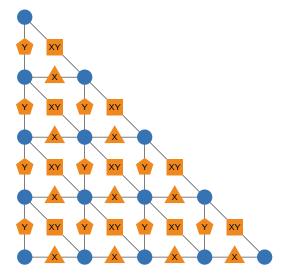


Figure 2: Grouping of degrees of freedom. Each type has exactly the same neighborhood except for the boundaries

1.3 Execution-Cache-Memory Model

This part introduces the performance model used in Section 5. For additional information, see, e.g., [18]. The ECM model can be viewed as an extension of the Roofline model [20], which similarly uses the principle that the execution speed of a program can be limited by either data transfer or the execution of operations. Both models also assume that these two limiting factors perfectly overlap, meaning data transfer does not influence the execution and vice versa.

In contrast to the Roofline Model, the ECM model uses processor cycles as a time unit, which has the advantage that the predictions are mostly independent of the processor frequency. Additionally, the model can take overlapping and non-overlapping parts into account, which is essential to predict in-core execution times.

In-core describes the actual computation in the processor and the loads and stores to and from the registers but leaves out the transfers within the caches. The in-core contribution is split into two parts: The first one is called T_{OL} , which is short for $T_{OverLapping}$ since the computation itself does fully overlap with data transfers. The loads and stores from and into the registers, however, do not overlap with cache transfers and are therefore named T_{nOL} for $T_{nonOverLapping}$. To determine T_{nOL} and T_{OL} , the Intel Architecture Code Analyzer (IACA) [11] can be used. This tool analyses the kernel's C++ source code or assembler code and predicts the execution happening within the CPU.

The transfers between the cache levels are also accounted for as T_{data} . Splitting T_{data} into different parts for each interface between two adjacent cache levels or the main memory which leads to, e.g., $T_{data} = T_{L1L2} + T_{L2L3} + TL3MEM$ for a CPU with three levels of caches. The unit for data transfer used by the ECM model is typically one cache line (CL) since this is the smallest data unit that can be transferred in the caches. One CL on modern Intel CPUs has a size of 64 B. A work unit is used for the computation, which includes all the instructions necessary to process all elements in one CL.

load streams	store streams	bandwidth	cycles per cache line
1	1	70 GB/s	2.5
3	1	87 GB/s	2.0
1	3	60 GB/s	2.9

Table 1: Bandwidth of different kernel using the Intel Skylake Xeon Platinum 8174 CPU at 2.7 GHz.

For example, eight iterations would be used as a work unit if an analyzed loop adds two vectors using double-precision elements. This assumes the typical double-precision element size of 8 B, which means eight elements are contained in one CL.

The ECM is often displayed in a short form:

 $T_{OL}||T_{nOL}|T_{L1L2}|T_{L2L3}|T_{L3MEM}$

The prediction for the case that the dataset fits into a certain cache level or the main memory is determined by adding up the respective transfer time. For example, if the data is in the L3 cache: $T_{nOL} + T_{L1L2} + T_{L2L3}$. The actual prediction is the maximum of T_{OL} and the sum of the data transfers.

A crucial tool when modeling performance is the so-called *layer* condition (LC) [18], which predicts the caching behavior of stencil codes. These kernels typically apply the stencil at each grid point inside loops that span all dimensions. Each iteration updates points by accessing various neighbors. In a two-dimensional grid, the points are typically sequential in memory for one dimension, but there are offsets in the other. An earlier iteration might have accessed some of the neighboring points already, which means these points might still be present in the cache. At least one point of the stencil has never been accessed before and is loaded for the first time. The vertical distance of the stencil also called the height, defines how many rows of the grid array are required to apply the stencil. If we assume sequential memory in the horizontal direction, a stencil that accesses the top and bottom neighbor has a height of three rows. The layer condition states that if the height of the stencils times the memory for one row is smaller than the cache size, then only the elements that have never been accessed are cache misses.

1.4 Hardware Description

Throughout this article, we will use an Intel Skylake Xeon Platinum 8174 CPU, as it is currently used in the SuperMUC-NG [15] supercomputer. This CPU supports both a 205 W and 240 W operational TDP mode. For SuperMUC-NG, the TDP is set to 205 W, which results in a nominal CPU frequency of 2.7 GHz.

On the Skylake architecture, one can use Advanced Vector Extensions 2 (AVX2) instructions, which means that the equivalent of four mul or add instructions can be executed in a single instruction when using double precision. Furthermore, fused multiply-add instructions (FMA) are also available, which would also execute the AVX mul and AVX add in the same instruction. The Skylake architecture can perform two FMA AVX (vfmadd*)instructions per cycle [1]. It is worth noting that AVX-512 is also supported, but the clock frequency will be reduced when using AVX-512-enabled code. This leads to the fact that mainly kernels that are bounded by the computation and not the data transfer will benefit. Since this is not the case for the kernels analyzed in this paper, AVX-512 does not yield a performance benefit and is, therefore, not enabled.

cache line size	64 B
L1 cache size	32 KiB (per core)
L2 cache size	1024 KiB (per core)
L3 cache size	33 MiB (shared)
Main Memory	96 GB
Clock Speed (fixed)	2.7 GHz
Cores	24
Bandwidth L1 \leftrightarrow L2	64 B/cy (half-duplex)
Bandwidth L2 \leftrightarrow L3	16 B/cy (full-duplex)

Table 2: Intel Skylake Xeon Platinum 8174 CPU specification and cache characteristics that are used as a basis for the performance modeling. For half-duplex, only one direction at a time can achieve the maximal bandwidth, while full-duplex can use maximal bandwidth in both directions simultaneously.

Several tests were conducted on the main memory bandwidth using the LIKWID tool suite. The results for different combinations of load and store streams are presented in Table 1. It is important to note that the number of streams is the actual number of streams from an application point of view. This implies that the store stream also includes one load stream for write-allocate.

In contrast to the roofline model, the ECM also requires the quantities of transfers between the caches. Table 2 lists some of the relevant specifications of this processor and the cache-hierarchy characteristics that are used as a basis for the performance modeling.

For the bandwidth of the caches, *half-duplex* and *full-duplex* mean that the cache can either read or write (half-duplex) or that both can happen simultaneously (full-duplex). In the latter case, if reading and writing co-occur, the actual bandwidth would be $2 \cdot 16$ B/cy. Normalized to one CL, which has 64 B, it takes one cycle to transfer between L1 and L2 and four cycles between L2 and L3.

In addition to the transfers between different cache levels, the bandwidth between the L3 cache and the main memory is required. To calculate the cycles it takes to get one CL from L3 cache to memory, the bandwidths from Table1 are used and converted. For one load and store stream for example this reads (64 B \cdot 2.7 GHz)/70 GB/s = 2.47 cy.

1.5 Outline

The target application in developing HyTeG is simulating convection in the outer earth mantle. This can be modeled by a buoyancy-driven convention in Stokes flow. Section 2 shows a simple example of this application.

As mentioned before, the possibility to use matrix-free methods is one of the defining features of HyTeG. A general comparison of matrix-free vs. sparse matrix methods is drawn in Section 3, as well as some experiments comparing HyTeG with the popular scientific software suite PETSc [3, 4] regarding memory consumption.

To combine the benefits of maintainability and performance HyTeG uses code generation for computationally intensive kernels. The process of how these kernels are created and integrated is described in Section 4.

In Section 5, the Execution-Cache-Memory (ECM) model [19, 10] is used to analyze the performance of the kernels in HyTeG that execute the matrix-vector multiplication.

Finally, an intra-node scaling experiment of the investigated kernel is shown in Section 6, followed by the conclusion and outlook in Section 7.

2 PLUME IN RECTANGULAR DOMAIN

To demonstrate the capabilities of the HyTEG software framework, we show the simulation of buoyancy-driven convection in Stokes flow, which is described by an advection-diffusion problem. We use Taylor-Hood ($\mathbb{P}_2\mathbb{P}_1$) elements for the discretization of the convection and a particle-based characteristics method for the advection. [12] presents details about the particle-based characteristics method and its solvers. The convection is solved using a MINRES ([16]) solver, which is easier to compare to PETSc than a more complex multigrid solver. Figure 3 shows a visualization of the simulation for different time steps. To obtain a baseline for the performance analyses, we profiled the application on refinement level eight with our naïve C+ version of the kernels without using the generated kernels described in Section 4. The total number of DoF is $1.1 \cdot 10^6$ in this example application. When looking at the MINRES solver used to solve the convection, the matrix-vector multiplication accounts for over 57 % of the runtime, which makes it a good candidate for optimization.

3 COMPARING MATRIX-FREE AGAINST SPARSE MATRIX METHODS

This section analyzes the performance benefits of matrix-free methods against sparse-matrix methods based on the two-dimensional HyTeG grids described in Section 1.2. A sparse matrix format stores all entries of the matrix except the ones that are zero. Additionally, the positions of the entries in the matrix are also stored. On the other hand, matrix-free methods do not store the entries, drastically reducing memory usage and therefore increasing the performance. Each row of the matrix describes the connection to the neighbors by storing a factor for each neighboring point. When updating a point, the corresponding sparse matrix row has to be loaded. Depending on the matrix's size, the data transfers occur from the caches or the main memory. Due to the regular refinement in HyTeG as described in Section 1.2, the rows representing the points inside one of the triangles are identical. In matrix-free methods, the row is often referred to as stencil and the factors as weights. If the stencil weights are constant, they can reside in the registers or the cache, resulting in the advantage in memory transfers mentioned above. However, if the weights vary, using matrix-free methods is more complex. It is still possible to compute the weights on the fly to reduce the memory transfers, but this introduced computational overhead compared to non-matrix-free methods. The number of floating-point operations that need to be performed is identical. Therefore, this aspect is neglected in our analysis. At first, we analyze the differences theoretically, where the data volume for matrix-free and non-matrix-free variants is determined and compared. In the second step, a benchmark application compares the actual HyTeG routines against PETSc, one of HPC's most popular libraries for matrix operations.

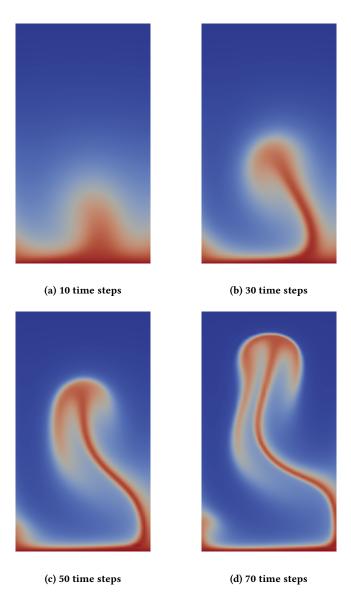


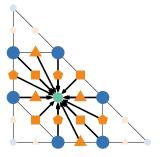
Figure 3: Buoyancy-driven convection in Stokes flow discretized with Taylor-Hood ($\mathbb{P}_2\mathbb{P}_1$) elements and a particle-based characteristics method.

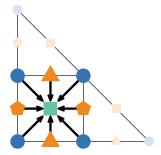
3.1 Theoretical analysis

Since HyTeG performs a regular refinement inside each element, the total number of DoF can be determined depending on the refinement level. The number of DoF that are located on the vertices of the grid is

$$\#vertex = \frac{(2^l + 1) * (2^l + 1 + 1)}{2}$$

where l is the refinement level. Figure 1 shows an example mesh for refinement levels zero and two. This is slightly different for the DoF located at the edges. Due to the regular refinement, the edges can be grouped into three different orientations. Each orientation





(a) Stencil for one vertex depending on vertices and edges

(b) Stencil for one group of edges (XY) depending on vertices and edges

Figure 4: Stencils for the vertices and one group of edges. The other edge groups have the same number of neighbors or stencil weights.

corresponds to one side of the original triangle as shown in Figure 2. Each of the three orientations can be treated identically and named X, Y, and XY in this paper. The number for **one single** orientation (*x* in this case) is

$$\#edge = \frac{(2^l)*(2^l+1)}{2}$$

. Since there are three types of edge orientations, the total number of DoF, including edges and vertices, is:

$$#dof = #vertex + 3 \cdot #edge$$
.

As stated, #dof is the same for matrix-free and non-matrix-free algorithms. The difference between the two occurs when considering the stencil weights. Figure 4 shows the stencils for a vertex (4a) and the XY group of edges (4b). To get the total number of stencil entries, one has to sum up all stencil weights corresponding to the neighboring vertex and edge DoF. For the DoF located at the vertices, this sums up to 19 entries. Seven correspond to the neighboring vertices (including the center), and twelve correspond to the adjacent edges of various groups. In the case of DoF located at the edges, four neighboring vertices and four adjacent edges must be considered. The entries sum up to a total number of nine stencil weights, including the edge itself.

Table 3 displays the required memory for a single triangle after ten refinement steps, as one example. The calculations neglect the domain boundary where the stencils are not fully populated and assume double precision entries with a size of 8 B.

When summing up the stencil entries, this means that for storing the matrix $80.0\,\text{MiB} + 113.4\,\text{MiB} = 193.4\,\text{MiB}$ are needed. Additionally, the position of each stencil entry in the whole matrix needs to be stored. A compressed format is often used in scientific computing to reduce the memory footprint of sparse matrices. When using a compressed row or column format, the additional data is one index for each element and one for each row/column in the matrix. Using 32-bit integers this leads to $193.4\,\text{MiB} \cdot 0.5 = 96.7\,\text{MiB}$ and $16.8\,\text{MiB} \cdot 0.5 = 8.4\,\text{MiB}$ of additional indexing memory. In summary, the storage needed for the whole matrix is $298.5\,\text{MiB}$. The source and destination vectors allocate $16.8\,\text{MiB}$ each. The total memory footprint for the matrix-vector multiplication with non-matrix-free

#vertex #edge #dof			= =	525825 524800 2100225
dof_mem vertex_mem edge_mem	= = =	8 B · #dof 8 B · 19 · #vertex 8 B · 9 · 3 · #edge	= = =	16.8 MiB 80.0 MiB 113.4 MiB
memory mat-vec sparse matrix			332.1 MiB	
memory mat-vec theoretical matrix-free memory mat-vec HyTeG implementation				33.6 MiB 67.2 MiB

Table 3: Required memory for degrees of freedom and stencils if a uniform refinement is applied ten times (refinement level 10). $vertex_mem$ refers to the memory required to store all vertex stencils and $edge_mem$ to store all edge stencils, respectively.

matrix storage is, therefore, 332.1 MiB. In comparison, a matrix-free algorithm only requires the source and the destination vector, i.e., 33.6 MiB. Therefore the sparse matrix needs a factor of $\frac{332.1}{33.6} = 9.9$ more memory in this scenario.

3.2 Comparing implementations

In this part, we compare the PETSc library, which assembles the full matrix, against implementing a matrix-free algorithm in the HyTeG framework. This naïve implementation in HyTeG is optimized for usability, using various abstractions provided by modern C++ programming capabilities. It is not optimized to reach the highest possible performance but primarily to use a matrix-free structure.

One specialty about the implementation in HyTeG is that the matrix-vector multiplication for discretizations that involve DoF at vertices and edges is split into four different kernels. Each of these kernels handles a different combination: vertex to vertex, edge to vertex, vertex to edge, and edge to vertex. Using these different kernels was the most straightforward approach when moving from vertex-only meshes to meshes that support DoF at the vertices and the edges. One possible optimization is merging the four kernels into one to reduce the number of data streams. Because HyTeG splits the matrix-vector multiplication into four parts, the memory has to be loaded multiple times. In Figure 4, this separation can be recognized by the difference in color. Figure 4a and Figure 4b shows two kernels each. One kernel considers only the blue vertices, and the other only the orange edges. All kernels update the green points.

Both the DoF located at the vertices and the DoF situated at the edges must be loaded two times and stored two times. This amounts to $4 \cdot 16.8 \text{ MiB} = 67.2 \text{ MiB}$. Therefore, the expected difference is not a factor of 9.9 as derived in Section 3.1 but rather $\frac{332.1}{67.2} = 4.9$.

To confirm the calculations, we used LIKWID to measure the main memory volume during the execution of the application. The main memory volume denotes the amount of memory loaded from and stored to the main memory during the computation. Ideally, one would instead measure the peak amount of memory allocated instead of the total volume transferred during the execution. However, measuring the process's peak amount of memory allocated is a

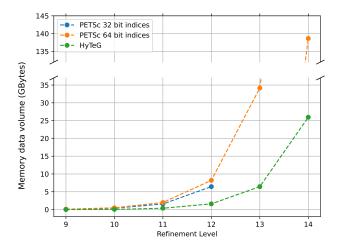


Figure 5: Memory data volume for the matrix-vector multiplication of HyTeG and PETSc for different refinement levels. Note that PETSc with 32-bit indices can only run up to refinement level 12. The difference converges to a factor of ≈ 5 as expected.

nontrivial task. There are different methods like the Linux function getrusage, internal methods of the PETSc library, or external tools like Valgrind¹. Our experiments with these tools showed inconsistent measurements, especially for applications with a relatively small memory footprint of a few hundred megabytes. Therefore, we measured the memory volume instead of the peak amount of memory. Since the goal is to compare PETSc and HyTEG, this method is well suited.

In the benchmark application, HyTeG first sets up the stencils and then transforms them into a PETSC matrix stored in a compressed format. In the next step, the application performs a matrix-vector multiplication using the PETSc sparse-matrix and the HyTeG stencils while measuring the memory volume for both operations separately. Figure 5 shows the difference between the two implementations. One interesting fact is that if PETSc is built with 32-bit integers, it can only be used up to refinement level 12 since, at refinement level 13, there are more entries in the matrix than 2^{32} . Using 64-bit integers for indices further increases the memory footprint of PETSc. Finally, above refinement level 14, the total memory limit of the system is reached with PETSc while HyTeG can utilize two steps more. This shows that HyTeG is capable of performing a matrix-vector multiplication with up to $8.6 \cdot 10^9$ DoF on a system with 96 GB.

In summary, the benchmark application confirms the theoretical advantages of matrix-free methods concerning memory usage. Since, in our case, the matrix-vector multiplication is memory bound, the performance is cross-checked by measuring the memory bandwidth and comparing it to the maximal memory bandwidth achievable. The analysis with the LIKWID tools revealed that the abstract C+ implementation on refinement level 12 only achieves \approx 12.5 GB/s. This bandwidth is far from the theoretical maximum, as

shown in Table 1. The following section explores how this gap can be closed using code generation to optimize performance.

4 CODE GENERATION

This section will introduce how code generation is used to generate highly performant compute kernels from abstract C+ code. The following shows a pseudo version of the abstract C+ kernel for the matrix-vector multiplication kernel that couples the DoF located at the vertices:

Code generation can be used in various ways to aid software development. The idea is generally to specify the problem in an abstract and often simpler and more compact form. Code generation allows for faster development and reduces the risk of errors since less code must be developed and maintained. Another advantage is that with a general problem specification, the generation framework can produce code adjusted to the targeted hardware architecture and take advantage of its specific features.

In HYTEG, we utilize code generation only for the time-consuming parts of the code in contrast to other approaches in which the whole framework, including the data structures, is generated. The Exastenicls framework [14] employs whole program generation using a domain-specific language to generate advanced multigrid solvers. Other examples are the FEniCSx [17] and the Firedrake [8] projects, which generate code for the solution of partial differential equations using the finite element method.

For the generation of the compute kernels, we use the PYSTENCILS [6] code-generation framework, which utilizes an embedded DSL in Python. The general idea is to specify a stencil-based interpretation of the compute kernels and automatically transfer these to highly optimized C+ code. PYSTENCILS uses and extends the computer algebra package SYMPY such that stencil kernels can be formulated symbolically. The framework can then transform the symbolic representation into an abstract syntax tree (AST), a tree representation of the code structure. Based on the AST, PYSTENCILS performs various optimizations, such as eliminating common subexpressions. Finally, PYSTENCILS renders the AST into compilable C+ source code. It is worth mentioning that other backends are also available to generate source code for different hardware like GPUs. Once the desired C+ functions are generated, these can replace the original abstract C+ functions in the HyTeG framework.

The following shows an example of the PYSTENCILS code to generate the kernel, which handles the matrix-vector multiplication for the DoF located at the vertices. Additionally, the resulting C+code is shown to demonstrate the usefulness of PYSTENCILS. In contrast to the Python code, which is relatively easy to read, the C+ kernel is highly error-prone, especially concerning indexing.

¹https://valgrind.org/

```
triangle_source = VertexTriangleField('triangle_source',
         const=True)triangle_destination =
        VertexTriangleField('triangle_destination')
  vertex_to_vertex_stencil = StencilField('vtv',
        vertex_stencil_layout)
  level = 10
4 neighbors = list()
  for direction in vertex_stencil_layout:
       neighbors.append(vertex_to_vertex_stencil[direction]
        * triangle_source(direction))
   update = sympy.Eq(triangle_destination((0, 0)), sum(
        neighbors))
kernel = create_kernel('kernel', [update], level)
  print(generate_c_code(kernel))
  void kernel(double * _data_triangle_destination, double const * const
        _data_triangle_soucrce, double const * const _data_vtv)
  const double xi_0= _data_vtv[2]; const double xi_1= _data_vtv[5]; const double
        xi_2 = _data_vtv[0]; const double xi_3= _data_vtv[3];
  const double xi_4= _data_vtv[6]; const double xi_5= _data_vtv[1]; const double
        xi_6= _data_vtv[4];
   for (int ctr_2 = 1; ctr_2 < 1024; ctr_2 += 1) {
   for (int ctr_1 = 1; ctr_1 < 1024 - ctr_2; ctr_1 += 1) {
   const double xi_10 = xi_0*_data_triangle_source[ctr_1 + 1026*ctr_2 - ((ctr_2*(
        ctr_2 + 1)) / (2)) - 1];
   const double xi_11 = xi_1*_data_triangle_source[ctr_1 + 1026*ctr_2 - (((ctr_2
        + 1)*(ctr_2 + 2)) / (2)) + 1025];
    const double xi_12 = xi_2*_data_triangle_source[ctr_1 + 1026*ctr_2 - ((ctr_2*(
        ctr_2 - 1)) / (2)) - 1026];
   const double xi_13 = xi_3*_data_triangle_source[ctr_1 + 1026*ctr_2 - ((ctr_2*(
        ctr_2 + 1)) / (2))];
   const double xi_14 = xi_4*_data_triangle_source[ctr_1 + 1026*ctr_2 - (((ctr_2
        + 1)*(ctr_2 + 2)) / (2)) + 1026];
   const double xi_15 = xi_5*_data_triangle_source[ctr_1 + 1026*ctr_2 - ((ctr_2*(
        ctr_2 - 1)) / (2)) - 1025];
   ctr_2 + 1)) / (2)) + 1];
   _data_triangle_destination[ctr_1 + 1026*ctr_2 - ((ctr_2*(ctr_2 + 1)) / (2))] =
     xi_10 + xi_11 + xi_12 + xi_13 + xi_14 + xi_15 + xi_16;
16
  333
```

5 PERFORMANCE MODELING

5.1 Experiment Description

The profiling in Section 2 revealed that the matrix-vector multiplication is the one part of the code that consumes most of the time, which is often the case in numerical simulation codes. In this section, we only focus on the matrix-vector multiplication analyses. However, HyTeG also applies code generation to other operations like vector addition or smoothers in the context of multigrid. HyTeG uses functions and operators as basic build blocks. A matrix-vector multiplication is equivalent to applying an operator to a function. Therefore, the matrix-vector multiplication is also referred to as apply in this publication. In our implementation, the matrix-vector multiplication consists of four different kernels, as explained in Section 3.2. Each kernel deals with a different combination of vertex and edge DoF. Therefore, the resulting kernels are

- Vertex-to-Vertex(Figure 6a),
- Edge-to-Vertex (Figure 6b),
- Vertex-to-Edge (Figure 6c),
- Edge-to-Edge (Figure 6d).

Each of these kernels is analyzed separately in the corresponding section. When iterating, we start at the lower left (the 90-degree angle of the triangle), and the horizontal direction (X) is the inner loop. These kernels do not update the DoF located on the boundaries. The boundary points are handled by dedicated interface primitives

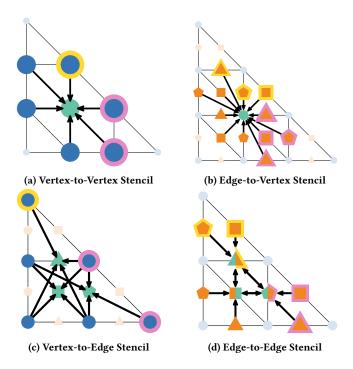


Figure 6: The four stencils involved in the matrix-vector multiplication. The borders describe the availability in the cache

No borders: the entry was used in the last iteration and is still in the L1 cache.

Yellow: the entry was never loaded before.

Pink: the entry was used in a former iteration and might still be in the cache.

```
dstVertex[y][x] =
    srcVertex[y-1][x+1] * c0 + srcVertex[y ][x+1] * c1 +
    srcVertex[y-1][x ] * c2 + srcVertex[y ][x ] * c3 +
    srcVertex[y+1][x ] * c4 + srcVertex[y ][x-1] * c5 +
    srcVertex[y+1][x-1] * c6
```

Listing 1: Vertex-to-Vertex kernel

as explained in [13]. We chose a minimum refinement level of seven to guarantee at least 100 entries in the longest row. Otherwise, the loop overhead is observable, and the performance is limited.

5.2 Vertex to Vertex Kernel

The kernel that couples vertex and vertex DoF is analyzed first and is shown in Listing 1. It is similar to a 9-point stencils kernel which contains all direct neighbors in two dimensions, including the diagonal ones. The only difference is that the top right and bottom left entries are missing due to the triangular mesh. Figure 6a shows the stencil pattern.

Table 2 describes the Intel Skylake architecture for which the kernel is analyzed. As described in Section 1.3, the basic units in the ECM model are cache lines (CLs). We must determine the work unit, meaning how many operations are executed for data in a single CL. The Skylake CPU has a CL size of 64B on all cache levels. If

LC	levels	ECM model cycles	prediction cycles	prediction Gflop/s
L1	7-10	{10 8 3 8 -}	{10]11]19]-]}	14.8
L2	11-14	{10 8 5 8 5.0}	{10]13]21]26]}	10.8

Table 4: ECM model for the Vertex-to-Vertex kernel. ECM model and prediction are stated in CPU cycles (cy).

double precision (8 B) is assumed, one work unit performs eight kernel iterations.

In the scalar case, the kernel executes seven multiplications and six additions for each iteration. For a work unit of eight iterations, this leads to (7+6)*8=104 operations. One AVX instruction operates on a vector length of 32 B, equivalent to four doubles. Therefore, 14 FMA AVX instructions are needed to process one work unit iteration and $T_{OL}=7cy$. However, these are only theoretical numbers that do not consider the CPU's hardware features, like the port utilization. To obtain more realistic numbers, we use the IACA[11] tool, which reports that it takes 10 cy to execute one work unit. The CPU can sustain two AVX load and one AVX store per cycle, and the kernel needs 14 AVX LOADs and two AVX STOREs, which leads to $T_{nOL}=7cy$. Again, using IACA shows that practically 8 cy are needed.

Next, the data transfer is analyzed. For the target array dstVertex, two CL transfers are needed throughout the whole memory hierarchy since every store miss leads to a write-allocate. We assume that the array entries a[x-1][y+1], a[x-1][y], a[x][y] and a[x][y-1] are in the L1 cache since they have been used in the previous iteration. These three entries are shown in Figure 6a without a border and contribute only to T_{nOL} . The entry a[x][y+1] (yellow border in Figure 6a) must always be loaded from the lowest memory level. Up to this point, there are two CL loads and one CL store for each work unit. Since the connection between the L1 and L2 cache has a half-duplex bandwidth of 64 B/s, it takes three cycles to transfer three cache lines ($T_{L1L2} = 3$ cy). For the transfer between L2 and L3, only the two cache line loads are considered since the store happens simultaneously due to full-duplex. With the given bandwidth of 16 B/cy this results in 8 cycles ($T_{L2L3} = 8$ cy).

The analysis for the remaining entries a[x+1][y] and a[x+1][y-1] is more complex since it depends on the size of the leading dimension and whether these entries are still in the cache. The LC, as described in Section 1.3, can determine the cache behavior. In this case, if three successive rows of the array can reside in a particular cache level, the LC for that cache level is fulfilled. Otherwise, the lower levels in the memory hierarchy have to be accessed. For a certain cache level k, a number of entries n and the cache Size C_k , this condition is $(3+1) \cdot n \cdot 8B < C_k$. We add one line to account for the target array dstVertex. To simplify the calculations, we ignore that the row size decreases by one with each outer iteration.

The hierarchy of the HyTEG grids allows only for a finite set of array lengths depending on the level of refinement. Therefore we can determine for which cache level the LC is fulfilled for a particular refinement level.

Table 4 shows the ECM model for different refinement levels. If the level is below eleven, the LC for the L1 cache is fulfilled, and

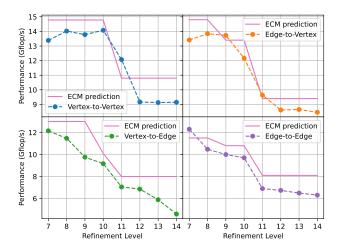


Figure 7: ECM model predictions and measurements for the different kernels analyzed in Section 5.

additionally, the whole data fits into the L3 cache. The last column states the performance prediction for the highest level in the given range.

To calculate the predicted performance in Gflop, we multiply the number of flops by the CPU frequency and divide that through the predicted cycles. In the case that the L1 LC is fulfilled the prediction is $(8 \cdot 13 \text{ flop} \cdot 2.7 \text{ GHz})/19 \text{ cy} = 14.78 \text{ Gflop/s}$.

For the calculations in Table 4, we assume that the LC is constant for the whole kernel, which is not the case since we deal with triangular domains. Therefore the actual measured performance is different, as shown in Figure 7.

Refinement level 11 shows a higher performance than the prediction of 10.8 Gflop/s. We explain this by constantly decreasing row sizes due to the triangular structure. After a certain number of iterations, the rows will start to fit into the L1 cache again. It is assumed that the LC for the L1 cache is fulfilled for the upper half of the rows, which explains the performance overshoot compared to the prediction. For level 12, the ratio of L1LC reduces to bellow 10 %, and therefore, the effect can be neglected.

The prediction of 10.8 Gflop/s is 17 % above the actual measured performance of 9 Gflop/s. The results from how the ECM model was used in this publication do not consider the changes to the L3 cache with the introduction of the Skylake microarchitecture. Details on these changes, introduced with Skylake, can be found in [2].

5.3 Edge-to-Vertex

This section analyzes the kernel that couples the edge DoF to the vertex DoF. Listing 2 and Figure 6b show the details. Since the horizontal, vertical, and diagonal edge DoFs are split into separate arrays, there are three loads and one store stream.

Each iteration of the kernel executes twelve MULT and eleven ADD instructions. Normalizing these numbers to an entire cache line yields 24 MULT and 22 ADD. With FMA AVX, the theoretical

Listing 2: Edge-to-Vertex kernel

LC	levels	ECM model cycles	prediction cycles	prediction Gflop/s
L1	7-8	{24 12 5 16 -}	{24]24]33]-]}	15.1
L2	9-10	{24 12 9 16 8}	{24]24]45]53]}	13.4
L2	11-14	$\{24 12 9 24 8\}$	{24]24]45]53]}	9.4

Table 5: ECM model for Edge-to-Vertex kernel.

throughput is at 12 cycles, but using the IACA tool, the prediction is 24 cycles per iteration, leading to $T_{OL} = 24cy$.

Concerning the data transfer from the L1 cache, there are twelve load streams and one store stream resulting in 2 AVX STOREs and 24 AVX LOADs per cache line. Therefore $T_{nOL}=12$, which IACA also confirmed.

For the data transfer between the cache level, the writing to the target array vertex causes the store and load of one cache line due to write-allocate. The edgeX, edgeY, and edgeXY arrays depend again on the LC. In the best case, only one entry per array (yellow border in Figure 6b) needs to be fetched from memory summing up to a total of three. The five entries without a border in Figure 6b are always available in the L1 cache. The other four entries reside in the L1 cache as long as the corresponding LC is fulfilled. Figure 6b shows these entries with a pink border. In this case, the predictions from the ECM model are $T_{L1L2} = 5cy$ and $T_{L2L3} = 16cy$. This condition holds if the refinement level is below ten, and this also means that the entire data resides in the L3 cache, meaning there is no traffic between the L3 and main memory.

If the LC is violated, four additional loads exist between each cache level. Interestingly, due to the stencil's shape for the edgeY and edgeXY arrays, there is only one additional entry, but for the edgeX array, there are two. This is because the kernel touches both y+1 and y-1, whereas in the other cases, only y+1 is needed.

From level eleven onwards, there is also traffic between the L3 cache and the main memory. Since there are three loads and one store stream, we use a transfer time of 2.0 cy per cache line from Table 1.

Figure 6b show the measurements for this kernel, which are in good accordance with the predictions.

5.4 Vertex-to-Edge Kernel

Now the kernel coupling from vertex DoFs to edge DoFs is analyzed, shown in Listing 3 and Figure 6c. In contrast to the Vertex-to-Vertex kernel, it writes to three data targets (edgeX, edgeY, edgeYY).

This kernel performs four multiplications and three additions for all three target arrays in each iteration. A total of twelve MULT and

```
edgeX[y][ x] =
    vertex[y+1][x-1] * c0 + vertex[y ][x ] * c1 +
    vertex[y ][x+1] * c2 + vertex[y-1][x+1] * c3;

edgeXY[y][ x] =
    vertex[y+1][x ] * c4 + vertex[y+1][x+1] * c5 +
    vertex[y ][x ] * c6 + vertex[y ][x+1] * c7;

edgeY[y][ x] =
    vertex[y+1][x-1] * c8 + vertex[y+1][x ] * c9 +
    vertex[y ][x ] * c10 + vertex[y ][x+1] * c11;
```

Listing 3: Vertex-To-Edge kernel

LC	levels	ECM model cycles	prediction cycles	pred. Gflop/s
L1	7-9	{14.8 12 7 16 -}	{14.8]19]35]-]}	13.0
L2	10	{14.8 12 9 24 -}	{14.8 21 45 - }	10.1
L2	11-14	{14.8 12 9 24 11.6}	{14.8 21 45 56.6 }	8.0

Table 6: ECM model for Vertex-to-Edge kernel.

nine ADD instructions. Using vectorization and fused multiply-add, this reduces to 12 FMA AVX instructions for four iterations and 24 FMA AVX instructions for one work unit. Theoretically, two FMA AVX instructions can be executed per cycle, suggesting that processing an entire cache line needs 12 cycles. However, an analysis of the kernel using the IACA tool shows that the throughput is slightly higher $T_{OL}=14.8cy$.

The kernel writes into three different array locations and reads from twelve. However, [x][y], [x+1][y] and [x][y+1] are used three times, and therefore only six actual loads are needed. IACA predicts that these loads and stores take 12 cycles $(T_{nOL} = 12cy)$.

Now the data transfers between the cache levels are analyzed. There are three store streams and three load streams due to write-allocate for the target arrays edgeX, edgeY,edgeXY. At least one CL transfer is needed for the source array srcVertex. Figure 6c show this point with a yellow border. Similar to the Vertex-to-Vertex kernel, there are two entries in the source array (pink border) where the LC determines from which level of the memory hierarchy they are fetched. If the LC for the L1 cache is fulfilled $T_{L1L2} = 7cy$ and $T_{L2L3} = 16$. Once the L1 LC is violated T_{L1L2} increases to 9cy, and in the case that the L2 LC is also violated T_{L2L3} becomes 24cy. Remember that only the load streams are considered for T_{L2L3} since this connection is full-duplex and can read and write simultaneously.

For the transfer between the L3 cache and main memory, we use the bandwidth from Table 1. Since there is one load and three store streams to memory, T_{L3MEM} is 11.6 cy.

Table 6 displays the ECM model predictions for the kernel. The ECM predictions here are in good accordance except for the higher levels, where the prediction and the measurements diverge. We attribute this to the fact that at refinement level 15, the LC for the L3 cache would be violated, which already shows at smaller sizes. Additionally, the ratio of three stores to one load stream reduces the performance. Table 1 also displays this characteristic, where the respective benchmark reaches the lowest bandwidth.

```
dstEdgeX[y][ x] =
 srcEdgeX [y ][x ] * c0 + srcEdgeY [y ][x
 srcEdgeY [y-1][x+1] * c2 + srcEdgeXY[y
                                        ][x
 srcEdgeXY[y-1][x ] * c4;
dstEdgeY[y][x] =
 srcEdgeY [y ][x ] * c5 + srcEdgeX [y ][x ] * c6 +
 srcEdgeX [y+1][x-1] * c7 + srcEdgeXY[y ][x
 srcEdgeXY[v
             ][x-1] * c9;
dstEdgeXY[y][x]
  srcEdgeXY[y
              ][x ] * c10 + srcEdgeX [y
                                              ] * c11 +
 srcEdgeX [y+1][x ] * c12 + srcEdgeY [y ][x ] * c13
 srcEdgeY [y ][x+1] * c14;
```

Listing 4: Edge-to-Edge kernel

5.5 Edge-to-Edge

The last kernel to be analyzed is the one coupling edge and edge DoF shown in Listing 4 and Figure 6d. This kernel uses three load streams and three store streams.

For each group of edge DoFs, five MULT and four ADD instructions per iteration need to be performed. Like before, there are eight iterations when normalizing to an entire cache line, leading to $5 \cdot 3 \cdot 8 = 120$ multiplications and $4 \cdot 3 \cdot 8 = 96$ additions. Within one FMA AVX instruction, a maximum of four MULT and four ADD instructions are executed, reducing the total operations to 30 FMA AVX instructions. The IACA tool reports that it takes 20 cycles to process one cache line for this kernel which is higher than the theoretical value of 15 cycles since the Skylake architecture is theoretically capable of performing 2 FMA AVX instructions per cycle ($T_{OL} = 20cy$).

Looking at the data traffic between the L1 cache and the registers, three writes, and nine loads (three per group) are necessary. Since one AVX load is equivalent to four double loads, this results in six AVX STOREs and 18 AVX LOADs per cache line. IACA shows that it takes ten cycles, which leads to $T_{nOL}=10$

For the data traffic within the cache hierarchy, the dstEdgeX, dstEdgeY, and dstEdgeXY arrays cause one store and one load stream each. For the srcEdgeX,srcEdgeY, and srcEdgeXY arrays, each array has one entry that was never touched, causing one load stream throughout the whole cache hierarchy. The last iteration used one entry of each array, meaning these entries still reside in the L1 cache. For the remaining three entries, the LC determines the location in the memory hierarchy. Figure 6d shows the entries in the L1 cache without a border, the new entries with a yellow border, and the entries that are possibly in the cache with a pink border. If the L1 layer condition is fulfilled the ECM reads $T_{L1L2} = 9cy$ and $T_{L2L3} = 24cy$. The ECM model for the different refinement levels is presented in Table 7.

Above level eight, the L1 LC no longer holds and T_{L1L2} increases to 12 cy. Until level ten, the entire data can also be kept in the L3 cache, meaning there is no data traffic to memory. From level eleven on, the memory traffic needs to be considered. We used the bandwidth results for the LIKWID benchmark with one load and one store stream since it has the same ratio. The transfer time for one cache line from main memory to L3 cache is, therefore, 2.5 cy The six streams that are required result in a prediction of T_{L3MEM} being 15 cy.

Figure 6d compares the measurements with the predictions, which match very well. The fact that on refinement level seven, the

LC	levels	ECM model cycles	prediction cycles	prediction Gflop/s
L1	7-8	{20 10 9 24 -}	{20]19]43]-]}	11.5
L2	9-10	{20 10 12 24 15}	{20]22]46]61]}	10.8
L2	10-14	{20 10 12 24 15}	{20]22]46]61]}	8.1

Table 7: ECM model for the Edge-to-Edge kernel

whole dataset nearly fits into the L2 cache explains this point being above the prediction of the ECM model.

6 MULTI-CORE SCALING

This section analyzes the scaling of all four kernels when executing on a single node. When using the ECM model to predict the performance for a specific number of cores, one has to differentiate between exclusive and shared resources within the CPU. All compute units, registers, the L1, and the L2 cache are exclusive for each core. However, the L3 cache and the main memory are shared amongst different cores. Therefore, we expect perfect scaling if the data fits in the L2 cache.

Figure 8 shows weak scaling of the four kernels from 1 to 48 processes for refinement level 8. Weak scaling means the application adds a new triangle for each process to the mesh. The scheduling is chosen to fill one socket before using the second socket. As expected, the scaling up to six processes is linear since all the data can be kept in the L2 cache. Beyond this, the shared L3 and main memory cause a saturation up to the entire socket containing 24 processes.

The Vertex-to-Vertex-Apply kernel shows a particular behavior. After ten processes, the performance decreases because the shared L3 cache can no longer hold the whole mesh. In other words, the size of the L3 cache available per core decreases when the number of processes increases.

Once processes utilize the second socket, the performance increases linearly. The scheduling of the processes causes this characteristic. Since the first socket is already fully saturated, the performance can only increase by 1/24 because new processes have to wait for all 24 processes on the other socket. Overall this scaling behavior follows the characteristic of memory-bound kernels in general.

7 CONCLUSION AND OUTLOOK

This paper analyses the differences between matrix-free and sparse matrix versions of matrix-vector multiplication. One clear advantage of the matrix-free version is the reduced memory footprint. In particular, the article compares the standard HPC library PETSC against the recently developed HyTeG framework concerning their memory requirements. Here, HyTeG could reduce memory consumption significantly when the matrix-free methods were employed. Furthermore, PETSC must be compiled with 64-bit integer indices to reach the same number of global DoF as HyTeG since the default 32-bit indices would overflow at refinement level 12. Section 4 shows how HyTeG uses code generation techniques to fully utilize the memory bandwidth.

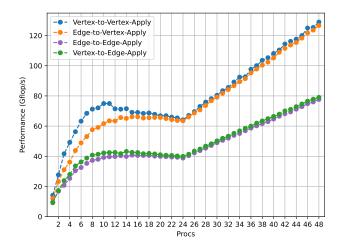


Figure 8: Intra-node scaling of the four different kernels to the full socket of one SuperMUC-NG node containing two sockets. The first 24 processes are scheduled onto one socket before the second socket is used. This scheduling explains the saturation at 24 processes due to the saturation in main memory.

The paper demonstrates how an elaborate exercise in performance modeling can be used to determine theoretical peak performance. This analysis is based on the ECM model. The article demonstrates that all analyzed kernels can reach the ECM-predicted performance limit when using code, the generation techniques of HyTeG. A first single-core comparison of the complete matrix-vector multiplication of HyTeG with PETSc on the SuperMUC-NG system showed a speedup of 5.3 in favor of HyTeG. However, more analyses would be required to evaluate this difference further.

The article thus presents a detailed performance analysis of the most critical kernels relevant for 2D simulations with the HyTeG framework. However, as discussed in Section 5, the four kernels needed to perform one complete matrix-vector multiplication are currently independent routines. As such, they cause an overhead in memory transfer. Merging these four kernels into a single one will accelerate the execution further. The same code generation techniques as already used could significantly reduce the work. However, the surrounding data structures need extensive adjustments to support the changed interface. In the limit, this loop merge could improve the performance of the whole matrix-vector multiplication by another factor of four, provided that data can be reused entirely and the memory bandwidth is still the limiting performance factor.

Clearly, the next significant step is to extend the performance analysis to 3D HyTeG-meshes. The transition from 2D to 3D leads to much more complicated stencil patterns, especially for DoF located at the edges. A comprehensive study will be the topic of future research.

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