Physical Design Challenges for Automotive ASICs

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ABSTRACT

The design of automotive ASICs faces several key challenges that mainly arise from the harsh environmental operating conditions, specific functional loads, cost pressure, safety requirements, and the steady progress of the automotive-grade semiconductor technologies that are unique to automotive applications.

The talk first highlights these key differences between the design approaches for automotive and non-automotive ASIC designs. It also addresses why automotive ASIC designs prefer larger and more mature nodes compared to leading-edge non-automotive ASIC designs. In addition, the talk introduces several automotive-specific physical design problems and essential solutions for design implementation, direct-verification and meta-verification to address them. Finally, the talk provides an outlook of several related and yet-unsolved challenges in the physical design domain.

CCS Concepts/ACM Classifiers

Hardware → Integrated circuits

Author Keywords

ASIC; automotive; design meta-verification; physical design; physical verification; reliability

BIOGRAPHY

From 1992-2000, Goeran Jerke studied Electrical Engineering at the Dresden University of Technology in Dresden, Germany. He joined Bosch Semiconductor in 2000, where he was developing solutions for analog routing, incl. the very first full-chip EMIR verification and physical design solutions for automotive ASIC production design flows. Later-on he developed production-proven solutions for constraint-driven design, module design, and he contributed to the evolution of parameterized cells for many novel (and unusual) use cases in several semiconductor application fields. Since several years, he oversees automotive-grade design flow developments for advanced node and advanced ASIC-/SiP-package co-designs. Furthermore, he is currently developing novel solutions for the mission-profile aware design of electronic applications, and he is leading a related international standardization activity at IEC TC56.

Goeran received the German EDA Achievement Award in 2005 for his work on Electromigration-aware design methodologies.

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