Computer Systems

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Digital Data Processor for Tracking the Partially Illuminated Moon*

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A study of lunar tracking techniques and fabrication of a breadboard to assess the feasibility of the best technique selected was conducted to define a tracking system for observation of the sightline to the center of a partially illuminated moon. The data processing portion of the system is presented in detail and then described in general are the operation of the tracker head assembly for data readout, the operation of the entire system and the effect data processing considerations have on the design of the tracker system.

The system basically consists of an optical sensor, digital computer and tracker drive mechanism. The three system units, connected in cascade, comprise the control loop. For this application, an optical telescope with a radial mechanical scanning mechanism was used that read out lunar sightline measurement information. This information is sequentially read into a special purpose digital computer that extracts the measurements and computes the error signals that drive the tracker to the appropriate attitude.

Tracking Technique

An analysis of tracking techniques indicates that methods for tracking a partially illuminated moon can be divided into two groups. The first group contains those methods that utilize area information about the moon to employ a disk matching technique to lock-on and track the moon. The second group consists of methods that distinguish the edge of the visible disk of the moon (lunar limb) from the other portions of the lunar contour, and by appropriate measurements locate the lunar image with respect to a reference coordinate frame. Although the disk matching technique is elementary in concept, it is difficult to mechanize, and the alignment sensitivity is nonuniform and frequently inadequate. For these reasons the limb sensing technique was considered superior and hence selected for this application.

The limb sensing tracking method was investigated using a multisweep routine and a three-sweep routine, where the sweeping operation occurs once per look. The multisweep approach was extremely attractive because of the desirability of redundant data; however, the computer requirements appeared severe compared to the gains to be expected. Therefore for this application, the three-sweep data gathering scheme was selected because of ease of data processing mechanization and adequacy for demonstrating the tracking principle within the specified tracking error range.

To define the sweep mechanism, consider a rotating opaque disk with a transparent spiral slit and a nonrotating opaque disk with three transparent radial slits displaced 60 degrees apart. These disks mounted on the same axis are almost in contact in the focal plane of the lunar image, (Figure 1). As the spiral slit rotates counterclockwise, the trace on the phototube defined by the intersection of the spiral and radial slits becomes a linear radial trace traveling inward toward the tracker barrel axis. An examination of this mechanical arrangement shows that the spiral slit can intersect more than one radial slit. Masking to one radial slit is obtained by using a third rotating opaque disk that isolates the appropriate slit during the sweep motion. An additional mask, the line of cusp mask, permits a group of three slits to be exposed depending on the moon's position at a particular time. The scanning mechanism mechanical specifications are contained in Table 1.

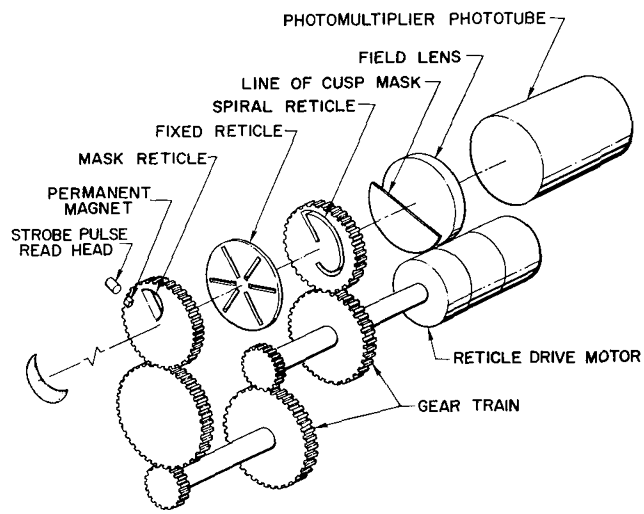

FIG. 1. Phototube and sweep mechanism

The phototube output consists of a sequential pattern of radiant flux pulses where, at a specified reference time, the interval between two successive positive-going pulses is

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proportional to the radial distance from the tracker axis sightline to the lunar limb. The computer logic requires an isolated pulse, the strobe pulse, that defines the start of a sensor readout cycle. This pulse is obtained when a permanent magnet fastened to the rotating mask disk and a magnetic drum read head fastened to the tracker barrel are adjacent. The relationship of the strobe pulse to the tracking data is shown in Figure 2.

TABLE 1. SWEEP MECHANISM SPECIFICATIONS

Radial slit width	0.34 arc minutes
Spiral slit width	0.17 arc minutes
Spiral angular velocity	30 rps
Rotating mask angular velocity	4.29 rps
Aperture linear velocity	2500 arc minutes per second of time
Radial sweep duration	25 msec

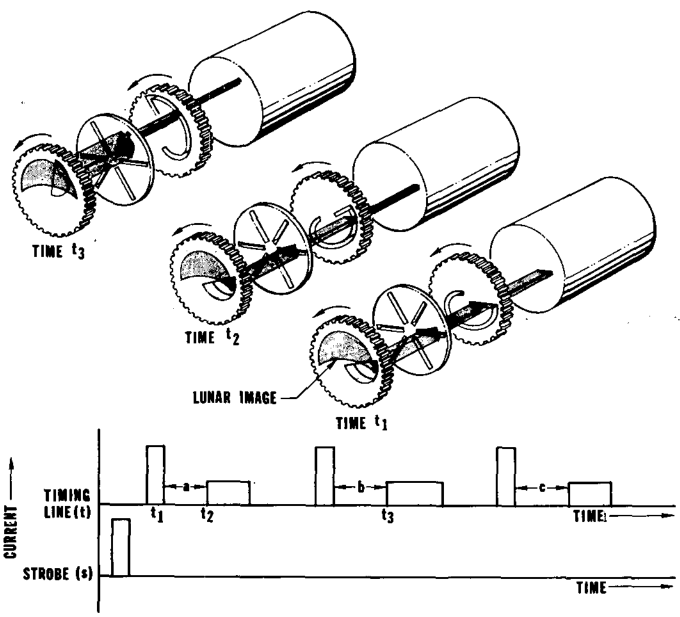

FIG. 2. Slit and masking disk positions for data readout

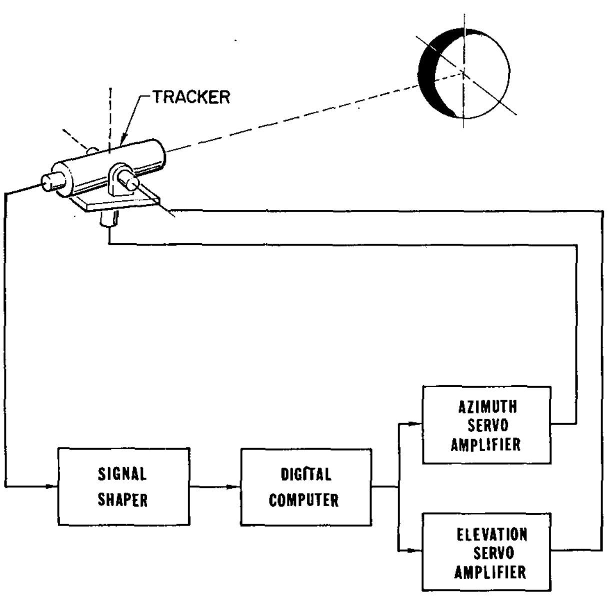

FIG. 3. The tracker loop

Information readout first occurs during a scanning cycle when a radial slit in the fixed disk coincides exactly with the radial slit on the spiral. This combination allows lunar flux energy to pass through the coincident slits and to generate a current pulse signal in the phototube. This corresponds to time t_1 of Figure 2. As the rotation of the spiral proceeds the scanning aperture moves inward at a linear velocity, and at time t_2 the aperture intersects the lunar limb. The process proceeds until three measurements are obtained. The measurements a, b and c are sequentially read into a digital computer that extracts the radial distance measurements and computes two orthogonal error signals, which are then converted from digital to analog voltage form. These analog command voltages are inputs to two high gain DC operational amplifiers that are the first stage of a servo drive mechanism attached to the elevation and azimuth tracker gimbals. A block diagram of the tracker loop is shown in Figure 3.

Computer Operation and Logic

When considering a data processing system for the solution of equations involving few terms, a digital computer especially designed for that application generally requires a relatively large amount of hardware. At the same time, for any application an analog computer requires a hardware mechanization tailored to the mathematics of the problem. In general, this makes the analog computer attractive for the handling of equations involving few terms and the digital machine applicable to the solution of complex problems. An analog and a hybrid analog-digital mechanization were thoroughly investigated for this application; they were rejected because the digital processor described in this paper appeared to be more advantageous in terms of cost, design effort, follow-on effort to demonstrate the multisweep approach, and hardware availability.

The lunar tracker digital computer is a special purpose machine designed to solve the equations that define two orthogonal tracker misalignment or error signals. These equations are, using the symbols of Figure 4,

$$\epsilon_x \cong \frac{1}{1-\cos 60°}\left(-\frac{r_A}{2} + r_B - \frac{r_C}{2}\right) \qquad (1)$$

$$\epsilon_y \cong \frac{1}{2-\sin 60°}\,(-r_A + r_C) \qquad (2)$$

Equations (1) and (2) are the basic relations used by the tracker to determine ϵ_x and ϵ_y, the misalignment errors in the x- and y-directions. However, in the actual tracker mechanization the quantities observed are

$$a = R - r_A\,, \qquad b = R - r_B\,, \qquad c = R - r_C\,,$$

where R is the radius of the sweep generated in the instrument. Therefore, the actual computer mechanization requires a solution to the equations

$$\epsilon_x \cong \mathrm{K}_1\left(-\frac{a}{2} + b - \frac{c}{2}\right) \qquad (3)$$

$$\epsilon_y \cong \mathrm{K}_2(-a + c) \qquad (4)$$

where K_1 and K_2 are constants representing loop scale factors.

Reference to Figure 5, which shows the information occurrence as a function of time on several computeres, lin and Figure 6, which shows the lunar tracker data processing structure, will aid in understanding the logical structure and operation of the lunar tracker data processor. The radial distance information is read out of the phototube on the t or timing line. The information, after preamplification, is shaped using a differentiating circuit designed to reproduce the positive going edge of the input pulses. These pulses in turn drive a Schmitt trigger circuit used to standardize the pulses to the logic requirements of the computer circuits.

The timing information, after pulse shaping, is gated into a 3-bit counter which in part performs the computer control function during the computation cycle. The counter is reset to zero at the start of the computation cycle and changes state whenever a timing pulse occurs. The 3-bit counter counts in a standard binary fashion through six states, and recycles at the concurrence of a timing pulse and the binary number equivalent to 5.

An analysis of the 3-bit counting process indicates that the time interval of the occurrence of the binary number 001 is proportional to the radial distance a. Also, the time duration of the number 011 is proportional to the radial distance b and the time duration of the number 101 similarly represents the distance c (Figures 2 and 5).

Given the radial distances as a function of time, a statement of the computer mechanization may be conveniently divided into several parts. These parts are: (1) the representation of each radial distance as a binary number, (2) the machine operation and control necessary for the time sharing of the ϵ_x and ϵ_y computation, (3) the arithmetic unit, and (4) the output unit.

A binary measure of the time intervals that are proportional to the radial distances is obtained by gating a clock pulse source to a binary counter. The gate is controlled by the 3-bit portion of the control counter. This gating operation allows a sequence of pulses to be counted during each controlled time interval. In some cases the required measurement of the time duration is half the radial distance; see Eq. (3). This was implemented by a gating arrangement that causes a flip-flop to change state every clock pulse time. This flip-flop operates at a rate that is exactly half the clock rate, and a count of these pulses during a controlled time interval is proportional to a radial distance divided by two. The lunar tracker data processor uses a 300 kc clock rate. This frequency was chosen on the basis of an error analysis of the tracker loop.

When considering the machine mechanization for the time sharing of the ϵ_x and ϵ_y computation, a trade-off becomes apparent. A sequential solution cycle where each

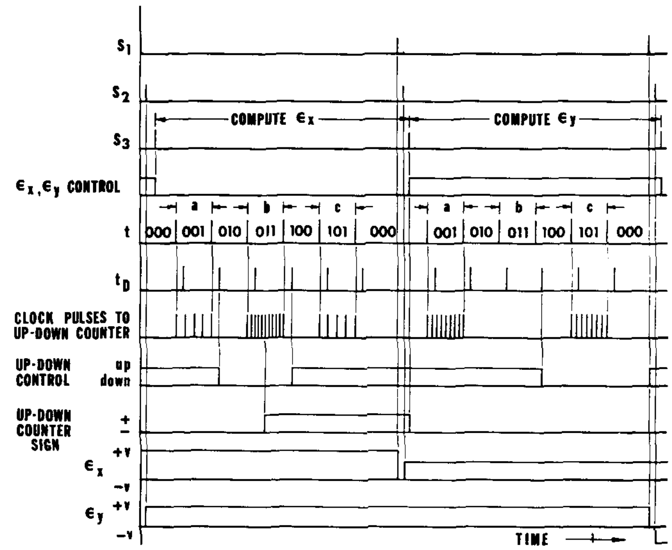

FIG. 5. Computer logic timing diagram

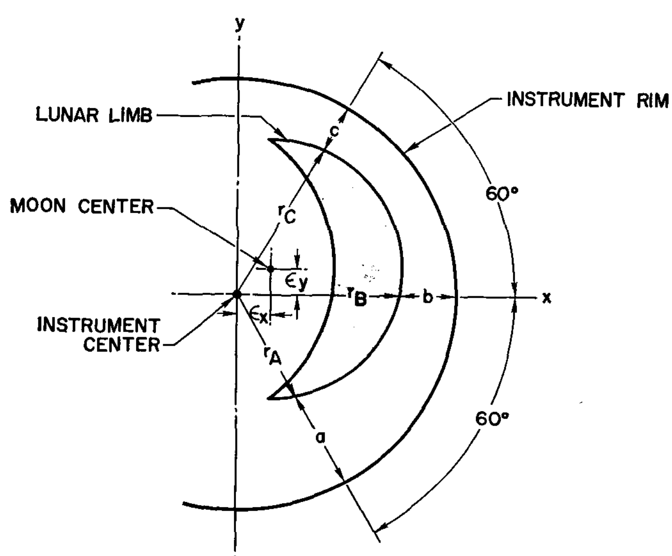

FIG. 4. Tracking geometry

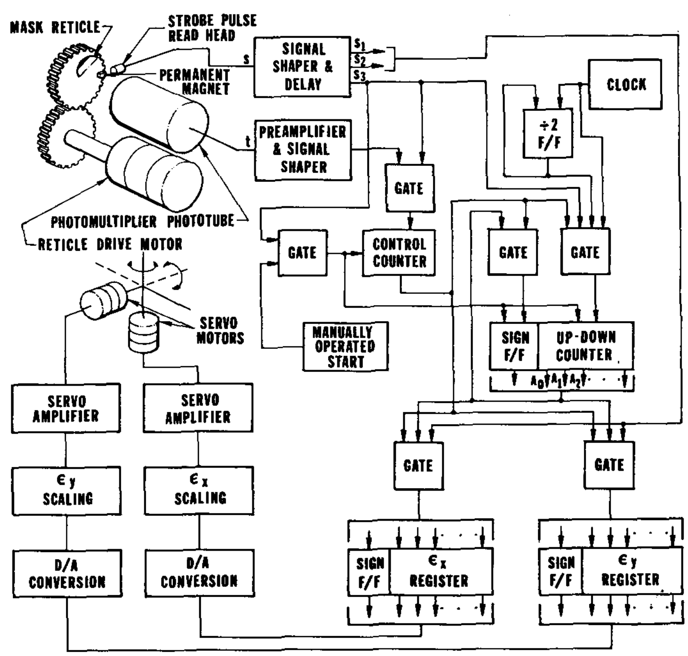

FIG. 6. Lunar tracker data processing structure

misalignment equation is solved separately requires less hardware at the sacrifice of additional data processing time. On the other hand, if parallel solutions are demanded by loop stability timing considerations, additional hardware is required. The desirable sequential solution cycle was analyzed for tracker loop stability by simulating the system on a large scientific digital computer. The simulation demonstrated the possibility of the successful use of the sequential solution cycle and the correctness of the system design.

For sequential operation, the control requirement is one additional bit added to the control counter. Basically, this control bit defines the ϵ_x or ϵ_y computation time; therefore, this bit changes state at the end of each scanning cycle. The information that defines the end of a scanning cycle occurs on the strobe line (S-line). The strobe pulse is shaped using a Schmitt trigger, and delayed to form three pulses S_1, S_2 and S_3 that occur on three separate lines. In this system, S_2 is delayed with respect to S_1, and S_3 is delayed with respect to S_2. The function of each strobe pulse will be defined subsequently.

The information available to the arithmetic unit is a controlled series of pulses proportional to the radial distances, as defined by eqs. (3) and (4), and occurring at controlled times. It therefore appears that a binary counter capable of reversing its count (subtraction operation) and a sign flip-flop necessary to define the direction of a magnitude are the necessary parts of the arithmetic unit. For this application, a 13-bit up-down binary counter was used.

To see how a solution is obtained for ϵ_x, consider a manually operated start pulse in coincidence with the strobe pulse. The coincidence of these pulses sets the entire control counter and the up-down counter to the zero state. Also, the up-down control flip-flop is set in an up-direction state and the sign flip-flop is set for a minus number. The lunar tracker digital data processor is now prepared to compute ϵ_x.

The first pulse that occurs on the timing line after control counter reset changes the state of the control counter. The state of this counter, in turn, allows a sequence of pulses that occur at half the clock rate to be gated into the up-down counter. The counting process continues until the next timing pulse occurs. At this time the up-down counter contains a number proportional to $-a/2$. Before the next counting sequence, a change in count direction must occur. This change of state of the up-down control flip-flop must occur between counting operations of the arithmetic unit. The mechanization of this requirement was obtained by delaying the timing pulses on a separate line (t_D-line) and gating these pulses with the state of the control counter (Figure 5).

The next sequence of pulses to be gated into the up-down counter occurs during the time interval proportional to the radial distance b. These pulses occur at the clock rate. The counting sequence is down, and at the end of this time interval the up-down counter contains a number proportional to $-a/2 + b$. The numerical sign associated with this number is contained in the sign flip-flop, which is set at strobe time and changes state every time the up-down counter travels through zero.

The computer logic requires a count direction change before the next arithmetic counting sequence occurs. After this operation, the next sequence of pulses that is gated into the up-down counter is proportional to the radial distance c. The input rate is exactly half the clock rate, and at the end of this time interval the up-down counter contains a number proportional to ϵ_x. At a convenient time this information is read out.

The development at this stage of the data processor indicates that the output unit must be capable of performing two functions. The output unit must store the end results of the arithmetic operations, and it must convert these digital signals to a DC analog voltage.

The output unit storage function is performed by two binary registers. The ϵ_x-register maintains the ϵ_x misalignment error and is updated at the end of every second scanning cycle. The ϵ_y-register maintains the ϵ_y misalignment error and is alternately updated at the end of every second scanning cycle. Therefore, the arithmetic unit sequentially computes each error signal and reads this information out in an alternate fashion to each output register. The readout occurs in a parallel fashion at a strobe pulse time.

A definition of the gating requirements to transfer a number from the up-down counter to an output register that contains prior information requires, as a gate input, the state of each bit of the register. However, if each bit of the output register is set to zero just before the transfer command, the state is implied beforehand and transfer can occur without sensing the state of each register bit. This computer mechanization consideration was taken advantage of in the present design, with gating hardware savings resulting. Tracker operation was not disturbed by this transient due to the gain-versus-frequency characteristics of the tracker loop.

At this time a review of a readout sequence is appropriate. The sequence starts when the ϵ_x- or ϵ_y-register is cleared to the zero state. After this operation is performed, the up-down counter and sign flip-flop are read into the cleared register. The third sequence instructs the up-down counter to clear to a zero-state. Also, at this time the ϵ_x or ϵ_y control flip-flop and the sign flip-flop are instructed to change state. The sequence requires three instructions that are initiated by the three strobe pulses S_1, S_2 and S_3.

A second hardware saving becomes evident when considering the nulling effect of the error signals during tracker operation. Because the tracker error signal during system operation is zero or close to zero, it appears that an output register with a dynamic range less than the capacity of the up-down counter can be used. In the lunar tracker application, a reduced size register containing eight bits was used. This resulted in a savings of five flip-flops per register.

An analysis of the computer logic to obtain a reduced output register indicates an increased gating requirement for proper up-down counter readout. Basically the increased gating causes every bit of the register to be set to

1 if any one of the five most significant bits of the up-down counter contains a 1. The increased gating requirement was trivial.

The digital-analog converter uses a weighted resistance network to obtain a DC output voltage proportional to the binary number contained in the output register. Each flip-flop of the output register operates a single-pole-double-throw transistor switch, which gates a constant reference voltage source to appropriate points of the weighted resistance network. The combination of switch positions determine the magnitude of the DC voltage that appears at a summing point of the resistor network. The tracker misalignment signal that appears at the summing point is required to swing either positive or negative with respect to ground to drive the tracker barrel in two directions from the origin of a reference coordinate system. The up-down counting sequence and the sign logic were tailored to the requirements for bipolar operation of the digital-analog converter.

Computer Design

The computer package was designed and fabricated using off-the-shelf solid state printed circuit logic cards, card holders and a power supply, all purchased from a vendor that designs and manufactures this equipment for digital data processing applications. The breadboard computer package required a neat packaging configuration suitable for test and laboratory use, and also had to be self-contained for shipment to the customer. Furthermore, from necessity, only a minimum amount of circuit design and drafting time was permitted. The vendor-supplied materials filled the above requirements and were functionally adequate.

The plug-in logic cards are housed in two rack-mounted card holders (Figure 7). Mounted between the two card holders is a control and test panel. This panel contains several computer test points for easy access, manual slewing control, power supply switches, readout calibration potentiometers and tracker start control. Also, attached to the inside of this panel are the ϵ_x and ϵ_y servo amplifiers (Figure 8). The bottom rack panel space contains the computer power supply.

The tracker head assembly on a mount in the observatory during an actual test is shown in Figure 9.

Conclusion

The lunar tracker data processing structure is unique among most applications of this type due to the digital mechanization of mathematics that, on the surface, appear attractive to analog computation techniques. The special purpose digital computer described in this paper was fabricated after a complete analysis was performed of pure analog, combination analog-digital and pure digital mechanization techniques for this application. The digital computer that was designed and built exhibited excellent performance and low cost because, in part, specially tailored digital mechanization techniques were used.

The program for testing the lunar tracker breadboard

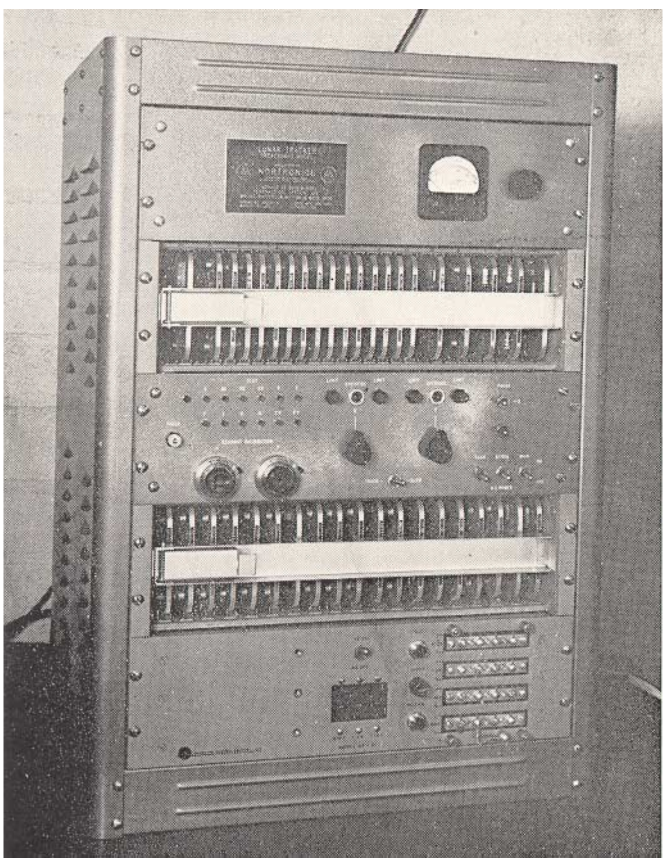

FIG. 7. Lunar tracker computer

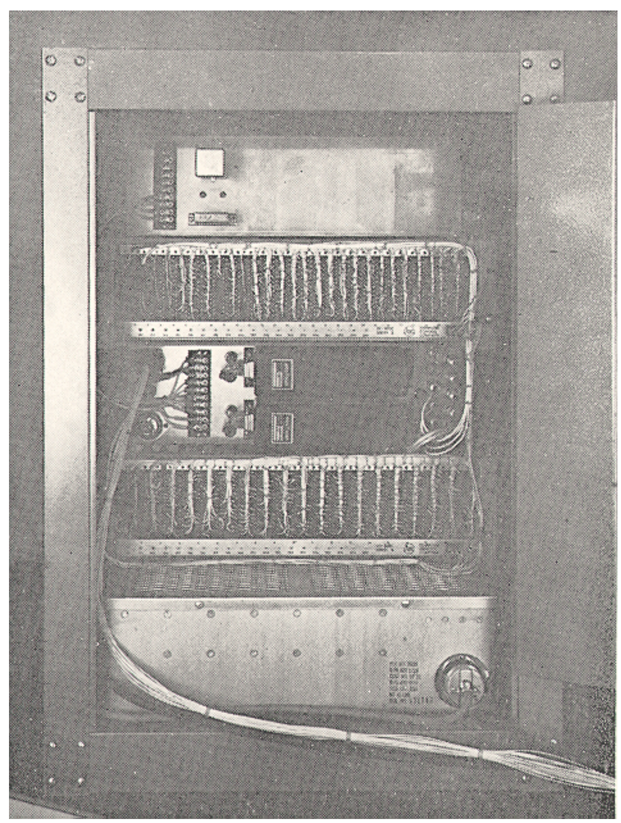

FIG. 8. Lunar tracker computer: rear view

and evaluating its performance was divided into two parts: (1) laboratory tracking of a simulated moon, and (2) observatory tracking of the natural moon. The laboratory lunar tracking simulation, in preparation for natural lunar tracking, was designed to appear as similar to the natural moon as possible. In the laboratory, the simulated moon was tracked successfully with a tracking error of less than 20 seconds of arc.

The observatory test was performed with the tracker head assembly mounted on a polar mount with a massive pedestal. Lunar tracking tests were performed during the waning period of the moon in the latter part of February 1962 and the waxing period during early March. The natural moon was tracked successfully with a tracking error of less than 20 seconds of arc.

APPENDIX. Digital Logic for Lunar Tracker Digital Data Processor

Introduction

The digital logic expressions for the lunar tracking digital data processor defines completely the operation of the computer and offers an estimate of the required hardware. For these reasons the Boolean expressions are appended for the interested reader. The equations contained in this appendix do not include the logic for a standard binary counting sequence, as used in the control counter, and the up-down counter of the lunar tracker digital data processor. This information can be found in many computer reference works.

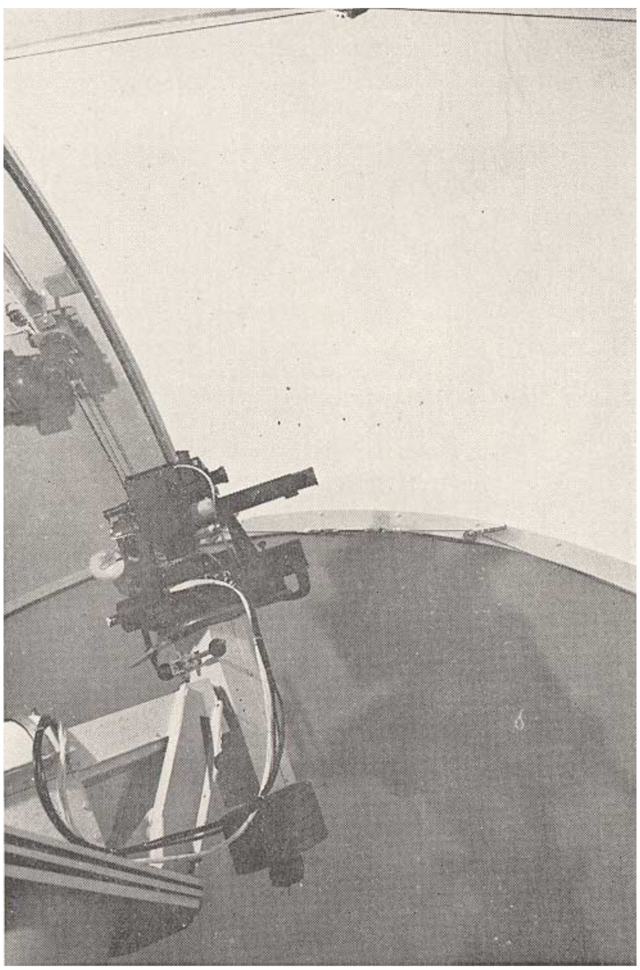

FIG. 9. Lunar tracker on mount in observatory

Nomenclature

S_1, S_2, S_3	Strobe pulses: S_3 delayed with respect to S_2, S_2 delayed with respect to S_1
t, t_D	Timing line or input data line: t_D delayed with respect to t
C	Clock
X_n	nth flip-flop of the X-register
Y_n	nth flip-flop of the Y-register
A_n	nth flip-flop of the up-down counter
S	Strobe pulse—can be S_1 or S_2 or S_3
Start	Start pulse

Logic

GHI Counter (control counter)

$$_0G = S\ (\text{Start}) + GIt \qquad _1G = HIt$$
$$_0H = S\ (\text{Start}) + HIt \qquad _1H = G\overline{HIt}$$
$$_0I = S\ (\text{Start}) + It \qquad _1I = t\bar{I}$$

P Flip-Flop (ϵ_x or ϵ_y computation control)

$$_0P = S_3P + S\ (\text{Start}) \qquad _1P = S_3\bar{P}$$

F Flip-Flop (up-down control)

$$_0F = \bar{P}H\bar{I}t_D + PG\bar{I}t_D \qquad _1F = S + \bar{P}G\bar{I}t_D$$

where F-state $\equiv$ count up
$\bar{F}$-state $\equiv$ count down

T Flip-Flop (sign)

$$_0T = Z_2\ \bar{P}HI + Z_2\ PGI \qquad _1T = S + Z_1\ \bar{P}GI$$

where T-state = minus number
$\bar{T}$-state = plus number
$Z_1 = \bar{A}_0\ \bar{A}_1\ \bar{A}_2\ \bar{A}_3 \cdots \bar{A}_{12}$
$Z_2 = A_0\ A_1\ A_2\ A_3 \cdots A_{12}$

X_T Flip-Flop (X-register sign)

$$_0X_T = \overline{TP}S_2 \qquad _1X_T = T\bar{P}S_2$$

Y_T Flip-Flop (Y-register sign)

$$_0Y_T = \bar{T}PS_2 \qquad _1Y_T = TPS_2$$

Q Flip-Flop (Divide by two)

$$_0Q = CQ \qquad _1Q = C\bar{Q}$$

Up-Down Counter Gating

$$\text{Counter Input} = \bar{P}HIC + P\bar{H}IC + \overline{PH}IQ$$

Up-Down Counter Read-out Gating

Reduced size register:

$$_0X_n = S_1\bar{P} + S_1\ \bar{P}B\bar{T} \qquad _1X_n = S_2\bar{P}\ (TA_n + A_nW + TW)$$
$$_0Y_n = S_1P + S_1\ PB\bar{T} \qquad _1Y_n = S_2P\ (TA_n + A_nW + TW)$$

where $W = A_8 + A_9 + A_{10} + A_{11} + A_{12}$
$B = \bar{A}_8 + \bar{A}_9 + \bar{A}_{10} + \bar{A}_{11} + \bar{A}_{12}$

Full register:

$$_0X_n = S_1\bar{P} \qquad _1X_n = S_2\bar{P}A_n$$
$$_0Y_n = S_1P \qquad _1Y_n = S_2PA_n$$

Acknowledgment. A paper about a project such as the preceding necessarily reflects the concepts and creative efforts of many individuals. The contributions of these individuals are gratefully acknowledged.

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1. Investigation of optical techniques for lunar tracking. Final Engineering Report NORT 62-86, Nortronics, a Division of Northrop Corp., Contr. No. AF 33(616)-8242, April 1962.