Analysis and Optimization Strategies Based on 4-bit Absolute Value Detector

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ABSTRACT

Currently, there is a strong emphasis on miniaturization and integration, allowing for smaller, more portable devices with multifunctionality, abundant strategies could be used to improve the algorithm, such as FPGA and quantum computer and specialized architecture to algorithms. Absolute value detector (AVD) is one of the most core factors to accomplish the integration. This paper presents optimization strategies for enhancing the performance of an absolute value detector. The significance of the absolute value function and the fundamental principles of absolute value detection are initially introduced to facilitate better understanding. Subsequently, addressing the limitations of existing absolute value detectors, a solution is proposed by constructing a logic circuit using a combination of comparators, multiplexers (MUX), and half adders to achieve an optimized absolute value detector. This optimization leads to reduced energy consumption. However, the proposed solution still has room for improvement in terms of component performance to further minimize both energy consumption and circuit delay. The aim of this study is to optimize the absolute value detector to assist in the enhancement of computational capabilities and integrated circuit algorithms, while emphasizing the need for continued efforts in the development of human technology.

CCS CONCEPTS

• **Hardware**; • **Integrated circuits**; • **Logic circuits**; • **Combinational circuits**;

KEYWORDS

4-bit Absolute value detector, Optimization strategies, Logic circuit, Energy consumption, Delay

ACM Reference Format:
Tianze Zhang. 2023. Analysis and Optimization Strategies Based on 4-bit Absolute Value Detector. In *6th International Conference on Information Technologies and Electrical Engineering (ICITEE 2023), November 03–05, 2023, Changde, HUNAN, China.* ACM, New York, NY, USA, 7 pages. https://doi.org/10.1145/3640115.3640116

1 INTRODUCTION

Currently, the whole human world is in an era where the technology is boosting, and one of the paramount developments is computer hyper-computing. The hyper-computing (HPC) has already been a critical part of academic research and industry innovation for decades. HPC helps engineers, data scientists, designers, and other researchers significantly, reducing the computational time, aiding in the rapid and accurate processing of massive complex calculations, such as DNA sequencing [1, 2]. However, the processing of large-scale datasets, which is "big data" is one of the most serious challenges in HPC, it is indeed difficult to process large amounts of data, high data rates, or particularly complicated or unstructured data, absolute value detector, with highly sensitive and precise characteristics, could effectively handle with vast quantities of complex datasets [3].

This article would give a systematic introduction of the Absolute Value Detector, in the introduction part, the basic mathematical logic is expected to be briefly discussed, and then the passage gives you the operation principle of absolute value detector for better comprehension in subsequent discussions. In this article, a common device, 4-bit Absolute Value Detector, is used as the classic example to analyze current development and problematic of the detectors, and then the possible optimization strategy is given. In the given optimization, at the very first, a truth table is listed, and further logical circuits are built upon this foundation. Considering the balance between performance of the device and its power consumption, the path with shortest delay is selected to calculate the corresponding data. Ultimately, the feasibility of the proposed optimization would be evaluated from several sections. As the crucial parts of the HPC, 4-bit absolute value detector provide us great opportunities and possibilities, driving continuous progress in human society, development, and innovation of technology.

2 BRIEF INTRODUCTION OF ABSOLUTE VALUE DETECTOR

2.1 Absolute Value Function

It is necessary to give a distinct concept of the absolute value, which is one of the cores basic knowledge areas of the absolute value detector. The absolute value function, a mathematical expression that describes the distance of a number from the origin of the number line, is usually denoted as |x|, which is known as the modules of x [4]. Furthermore, the absolute value of any integer would be the real numbers, regardless of which sign it has. There are two vital properties which are expected to contribute the absolute value detector modeling: symmetry and non-negativity. Symmetry implies that the function remains unchanged if the input is negated, and non-negativity indicates that the output of the absolute value function is always greater than or equal to zero.

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ICITEE 2023, November 03–05, 2023, Changde, HUNAN, China

ACM ISBN 979-8-4007-0829-9/23/11
https://doi.org/10.1145/3640115.3640116

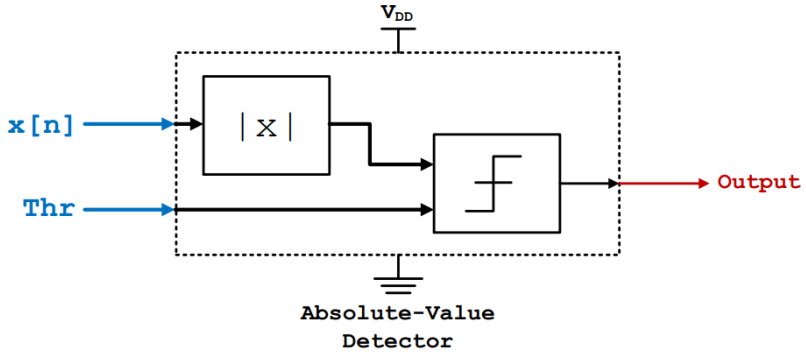

Figure 1: Absolute-Value Detector [5]

2.2 Principle and Operation of Detector

Absolute value detector (AVD) is commonly a circuit or algorithm, can implement basic bit arithmetic with logic circuits. Firstly, a threshold signal and an input signal would be given, and then they are expected to be compared. If the input signal is larger than or equal to the threshold signal, the detector would output 1, otherwise, the output would be 0. To compare these two signals, comparators are applied to implement it. Two input ports are designed in a comparator, one is input port, and the left one is reference signal, then the inner amplifier would amplify these two signals to detect the difference. Following that, the amplified input signal is compared with the reference signal. If the voltage at the input is greater than the voltage at the reference port, the output of the comparator is set to a high level (1); otherwise, the output would be set to a low level (0). The Absolute-Value Detector is shown in Figure 1.

3 OPTIMIZATION STRATEGIES

In order to ensure the experiment can reproduce and generalize, in this article 4-bit absolute value detector is taken as an example to analyze and optimize.

3.1 Limitations

To optimize the design of absolute value detectors, it is crucial to understand their limitations. This section gives the basic functionality where the limitations could appear of detectors, including accuracy, speed, power consumption, and dynamic range.

The accuracy of an absolute value detector refers to its ability to provide precise absolute value outputs, representing how close the correct value and measurements are [6]. It is influenced by factors such as component tolerances, circuit non-idealities, and noise. Designers must carefully consider these factors to minimize errors and achieve high accuracy in absolute value detection. The speed of an absolute value detector determines how quickly it can process input signals and produce accurate absolute value outputs. Faster operation is particularly crucial in real-time applications, where immediate results are required. Design optimizations, such as reducing propagation delays, optimizing component selection, and utilizing high-speed circuits, can enhance the speed of the detector.

Power consumption is a critical consideration in absolute value detector designs, especially in portable or battery-powered devices. Minimizing power consumption helps prolong battery life and reduce heat dissipation. Techniques such as low-power circuit design, efficient power supply management, and utilization of low-power components can be employed to minimize power consumption while maintaining adequate performance.

The dynamic range of an absolute value detector refers to the range of input amplitudes it can accurately process. A wider dynamic range allows the detector to handle a broader range of signals without distortion or loss of accuracy. Achieving a wide dynamic range involves careful selection of component specifications, signal conditioning techniques like amplification or attenuation, and ensuring sufficient resolution in analog-to-digital conversion stages.

3.2 Indicators

Performance indicators such as signal-to-noise ratio (SNR), total harmonic distortion (THD), and linearity are evaluated to assess the quality of detection.

3.2.1 Signal-to-Noise Ratio (SNR). The SNR is a performance indicator that evaluates the quality of detection in the presence of noise. It quantifies the ratio of the desired signal amplitude to the background noise level. A higher SNR indicates better noise rejection and more accurate absolute value detection. Design techniques such as noise filtering, shielding, and high-performance amplifiers can improve the SNR of absolute value detectors.

3.2.2 Total Harmonic Distortion (THD). THD measures the harmonic distortion introduced by the absolute value detector. It shows how much of the distortion of a voltage or current is due to harmonics in the signal. It is normally expected to be as low as possible, not always though, in audio, communications, power system, and in absolute value detector. Minimizing THD ensures that the detector accurately preserves the original signal's shape and eliminates unwanted distortions. Linearization techniques, careful component selection, and precise calibration can reduce THD and maintain signal fidelity.

3.2.3 Linearity. Linearity is an essential property of absolute value detectors, ensuring that the output is a faithful representation of the input signal's magnitude. Deviations from linearity can introduce

Table 1: Truth Table of AVD

A3	A2	A1	A0	X3	X2	X1	X0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	0	0	0
1	0	0	1	0	0	0	1
1	0	1	0	0	0	1	0
1	0	1	1	0	0	1	1
1	1	0	0	0	1	0	0
1	1	0	1	0	1	0	1
1	1	1	0	0	1	1	0
1	1	1	1	0	1	1	1

errors and distortions. Techniques such as proper biasing, careful circuit design, and compensation methods help maintain linearity and improve the overall accuracy of the detector.

3.3 Optimization Algorithm

As mentioned in the former part, to optimize the AVD, one of the core issues is try to improve the accuracy, speed, and make the power consumption as low as possible. If a relatively optimized critical path circuit delay, which means the original circuits are required to be simplified, is designed, then the issues could be solved. To design a comprehensive AVD, three parts are needed, which are half adder, MUX, and a comparator.

3.3.1 Half adder and MUX design. Table 1 shows a basic truth table of a 4-bit absolute value detector, where A is set to be the input, and X is set to be the output.

Normally, if the input value is positive, then no calculation is required to be done, only when the input value is negative should extra procedure be applied. To get the magnitude of negative value, the half adder is required. Generally, in a 2's complement value, if the value in the most significant bit (MSB) is 1, the whole value would be negative, conversely, the value is positive [7]. So, if the value is negative, then we need to use half adder to flip all bits and add 1 to it to get the magnitude value. Here's the details of converting the negative value into positive one. Table 2 gives the brief logic operation of 2's complement.

A normal half adder has XOR gate to calculate its sum (1) and an AND gate to calculate its carry (2) [5].

$$\text{Sum} = \text{A} \oplus \text{B} \tag{1}$$

$$\text{Cout} = \text{A} \times \text{B} \tag{2}$$

Because the less significant bit value (LSB) A0 always pluses 1 in the negative case. According to the equation 1), $A0^{'} \oplus 1$ is just A0 itself. According to this idea, a relatively reasonable MUX based half adder with lower power consumption is created. MUX, the multiplexer, which is applied to choose which value should be output. If A3 is 1, which means the value is negative, so the output would be converted to B, which is X3X2X1X0. Figure 2 shows the detail of the logic circuit.

3.3.2 Comparator design. The final part of 4-bit absolute value detector is a comparator, which is applied to compare the output value with the threshold value to ensure the AVD could detect whether the signal is positive or negative.[8] When comparing different values, there are two methods, one is to compare values from the most significant value (MSB) to less significant value (LSB), the other is to compare from LSB to MSB [9]. There, two methods are all designed. Figure 3 shows MSB to LSB and Figure 4 shows LSB to MSB.

Apparently, paths crossed in the second one, which is from LSB to MSB are less than the other one, and because only 6-bit value should be compared, which means the first two bits are the same, only the next three groups of values are expected to be compared, so the circuit could be further simplified. Therefore, it would have lower power consumption. Finally, all the parts are connected to be the ultimate AVD.

3.4 Final Circuit Design

Figure 5 is the final design of AVD.

Figure 6 shows the whole circuit of the AVD, and critical path is about to shown as below.

3.5 Critical Path Delay Calculation

The critical path is the longest path in the circuit and limits the clock speed [11]. To calculate the delay, several formulas are required.

$$\text{Delay} = \text{R}_{\text{gate}} (\text{C}_{\text{load}} + \text{C}_{\text{self}}) = \text{R}_{\text{gate}}\text{C}_{\text{load}} + \text{R}_{\text{gate}}\text{C}_{\text{self}} \tag{3}$$

Logical Effort basic equation:

$$d = f + p \tag{4}$$

d is the delay (normalized), f is known as the effort delay, p is known as the parasitic delay.

$$\text{d} = \text{Delay}/t = \left(\text{R}_{\text{gate}}\text{C}_{\text{load}}\right) + \text{R}_{\text{gate}}\text{C}_{\text{self}}/\text{R}_0\text{C}_0 \tag{5}$$

Table 2: 2's complement logic operation

*A*3(Sign bit)	*A*3*A*2*A*1*A*0(Input value)	*A*3*A*2*A*1*A*0(Flipped all bits)	*A*3*A*2*A*1*A*0(Add one)	X3X2X1X0(Magnitude value)
1 (negative)	1001(-7)	0110	0111	0111(+7)
0 (positive)	0001(+1)	\	\	0001(+1)

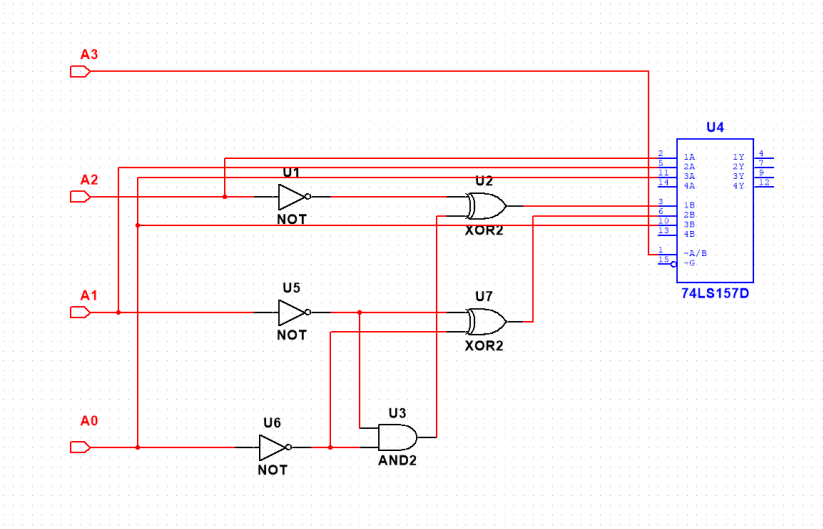

Figure 2: MUX based half adder (Photo/Picture credit: Original)

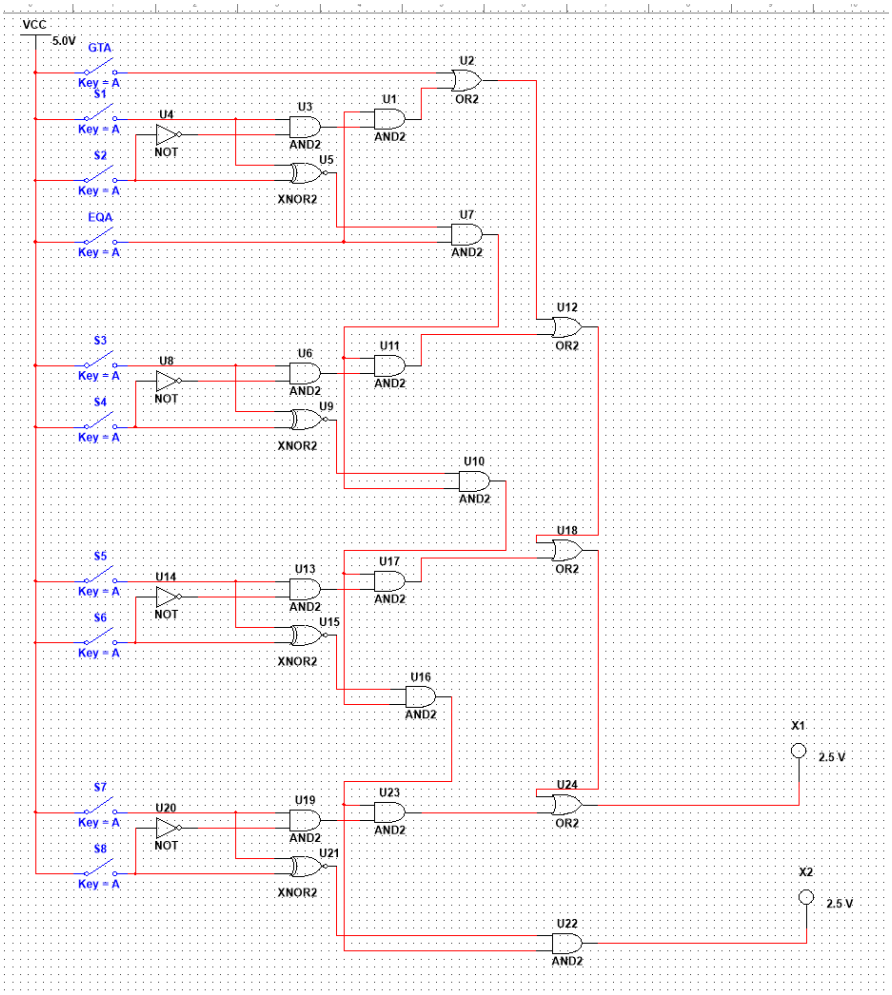

Figure 3: MSB to LSB 1 (Photo/Picture credit: Original)

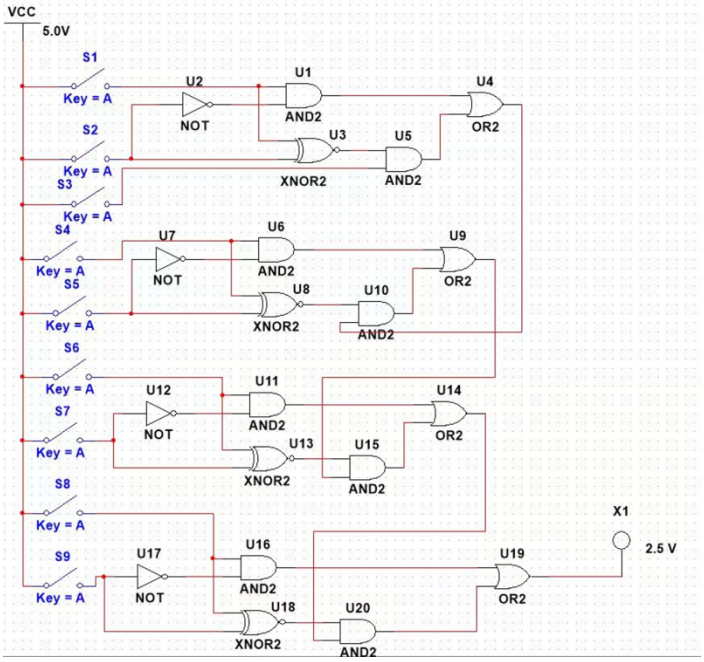

Figure 4: LSB to MSB 1 (Photo/Picture credit: Original)

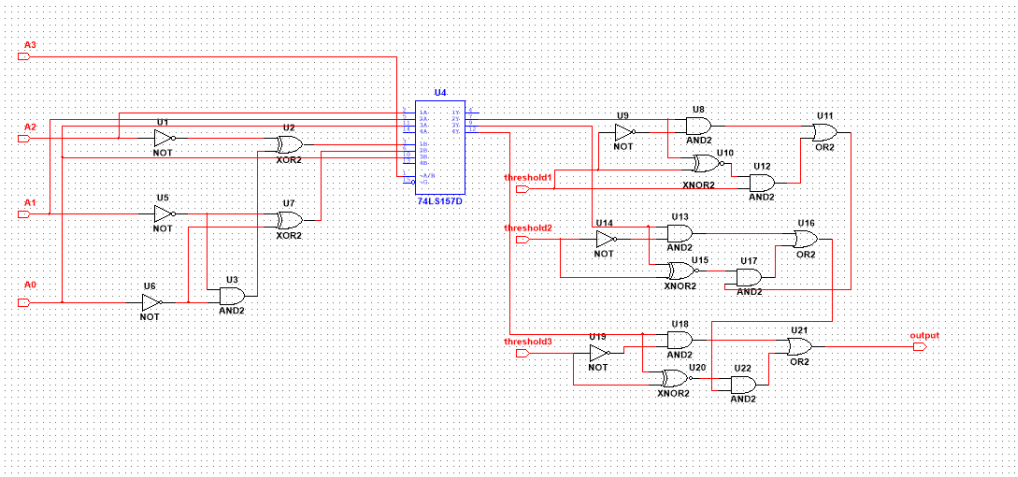

Figure 5: Final AVD design 1 (Photo/Picture credit: Original)

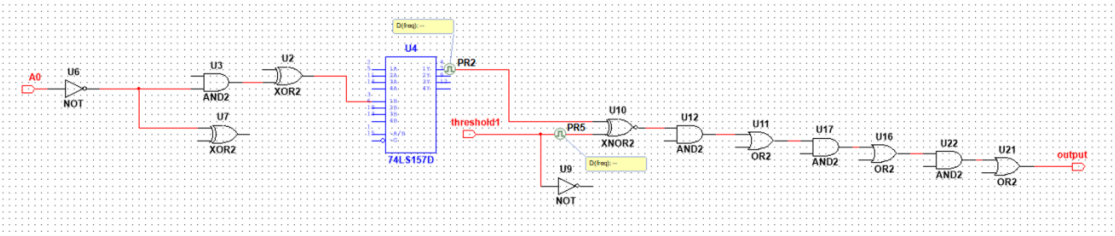

Figure 6: Critical path 1 (Photo/Picture credit: Original)

Table 3: Logical effort of common gates, from p 7 of [10]

Gate Type	Number of Inputs				
	1	2	3	4	n
Inverter	1				
NAND		4/3	5/3	6/3	(n+2)/3
NOR		5/3	7/3	9/3	(2n+1)/3
Tristate, Multiplexer	2	2	2	2	2
XOR, XNOR		4,4	6,12,6	8,16,16,8	

Logical effort (g)

$$g = \frac{R_{gate} \times C_{in,gate}}{R_{INV} \times C_{in,INV}} \tag{6}$$

R ration for equal C, so it can be simplified as

$$g = \frac{C_{in,gate}}{C_{in,INV}} \tag{7}$$

Electrical fanout (h)

$$h = \frac{C_{out}}{C_{in,gate}} \tag{8}$$

Parasitic effort (p)

$$p = \frac{C_{par,gate}}{C_{par,INV}} \tag{9}$$

Path effort is calculated:
H is path branch effort.

$$\mathrm{F = GBH} \tag{10}$$

$$f = \sqrt[N]{F} \tag{11}$$

$$\mathrm{Totalpathdelay = N \times f * + p} \tag{12}$$

3.5.1 Sizing and V_{dd} . Table 3 shows the number of inputs of different gate types

$$G = \prod = \frac{2 \times 4^6 \times 5^3}{3^7} \tag{13}$$

Path electrical effort is calculated:

$$H = \frac{C_{out(path)}}{C_{in(path)}} = 32 \tag{14}$$

Path branch effort is calculated:

$$\mathrm{B = 2 \times 2 = 4} \tag{15}$$

Path effort is calculated:

$$\mathrm{F = GBH} \tag{16}$$

$$\mathrm{f^* = \sqrt[N]{F} = 2.718} \tag{17}$$

Path parasitic delay is calculated:

$$\mathrm{P = 1 + 2 + 4 + 4 + 26 + 4 = 27PS} \tag{18}$$

Total path delay is calculated

$$\mathrm{D = N \times f^* + P = 56.9PS} \tag{19}$$

3.5.2 Gate Sizing Approach. According to the formula, the sizing of the critical path gates from left to right is: C_{in} u6 = 1.002; C_{in} u3 = 2.72; C_{in} u2 = 2.776; C_{in} u4 = 1.880 ; C_{in} u10 = 2.563; C_{in} u12 = 0.871; C_{in} u11 = 1.7756; C_{in} u17 = 2.8956; C_{in} u16 = 5.9026; C_{in} u22 = 9.6259; C_{in} u21 =19.623; Output = 32.

$$\mathrm{C_{in} = g \times \frac{C_{out}}{f^*}} \tag{20}$$

3.5.3 V_{dd} Calculation. The V_{dd} is optimal voltage for the V_{dd} in the range of 0v - 1v. This voltage also satisfies the requirements that the maximum delay is 1.5 minimum delays [10].

$$\mathrm{Delay = \frac{K \times 1}{(1 - V_T)^2}} \tag{21}$$

$$\mathrm{1.5Delay = \frac{K \times V_{ddmin}}{(V_{ddmin} - V_T)^2}} \tag{22}$$

V_T is preset to be 0.2V, according to the formula (19), the minimum voltage, which is V_{ddmin} is calculated as 0.7751V.

When the voltage is 1V, total power consumption could be

$$\mathrm{E = C_l \times V_{dd}^2 = 32} \tag{23}$$

However, the optimized circuits own only 0.7751V, there, the power consumption would be decreased to:

$$\mathrm{E = C_l \times V_{ddmin}^2 = 19.225} \tag{24}$$

3.6 Result Analysis

When the VDD changes from 0V to 1V, we consider reducing energy consumption.[10] We plan to recalculate the critical delay and energy consumption. Obviously, the total power consumption has been decreased by 33.6%. However, the relative delay would increase by 50%. It seems that it is difficult to lower down the delay and power consumption at the same time. Indeed, when voltage decreases, power consumption could be controlled, inevitably, flexibility and sensitivity of this circuit would be limited. But there still have several solutions. Parallel processing could also be applied, dividing the whole procedure of the AVD into multiple stages to reduce the delay while improving the calculation speed. Besides, currently, integration of circuits and chips in a overwhelming trend, a more accurate device with smaller volume, which means lower power consumption, could solve this issue, lowering down the consumption while maintaining a high work efficiency. Nevertheless, those delicate devices are still not perfect, there still exist a risk of being prone to defects and transient faults. So they are also expected to be further optimized [12].

4 CONCLUSION

In conclusion, this article mainly focusses on the performance and possible strategy of 4-bit absolute value detector, with given circuit, the power consumption could be lower down while keeping a relative highly effective performance. According to the experiment and current situation, it is believed that 4-bit absolute value detector could have more space to be improved and enhanced, therefore, future development is expected to focus on three key directions. Reducing latency will be a priority, enabling faster and more efficient operations. A well-designed circuit could significantly decrease the delay and power consumption, greatly affect the performance, therefore, finding an appropriate transistor size and designing a sound circuit structure is a great method to optimize the AVD. And advancements in device-level technologies will lead to higher performance, improved energy efficiency, and enhanced functionality. Lastly, there will be a strong emphasis on miniaturization and integration, allowing for smaller, more portable devices with multifunctionality, abundant strategies could be used to improve the algorithm, such as Field-programmable gate array, and specialized architecture to algorithms. These trends collectively contribute to the evolution of devices towards a more connected, efficient, and compact future.

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