High performance of short-channel MOSFETs due to an elevated central-channel doping

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Abstract— An elevated central-channel doping with a depth similar to the S/D junctions is proposed as the best measure for simultaneously improving MOSFET device and high speed circuit performances as well as minimizing their fluctuations. We base our arguments on hydrodynamic device simulation, measured device data of vertical MOSFETs with a central delta-doped impurity profile and include experimental results on doping-profile fluctuations along the channel, which have not been available previously.

I. Introduction

Scaled MOSFETs must simultaneously satisfy following performance requirements: (i) Suppression of the short-channel effect. (ii) Sufficiently high driving capability under operating conditions. (iii) Small subthreshold swing. Another important aspect is (iv) small threshold voltage V_{th} scattering due to fluctuations in dopant concentration, which may be a major limitation for reducing the device size [1]. If (i) is optimized with a homogeneous channel doping, unacceptable deficits occur with respect to (ii), (iv) [2]. To achieve satisfactory further improvement for 100nm-MOSFETs, the importance of the channel engineering has been recognized. There are two types of such engineerings. One is in the vertical direction to the surface, and another is optimization in the lateral direction. Vertical engineering of the doping profile can improve on (iv) [3], but (ii) and (iii) are not clear. As a lateral engineering Hiroki et al. [4] have shown by simulation that a highly doped region in the channel nearer to the source improves device performances due to high efficiency of carrier injection into the channel. However, for circuit applications the S/D symmetry has to be conserved, which is often forgotten by device developers [5]. Momiyama et al. [6] have fabricated a highly doped impurity profile in the middle of the channel by tilted ion implantaion both from the source and the drain, and have shown an improvement of p-MOSFETs performance by 16%. However, (iv) may be difficult to be satisfied.

An advantage of the delta-doped MOSFET was demonstrated by Monte Carlo device simulations which predict an improvement of the transconductance up to two times [7, 8]. Especially the advantage in the transit time frequency has been emphasized. Experimental results for vertical MOSFETs with a central δ-doping (Planar-Doped-Barrier FET) simultaneously provide improved results for (ii) and (iii) [9, 10], but deficits with respect to (i) and (iv) remain. The results for (i) and (ii) are additionally not so good as expected from the theoretical calculations. The aim of this investigation is to derive a solution satisfying all four requirements by studying the experimental PDBFET results.

II. Experimental data of vertical δ-doped MOSFETs

Figure 1 shows a schematic of PDBFET [9]. Channel length and lateral doping of the fabricated vertical PDBFETs are accurately controlled by MBE (Molecular Beam Epitaxy) [11]. The doping profile along the channel, an experimental information not available for planar MOSFETs, is easily determined by SIMS analysis as shown in Fig. 2. Statistical data on PDBFETs from complete wafers are depicted in Figs. 3 and 4 for V_{th} and the drain current (I_{ds}) versus gate voltage (V_{gs}) characteristics. Figure 5 shows the dependence of the off-current (I_{off}) on V_{th}. The device parameters are the gate length L_{gate}=120nm, the impurity concentration of the substrate $N_{sub} = 5 \times 10^{16}\text{cm}^{-3}$ and the gate oxide thickness of a relatively thick value T_{ox}=12nm. The V_{th} distribution of Fig. 3 can be approximated by a Gaussian with a stan-

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 ISBN 0-7803-5974-7

dard deviation σ=0.2V. This relatively large σ-value is attributed to defects created during MBE layer growth, which emphasize redistribution of the δ-doping at higher temperatures in post-MBE fabrication processes (e. g. gate-poly activation at 770^{o}C for 90min).

III. Simulation study on central-channel engineering

Our central-channel-engineering study by hydrodynamic simulation, a precise method available at present [13], is based on above experimental data as a real-world starting point. Though Monte Carlo simulations provide more precise nonequilibrium transport, applications are still limited due to statistical deficiency especially in the subthreshold region. We can assume δ-doping-profile fluctuations as the source for V_{th}-fluctuations, because L_{gate}- and T_{ox}-fluctuations are small due to MBE application for L_{gate}-definition and the relatively thick T_{ox}, respectively. The small variation of the transconductance ($\leq$ 3%) additionally supports this assumption [11]. Determined doping profiles for nominal, σ^+ and σ^- cases reproducing the measured I-V distribution are shown in Fig. 6. A single Gaussian is assumed and doping dose is fixed to the fabrication value of 5×10^{12}cm^{-2}. From this firm experimentally-backed starting-point, we investigate the effects of a central-channel δ-doping in devices with parameters typical for 100nm scale lateral planar type named Delta-Doped MOSFETs (see Fig. 7) in stead of the unlimited depth of the S/D junction as shown in Fig. 1, namely T_{ox}=3nm and the S/D junction depth X_j=30nm.

Figure 8 shows simulated transconductance g_m characteristics of the device with the three profiles given in Fig. 6 with MEDICI, realizing maximum of nearly 1000mS/mm. The reduction of X_j was found to give practically no influence on $I-V$ characteristics of the δ-doped (DD) MOSFET. This is an advantage in comparison with conventional MOSFETs, where the junction reduction is

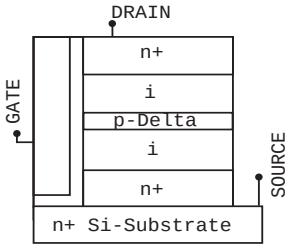

Fig. 1. Schematics of the vertical Planar-Doped-Barrier FET.

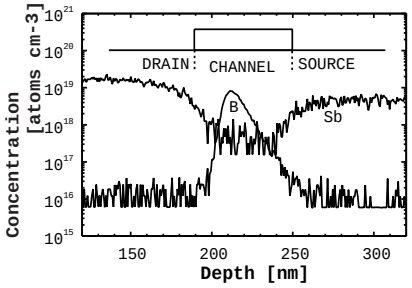

Fig. 2. SIMS measurement of the PDBFET doping profile along the channel. The channel length and the gate length are the same for this case.

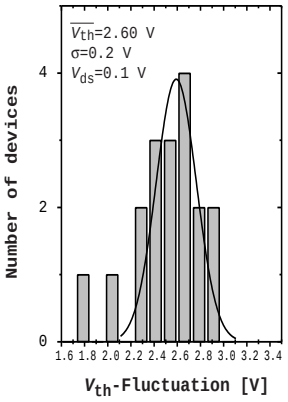

Fig. 3. Measured threshold voltage (V_{th}) distribution. The solid curve is the fitted Gaussian with an average V_{th}-value of 2.6V and a σ-value of 0.2V (σ^+ =-2.8V and σ^- =2.4V). The threshold voltage values are extracted with the gm-linear-extrapolation method [12].

required to minimize the short-channel effect [14, 16]. The reason for the negligible influence of X_j for DD-MOSFET is understood by Fig. 9, where the potential distribution along the channel surface is shown. The DD region acts as a potential barrier for the current flow below threshold condition. Therefore this region determines the V_{th} value but not the junction depth as conventional homogeneously doped devices.

As expected, T_{ox} reduction leads to substantial improvements for (iii) and also (iv) as shown in Fig.10. The standard deviation σ is reduced from 0.2V to 70mV. A reduction of the depth X_d of the δ-doping into the substrate to values smaller than the junction depth X_j=30nm is not appropriate, causing an increase of leakage current flow below the δ-doping. Due to the extremely large δ-doping-profile fluctuations of the fabricated vertical PDBFETs,

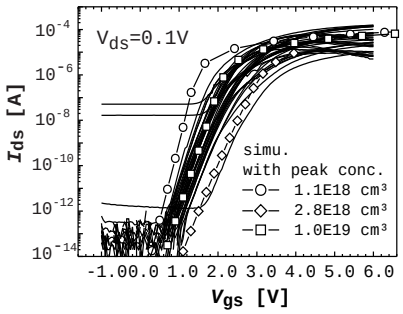

Fig. 4. Fluctuation of drain current as a function of V_{gs}. Solid lines are measurements on a single wafer. Open symbols are simulations with Gaussian for the δ-dopings, as shown in Fig. 6.

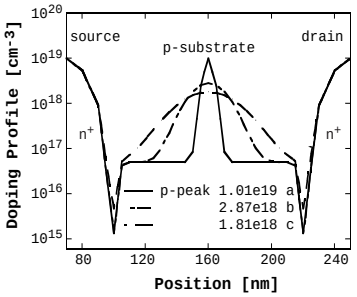

Fig. 6. Doping profiles fitted to the measured drain current fluctuation (nominal, σ^+ and σ^-) as a function of gate voltages as shown in Fig. 4.

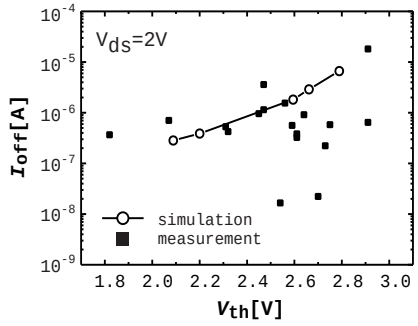

Fig. 5. Comparison of measured and simulated off-current I_{off} as a function of threshold voltage V_{th}. The drain voltage V_{ds} is fixed to 2V for sufficient magnitude of measured I_{off}.

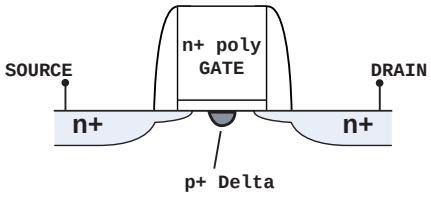

Fig. 7. Lateral MOSFET with a central-channel δ-doping.

V_{th} scattering (iv) is still larger than for a planar homogeneously doped channel with σ=35mV [2]. However, a main concern to suppress the V_{th} scattering is to minimize dopant diffusion during processes. In the PDBFET case, a diffusion fluctuation of even 50nm is observed. This can be easily improved by existing advanced technologies for shallow junction formation [7].

Since V_{th} is determined mainly by the highly doped DD region, the suppression of the short-channel effect is expected. Figure 11 shows simulated V_{th} results as a function of the drain voltage V_{ds} for two L_{gate} values in comparison with the homogeneous case. The V_{th} values are fixed to be 0.3V for both cases with L_{gate}=150nm. Enhanced short-channel effect for the homogeneous case is obvious from the larger V_{th} reduction for reduced L_{gate}. However, the V_{ds} dependence of DD-MOSFETs is much steeper than the homogeneous case. The reason is that the position where V_{th} is determined shifts to the source side by increasing V_{ds}. The V_{th} fluctuation ΔV_{th} due to the position deviation of doping peak is very small. The amount of ΔV_{th} is about -10mV for the case that the peak position is shifted from the middle to the drain or source side by 10%.

Since the DD-profile used for the simulation is relatively steep and the maximum concentration region is narrow, the position where V_{th} is determined, does not stay on the same concentration level but changes drastically according to the profile. This provides serious requirement on technology to utilize the DD-MOSFET.

Clear advantages of the δ-doping are the reduction of the subthreshold swing and the improvement of the transconductance g_m as summarized in Table1. The rea-

TABLE I
COMPARISON OF THE SUBTHRESHOLD SWING S AND THE TRANSCONDUCTANCE g_m IN THE δ-DOPED MOSFET WITH A CONVENTIONAL CASE FOR $L_{gate} = 150nm$.

	DD-MOSFET	**MOSFET**	**remarks**
S(mV/decade)	66	72	60(ideal)
g_m(mS/mm)	850	700	$V_{gs} = V_{ds} = 2V$

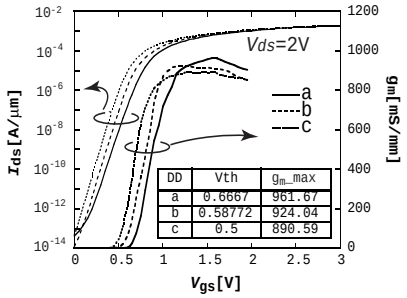

Fig. 8. Simulated transconductance g_m characteristics of DD-MOSFET for three doping profiles given in Fig. 6 with the structure shown in Fig. 7. Each line style corresponds to that shown in Fig. 6.

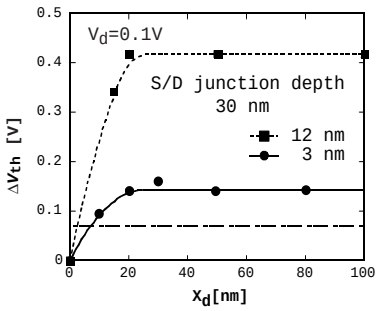

Fig. 10. Simulated threshold-voltage scattering ΔV_{th} ($=2\sigma$) as a function of the δ-doping depth for L_{gate}=120nm. The horizontal dotted-dashed line shows a published value [3] for homogeneous channel-doping and L_{gate}=100nm.

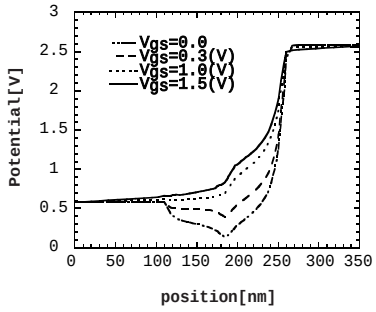

Fig. 9. Simulated potential distribution along the channel for L_{gate}=150nm with the profile of the solid line in Fig. 6.

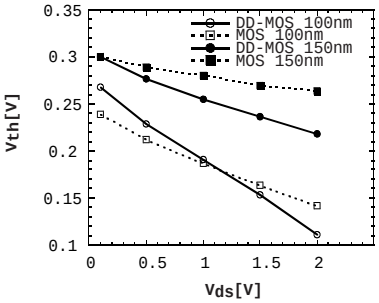

Fig. 11. Comparison of simulated V_{th} between a DD-MOSFET and a homogeneous case. The peak concentration of the DD case and the concentration for the homogeneous case are selected to result in V_{th}=0.3V for L_{gate}=150nm.

son for the former improvement is that the δ-doping acts as potential barrier, which causes the suppression of the leakage current. The improvement of g_m is due to the potential jump at the edge of the δ-doping as shown in Fig. 12. The jump results in the velocity overshoot without loosing the carrier concentration. Another advantage of the DD-MOSFET is that the nominal V_{th} can be calibrated to a desired practical value, without degradation of the driving capability by adjusting the peak concentration of the central-channel δ-doping.

IV. Discussion

In our simulation we have focused on the device size of T_{ox}=3nm and L_{gate}=150nm with X_j=30nm. For this case X_d=30nm is shown to be the solution. If the width of the δ-doping is well controlled by preventing the lateral diffusion expansion, the superiority of the δ-doping becomes more significant. Especially the velocity overshoot becomes more drastic by reducing L_{gate}, which enhances the transit speed of carriers. Figure 13 shows the output response of an inverter for L_{gate}=150nm. For the calculation the profile shown with a solid line in Fig. 6 is applied both for the n-channel and the p-channel .The simulation is obtained under the drift-diffusion approximation, since it was not possible to calculate with the hydrodynamic method, mainly due to the simulation time. To reproduce the velocity overshoot of the DD-MOSFET qualitatively with the drift-diffusion approximation, the saturation velocity was fitted to two times more than the measured value. The high transit speed caused by the velocity overshoot and the large transconductance are the reasons for the improvement of nearly 40%. The improvement of the p-channel performance is more drastic than that of the n-channel case. When reducing L_{gate} below 100nm, the improvement of the transient characteristics may be enhanced [8]. Unfortunately this calculation is not available with sufficient reliability due to the limitation of theories included into the simulator.

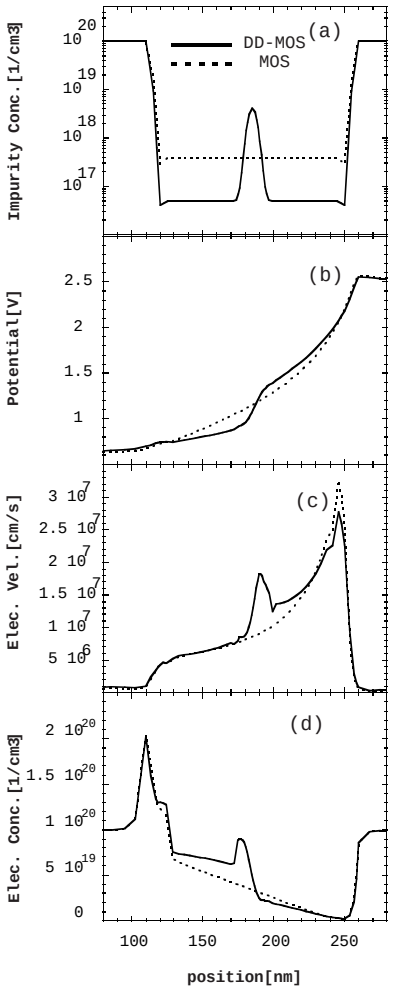

Fig. 12. Comparison of the DD-MOSFET characteristics along the channel with a homogeneous case, (a) the input impurity profile, (b) the potential distribution, (c) the velocity distribution, and (d) the carrier distribution, for L_{gate}=150nm under the condition of $V_{gs} = V_{ds}$=2V.

V. Conclusion

In comparison to presently pursued concepts for scaled planar MOSFETs, significant overall performance advantages would be enabled by the key technology of a central-channel doping. A quantitative hydrodynamic simulation study, based on experimental results for PDB- MOSFETs, verifies that all practical performance requirements would profit substantially. A main concern to realize the prediction is the necessary technology achievement for the DD fabrication. A rather shallow central-doping opens a realistic possibility for fabrication with a modified planar technology such as the focused-ion-beam implantation [17], which can keep many fabrication steps of todays conventional CMOS technologies. Here the concept originally developed as a vertical MOSFET was studied to achieve

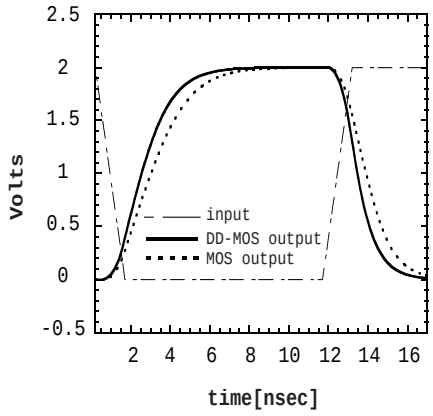

Fig. 13. Simulated response of an inverter with DD-MOSFET both for the n-channel and the p-channel . For comparison a result with a homogeneous case is depicted together. For comparison L_{gate}=150nm and V_{th}=0.3V are kept in both cases.

further improvement for the planar MOSFET. The main reason for this planarization is the difficulty of the gate-oxide formation occurred in the PDBFET. However, the conclusion given here is valid both the vertical and the planar case.

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