COMPUTER-AIDED COARSE GRID LAYOUT TECHNIQUE FOR PHOTOMASKS

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A comprehensive computer-aided mask layout technique has been developed which permits quick conversion of LSI circuits into working photomasks. It is an efficient solution to the problem when the demand for customized circuit layouts greatly overshadows the more standardized techniques. No computer background or programming experience is required. This approach allows the designer to quickly compose high-density mask layouts using simple free-hand line symbols. These easily drawn symbols, representing complex circuitry, utilize a standard device-level building block library which simplifies the conversion of LSI circuits into photomasks, and permits the designer to generate up to 100% of the layout without leaving his desk.

1. INTRODUCTION

The computer-aided coarse grid layout technique is a flexible approach with outstanding features that has been found to be invaluable when it is impractical to standardize special circuit configurations[3]. This concept facilitates the creation of customized high-density cell and die layouts through the use of a device-level building block library based on a coarse grid (>5μm) interconnect scheme. Not only does this layout technique significantly reduce the typical die design time, but it also offers the design engineer a very efficient means of interfacing with an iterative graphics design system. See Figure 1.

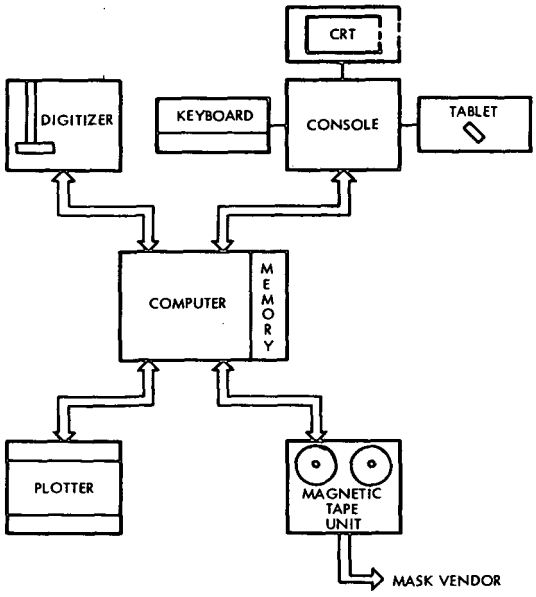


Figure 1 - Iterative Graphics Design System

2. COMMONLY USED PHOTOMASK LAYOUT TECHNIQUES

A brief description of the three most commonly used LSI photomask layout techniques is presented to illustrate some of the inherent design restrictions associated with each approach.

2.1 Standard Manual Layout Approach

Manually creating LSI photomask layouts involves the generation of master artwork at large scales to permit accurate photoreduction of the geometric details. The physical size of such drawings, some measuring up to 30 feet, are impractical to handle. It is a major task to properly check and revise these drawings, not to mention the documentation and storage requirements.

2.2 CAD Layout Approach with Standard Devices

TRW's iterative graphics design system (Applicon Graphic System/700) reduces the composition of LSI circuit layout drawings through interaction with the designer and an on-line computer. Standardized metal interconnect and device geometries are defined on a 1μm working grid and stored into the computer memory as digital information. The designer interfaces with the system through a combination of a remote digitizer and a CRT console. He then recalls copies of the required devices from the memory and positions them at specified coordinates on the master drawing file as required. The finished drawing is stored in memory until required for production of plotted drawings for record purposes, or for the generation of the magnetic tape which is sent to a photomask fabrication facility.

Although the typical LSI photomask design cycle is greatly reduced, experience has shown that there are some restrictions, as listed below, which occur once the basic drawing file is placed in the computer memory.

- It is impractical for more than one person at a time to implement changes to a particular drawing file by means of CRT editing.
- CRT editing is costly due to availability of allocated computer time.
- A change in the basic metal interconnect of device geometry usually necessitates a major drawing file redesign.
- The approximate time required for a change is inversely proportional to the basic working grid unit. A small working grid requires more time.

2.3 CAD Layout Approach with Standard Cells

Most computer-aided design systems are based on the standard cell building block concept. Groups of individual devices are combined into geometric "standard cells", such as gates and flip-flops, and stored into the computer memory. The operation of positioning and interconnecting on the master die drawing can be performed automatically or manually. This is very efficient in that the die design time is significantly reduced; however, there are some characteristics which can restrict the creative productivity of the LSI engineering group, such as:

- Fixed Cell input/output node locations.
- Fixed Cell signal and power buss line widths.
- Inefficient interconnect density due to cell interfacial restrictions.
- Generally larger die size due to internal cell restrictions.

3. CAD LAYOUT APPROACH WITH COARSE GRID

A new layout scheme is being used which eliminates these problems. This LSI photomask layout concept is actually a combination of all three of the previous layout techniques to provide a fast method of creating and revising "customized" circuit cells from scratch, using a standard devices building block library. See Figure 2.

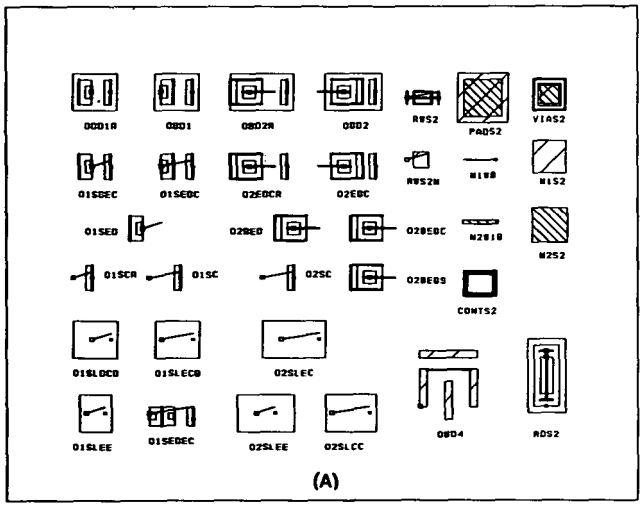


Figure 2 - Standard 5µm Grid Devices
(A) Symbolic form used in rough layouts.

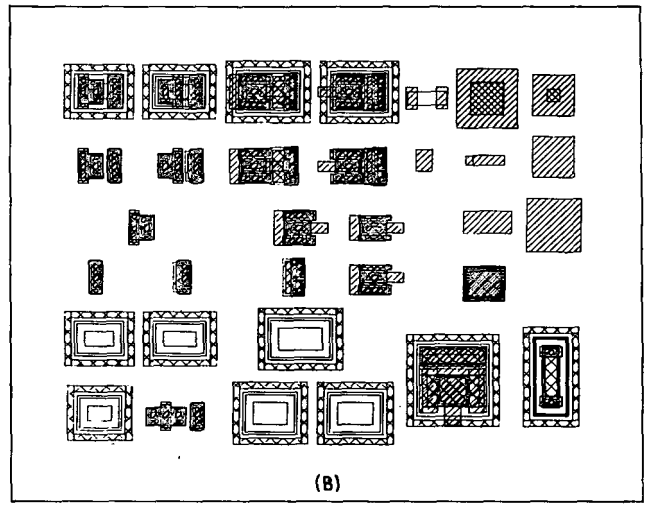


Figure 2 - Standard 5pm Grid Devices
(B) Actual device composite of all levels.

This approach basically allows the design engineer to compose his rough circuit layouts using simple line symbols to represent the devices within the circuit, and to interconnect the devices on a >5pm grid with simple point-to-point lines, representing metallization, as required. Figure 5A shows a typical rough (free-hand) cell layout. This rough layout is then digitized directly into position on the master drawing file of the computer memory.

The degree of efficiency in using this technique depends on the degree of compromise in obtaining a practical rough layout grid. Three problems were successfully solved during the development of this technique:

- Determination of appropriate grid for rough layout,
- Definition of devices such that a symbolic interconnect centerline falls on the 5pm grid, and
- Generation of 5um grid device spacing guide.

3.1 Determination of Grid for Rough Layout

Two factors were responsible for the decision to select a practical rough layout grid size with increments of 1/10 inch = 5m and 1/2 inch = 1 mil (by definition). First, dimensional criteria established Metal-1 (first of two metallization levels) width to be 8um minimum, and metal-to-metal spacing to be 2um minimum. The centerline-to-centerline spacing of Metal-1 is 10um minimum. Metal-2 (second metallization level) minimums are 18um width and 7um spacing, with centerline-to-centerline spacing of 25um.

The second reason for selecting this particular grid was based on experimentation with various digitizers. It was found that internal command recognition restrictions made it difficult to digitize from a rough layout and accurately position the devices on specified coordinates when the grid spacing was less than 1/10 inch.

3.2 Definition of Device with Symbolic Centerline

A family of standard devices has been created with all levels defining each device associated with a centerline on the 5um grid, even though some actual geometries are designed to the nearest 1/4um (Figure 2B). Each device has its own unique symbolic centerline arrangement to permit device recognition. This is necessary when the design engineer generates his rough layout, and later when the circuit is digitized into the master drawing file of the computer memory.

3.3 Guide for 5 Grid Device Spacing

The 5pm device spacing guide (See Figure 3) is an essential aide required during the composition stage of a circuit layout. It shows the minimum spacing relationship of all possible device configurations and combinations. Each device has four positive reference code points. These code points, located along the left side and bottom borders of the spacing guide, are cross-referenced to obtain the minimum grid spacing. This particular guide shows how 11 basic devices can be arranged in 526 different positions, accounting for every practical arrangement required during an average die design.

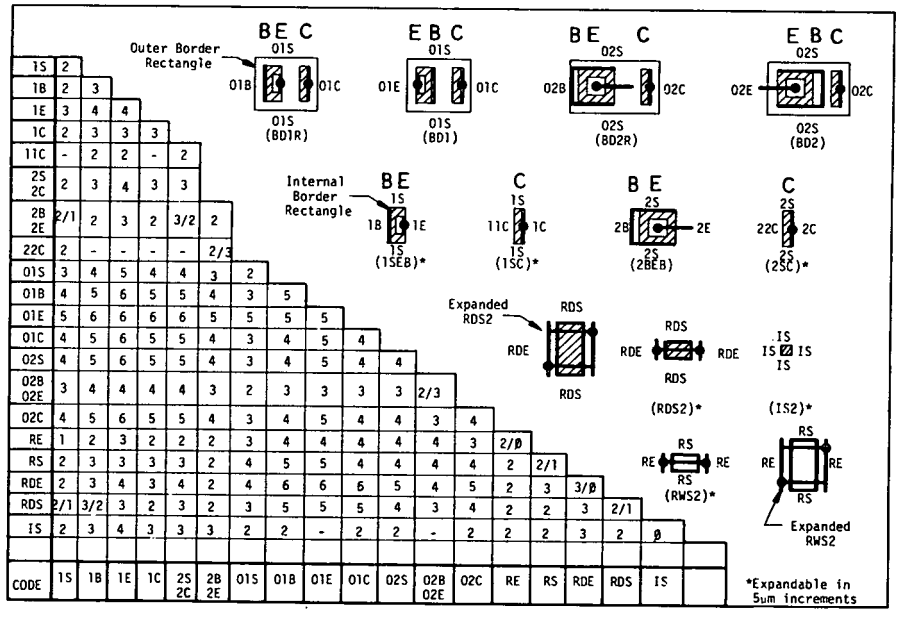


Figure 3 - Guide for 5um Grid Device Spacing

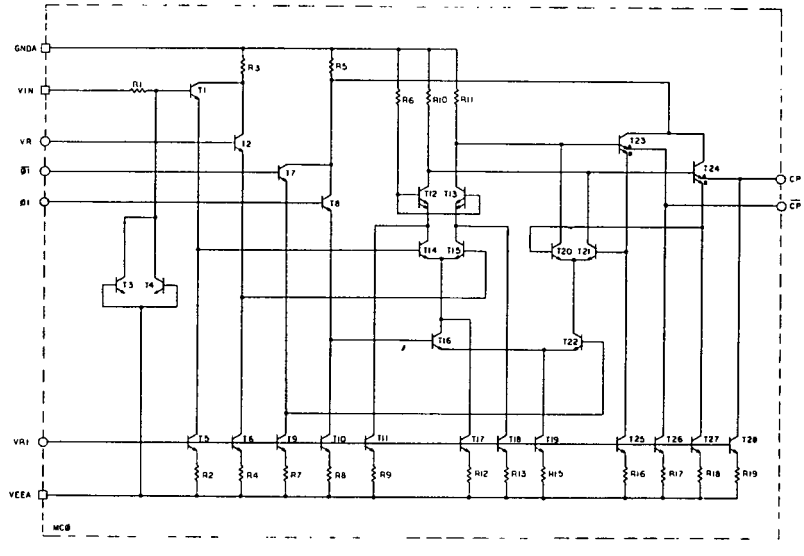


Figure 4 - Basic Cell Schematic Diagram

4. APPLICATION OF 5um GRID IN A TYPICAL DIE DESIGN

Initially, the designer verifies compliance with five basic prerequisites before beginning the actual layout.

- Circuit is logically divided into blocks of cells at 125X with preliminary bussing diagrams.
- Schematics contain all the necessary information, denoting special constraints, matched pairs, high current devices, etc.
- Rough stick figure interconnect drawings establish interface requirements.
- Signal interconnect is established to be on Metal-1 whenever possible.
- Buss interconnect is established to be on Metal-2 whenever possible.

After the basic prerequisites have been satisfied, each cell layout in a typical die design involves the following six steps:

Step 1 The design engineer obtains a standard device handbook for the applicable technology and makes same size copies of the 500X 5um grid devices (Figure 2A) and the 5um device spacing guide (Figure 3).

Step 2 The layout is created on stabilized, reproducible 1/10 inch (transparent) grid paper in free-hand sketch style. The 500X device template is slid into position under the grid paper, allowing the design engineer to quickly outline the applicable symbols as required. The devices are interconnected on the 5um grid using a solid line to represent Metal-1, and a dashed line to represent Metal-2 (Figure 5A). The cell circuit layout terminates at logical interface points.

Step 3 Reference designators are assigned to each component in the circuit layout in accordance to the schematic diagram (Figure 4). Length adjustments are indicated for each resistor that must be adjusted tighter than the 5um grid permits.

Step 4 The approved layout is directly digitized into position on the master drawing file of the computer memory. This is accomplished through the use of a digitizing procedure built around a simple point-to-point single stroke coordinate system. The starting reference point (dot on left side of device--Figure 3) locates the device and the second reference point (dot on right) orientates and stretches the geometry as desired. Single dot devices are assumed to have a second reference point one grid increment to the right of the starting point dot (by definition).

Step 5 A 500X symbolic check plot (Figure 5B) is generated from the computer memory and compared with the initial rough layout (Figure 5A). The rough layout and the symbol plot are superimposed over a light table and checked for differences--the fastest method of finding digitizing errors. Finally, a complete composite is generated (Figure 5C).

Step 6 Intermediate die plots are generated at 125X and/or 250X as the various cells are digitized into position on the master drawing file. These plots are checked to verify that the peripheral components and circuitry cells are progressing as planned per basic prerequisites. After the design is completed and approved, the stored digital information is copied onto a magnetic tape and sent to a photomask fabrication facility.

5. ADVANTAGES OF COARSE GRID APPROACH

This technique offers an efficient solution to the problem when the demand for customized circuit layouts is greater than the more standardized techniques[2,3]. Some of the outstanding advantages are listed below:

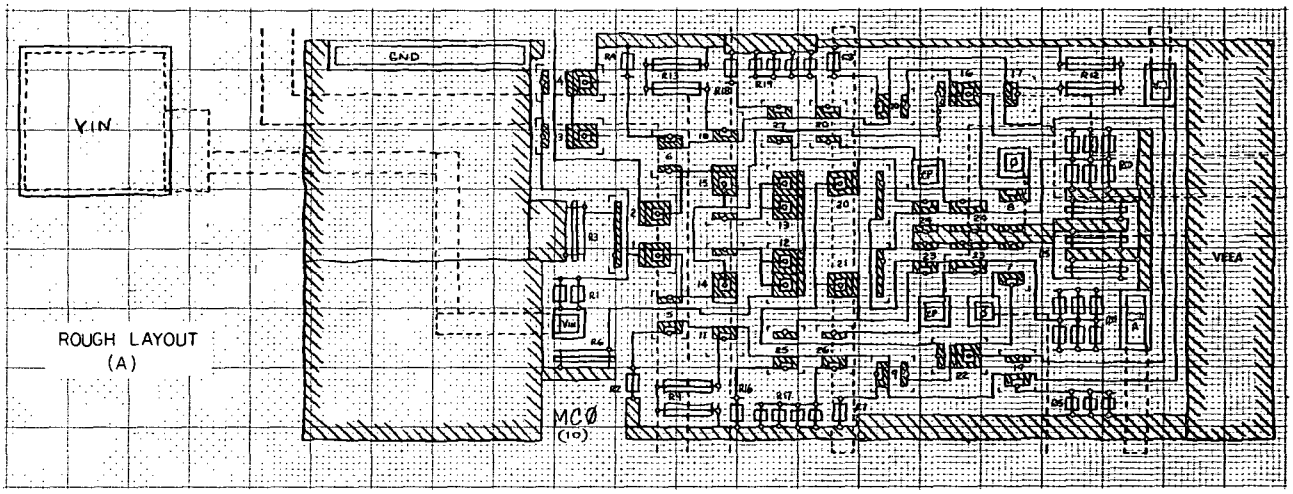
- No special computer background or programming knowledge is required.
- Simple line device symbols permit generation of free-hand circuit layouts, representing complex circuitry, which can be digitized directly into position on the master drawing of the computer memory.
- Digitizing time of an average layout is reduced from several days to a couple of hours.
- Symbolic plots reduce the average plot time of a typical cell from one hour to 15 minutes.
- CRT editing is reduced to a minimum by virtue of the efficient manner of placing the cell layout information into the master drawing file of the computer memory.
- Changes are easily implemented and seldom necessitate major drawing file redesign.
- Final layout check procedure is compatible with automated evaluation techniques.

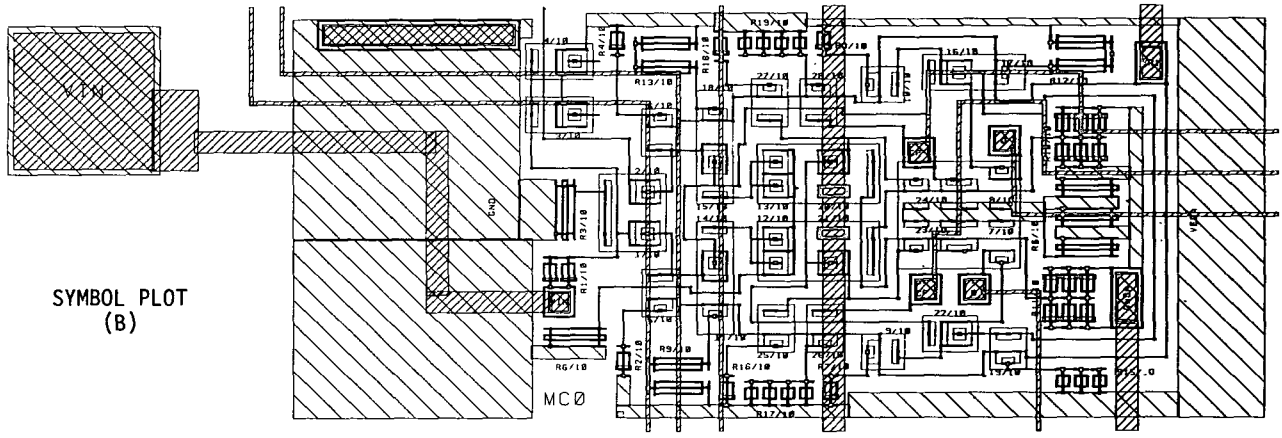
6. OTHER APPLICATIONS OF COARSE GRID APPROACH

This technique can be easily extended to other graphic applications. The process is similar to LSI approach in that the devices are created with symbolic centerlines falling on a desired grid. Then a border rectangle is placed around the centerline establishing a unique identification symbol with four positive reference code points (Figure 3). The spacing increments are determined to be the minimum coarse grid spacing acceptable between any two positive reference points.

Some of the other graphic application areas which would benefit from this approach are listed below:

- Printed circuit layouts.
- Multilayer circuit layouts.
- Thick and thin film hybrid circuit layouts.





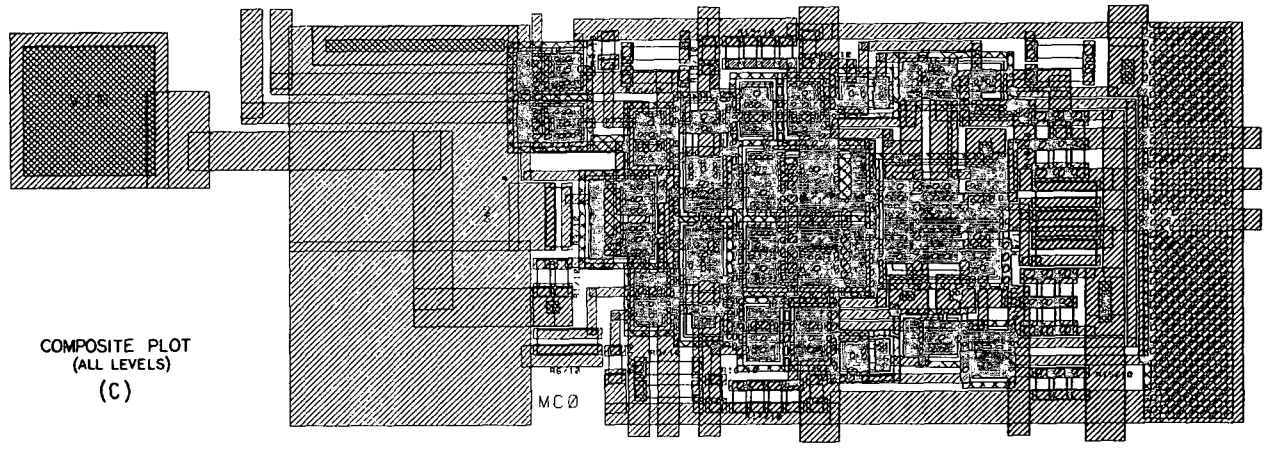


Figure 5 - Typical Cell Layout
(A) Initial Rough (free-hand) layout
(B) Symbol Plot at Same Scale as Rough Layout
(C) Composite Plot of all Levels Within Cell

7. SUMMARY

The computer-aided coarse grid layout technique has been successful in reducing the design time of customized high-density cell and die photomask layouts. Demonstrations have shown that the overall photomask layout time has been reduced by more than 400%. This asset improves die quality by permitting more time to be devoted to circuit function design effort. The design engineer is provided with a simplified layout concept which facilitates quick conversion of LSI circuits into photomasks. This technique reduces the typical die design time through the use of a standard device-level building block library, and it allows the designer to generate up to 100% of the circuit layout without leaving his desk.

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