AN INTRODUCTION TO CHDL (COMPUTER HARDWARE DESCRIPTION LANGUAGES)

The 1975 International Symposium on CHDL and Their Applications, co-sponsored by SIGARCH, SIGDA, IEEE Computer Society, City University of New York, and in co-operation with Utah State University has been held in New York City during September 3-5, 1975.

Dr. K.E. Iverson (IBM Fellow) was the keynote speaker, and Dr. H. Fleisher (IBM Fellow and IEEE Fellow) spoke at the banquet on "Science and Technology in the Academic and Industrial Worlds."

Computer hardware description languages (CHDL's) can be defined as languages for describing, documenting, simulating, and synthesizing digital systems with the aid of a computer. The main purposes of this symposium are to bring together experts in CHDL's and people who are interested in using CHDL's in various applications such as analysis, synthesis, and documentation of digital systems at the system and/or logic level(s).

Computers have been found to be a very effective tool for aiding the design of digital systems. Therefore, the area of design sutomation has received a great deal of attention. The task of designing a digital system can be considered as consisting of the following steps:

(1) The generation of a system diagram from the specifications of the system to be designed.
(2) The production of detailed logic diagram for each subsystem.
(3) The partitioning of the logic diagram into several units.
(4) The assignment of integrated circuits chips for implementing each unit.
(5) The placing of chips on logic cards and of cards on boards.
(6) The interconnecting of the chips.
(7) The testing of the integrated circuit boards.

Computers have been widely used for aiding steps 4 to 7. A total design automation system requires that steps 1 to 3 be automated. CHDL's can be used for aiding system and logic design as well as partitioning a digital system. A designer can use a CHDL to express his design and leave the tedious uninteresting computations to a computer. Recently there has been an increasing interest in CHDL's because they can bridge the important gaps in design automation.

The process of automated logic design may consist of the following steps:

(1) A designer expresses his design in a CHDL by writing a program consisting of the language statements.
(2) A hardware compiler (translator) checks the syntax of the language statements and reports the errors to the designer for correction. After the errors are corrected, the translator produces a data base to be used by the system simulator and the logic synthesizer.
(3) The system simulator verifies the design at the system level. This will save the large amount of computing time used for simulating everything at the detail gate level. If the system performance is unsatisfactory, the design language statements are modified. If the performance is satisfactory, the next step is taken.
(4) The logic synthesizer (a program) uses the data base produced by the translator, accepts the types and constraints of logic components, and produces a logic diagram.

Papers presented in this symposium covered the areas of new CHDL's, compilation and simulation driven by CHDL's, CHDL's in design automations, applications of CHDL's, as well as structured description of digital systems. In addition, there were tutorial sessions dealing with analysis and synthesis of a system. One panel discussion dealt with the future of CHDL's. Another covered the use of CHDL's as the input to design automation systems. There were also two sessions for presenting the most recent results and new concepts which are not fully developed.

Copies of the proceedings can be obtained from either ACM, 1133 Ave. of Americas, New York, New York 10036 or IEEE Computer Society, 5885 Naples Plaza, Suite 301, Long Beach, California 90803.

STEPHEN Y. H. SU, Chairman
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