A SIMPLIFIED SIX-WAVEFORM TYPE METHOD FOR DELAY FAULT TESTING

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Abstract: A new, simplified waveform method is presented for delay fault testing. The method enables accurate calculation of a delay fault detection threshold for definitely detectable faults, and a delay fault range for possibly detectable faults. The method is shown to correctly classify definitely detectable faults which are mis-classified by methods recently reported elsewhere[1,2]. A quantitative delay fault model with variable fault size is used, and the effect of the delay fault is explicitly described by the new waveform method. The calculation of the detectable delay size threshold occurs in linear time for any definitely detectable fault.

I. INTRODUCTION

Delay fault testing becomes increasingly important in the certification of high-performance VLSI circuits as tighter performance specifications leave relatively low margins for delay variations along critical timing paths. Delay faults may occur when process variations affect propagation delays of gates while not necessarily causing detectable stuck-at-faults. Conventional tests for stuck-at faults do not always detect the presence of delay faults because the size of the delay fault in relation to the fault observation time can mask the presence of the fault.

There are two kinds of delay fault models proposed in the literature, the gate delay fault model [3-5] and the path delay fault model [6]; several test generation methods have been presented for detecting delay faults [2,6,8-11]. Recently, the size of detectable faults has been proposed as a measure [1,12] of the quality of test patterns for delay faults.

A quantitative model for delay faults was introduced in [7], and a simplified waveform method was developed and used for delay fault simulation and test generation [1,2,7]. This simplified waveform method represents circuit waveforms in terms of only two-states, 0 and 1. Investigation has shown that this method does not explicitly consider the propagation of the fault through the circuit; as a result, the method: i. classifies some "definitely detectable" faults as being only "possibly detectable", and ii. determines a pessimistic threshold for definitely detectable faults.

We introduce in this paper a new, simplified six-waveform-type method for delay fault testing. This scheme explicitly describes the propagation effect of the delay fault, and, as a result, is able to definitely detect some faults which would only be possibly detectable using the two-state waveform method [1,2]. Our method calculates a detectable delay size threshold, ϵ, such that a delay fault is definitely detectable if its size exceeds ϵ. Unlike the pessimistic threshold calculated with the two-state waveform method, the value of ϵ calculated by the six-waveform-type method is accurate. In addition, the timing calculations required by this method are claimed to be much simpler than those in the two-state waveform method. Lastly, we are able to easily calculate a fault size range prescribing "possibly detectable" delay faults. In section II, two examples are given to show the drawbacks of the two-state waveform method. Section III presents the new method. In section IV, examples are given to demonstrate its merits. Section V presents conclusions.

II. DRAWBACKS OF THE TWO-STATE WAVEFORM METHOD

We consider combinational circuits consisting of AND, OR, NAND, NOR and NOT gates, and restrict our attention to single gate delay faults with variable size, δ. A test to detect a gate delay fault requires application of a pair of test patterns (T1, T2). T1 is first applied to the circuit to establish initial signal states. Then T2 is applied to sensitize the delay fault and propagate the effect of the fault to at least one of the outputs. The output will be observed at a certain time, t_{obs}. For a given observation time it is therefore important to determine detectable fault sizes. It is assumed that the fault-free circuit reaches and remains in a stable state for $t \geq t_{obs}$.

Now consider the slow-to-fall fault on line b of Fig. 1. A test to detect this fault must first create a logic value of 1 at b, and then drive b to a value of 0. The presence of a delay fault at b is to be inferred from the waveform observed at output d.

Suppose that the observation time has been set to $t_{obs} = 4$. The two-state waveform method would claim that a delay fault at b is only possibly detected by this observation because the initial logic state caused by applying T1 and the final observed logic state caused by T2 are the same at output d. However, careful analysis of the waveforms reveals that the delay fault can be definitely detected by the observation at time $t=4$ if $\delta > 1$. It is characteristic of the two-state waveform method that some definitely detectable faults are classified as possibly detectable faults. This will be shown

to be due to the method's failure to adequately describe the propagation behavior of the delay fault.

Now let us consider the problem of determining the detection threshold, δ. In Fig. 2, assume that line b has slow-to-rise fault and lines a and b have transitions from 1 to 0 and 0 to 1 at time 0. Assume that $t_{obs} = 9$. Using the two-state waveform method, the threshold, ϵ is calculated as

$$\epsilon_2 = t_{obs} - EA^* + \delta^* = 9 - 1 + 0 = 8$$

where EA* and δ^* are obtained according to the "last segment approximation" scheme of [1].

It is easy to confirm that any fault at b with $\delta > 1$ can be detected because the fault propagation path b, b1, c and d is the dominating path that ultimately determines the behavior of the output signal in the presence of the delay fault. Line c will change from logic value 1 to 0 at t = 7 and keep logic value 0 until after t = 8 if $\delta > 1$. Therefore, line d will keep its initial logic value, 0, until at least t = 9. So, the threshold is $\epsilon = 1$ instead of the previously calculated $\epsilon_2 = 8$.

This example also shows another drawback of the two-state waveform method -- it does not explicitly consider the propagation path of the fault. As a result, using EA and LS values determined by fault size but not by propagation dynamics requires complicated calculations and causes pessimistic results.

III. SIX-WAVEFORM-TYPE METHOD

A "waveform type" method is now introduced to address the deficiencies of the two-state waveform method. Six waveform types are used to provide a description of waveform behavior, but without explicit timing information. The waveform of each line is also represented by a six-tuple containing waveform type and timing information. This provides a uniform description of the waveform behavior in the fault-free and faulty circuit. It also supports explicit propagation of the effect of the delay fault.

WAVEFORM TYPES For the purpose of delay fault detection the line waveforms affected by the fault can be considered to be a member of the waveform-type set, S, where S = {0, 1, R, F, 0*, 1*}. Here a symbol used to denote a particular waveform type does not have the same meaning that it does in logic simulation or in timing verification. Instead, a symbol provides a simplified summary of the behavior of an entire waveform, rather than indicating the logic value of the waveform at a single point in time.

The members of S are described below:

0 (1) represents a type of waveform having a stable logic value 0 (1);

R (F) represents a waveform having a transition from 0 to a final value of 1 (from 1 to a final value of 0), with the transition occuring during an uncertainty interval denoted by T_U when $\delta > 0$.

0* (1*) represents a waveform having a final value 0 (1) with a hazard occurring over an interval of uncertainty denoted by T_U when $\delta > 0$.

The six waveform types are shown in Fig. 3. Note: the starting time of the fault effect, T_{FES}, is the earliest time at which a transition may occur in the faulty component of the waveform with $\delta = 0$. The time period in which the waveform's logic value is uncertain is denoted by T_U. Rules for calculating T_{FES} and T_U will be given later.

The circuit's behavior in the presence of the delay fault can be "simulated" using a novel "waveform-type logic" shown in Fig. 4. This logic determines the type of the waveforms on each line, without determining the times at which logic transitions actually occur. For example, for an AND gate, if $\delta > 0$ application of a type-R and a type-1 waveform creates a type-R output waveform. The output will undergo a 0 to 1 transition. Depending on t_{obs} and δ, this transition may or may not be apparent in the observed waveform. Notice that applying type-R and type-F waveforms together create either a type-0 or a type-0* output waveform. This corresponds to there being a steady 0 at the output, or a hazard followed by a final value of 0, depending on the relative edge transitions of the input signals and the effect of the fault.

Only six waveform types are used to represent the behavior of the circuit with the delay fault. For the fault-free circuit, these six types can be mapped into two waveform types

WAVEFORM-TYPE DESCRIPTOR Let FL be a line with a delay fault, and let d_r and d_f be the rising and falling delays of a gate.

Definition 2: The precedent line set (PLS) of a faulty line is a set of lines connected to FL by a forward-propagating path.

Definition 3: The descendent line set (DLS) of a faulty line is the set of lines connected to FL by forward-propagating paths from FL.

Note that the only line common to the PLS and the DLS is FL.

To detect a delay fault using a quantitative fault model, we need to describe the qualitative faulty and fault-free behavior of the circuit using the waveform types, and also determine when a line's signal leaves its initial state and when it reaches its final state. In addition to having a type, the signals at the lines of a circuit each have a 6-tuple waveform descriptor. The waveform-type descriptor of line l, WT(l), is defined by $WT(l) = (WT_I(l), WT_F(l), TK(l), TA(l), T_{FES}(l), T_U(l))$ where,

$WT_I(l) \in \{0, 1\}$ is the initial waveform type (caused by T1);

$WT_F(l) \in \{0, 1, R, F, 0^*, 1^*\}$ is the waveform type caused by T2 - note that the final waveform logic value is implicit in WT_F;

TK(l) is the longest time that the line keeps the logic value implied by its initial waveform type if the line is in the PLS;

TA(l) is the latest time that the line waveform arrives at the final logic value (0 or 1) implied by its waveform type if the line is in the PLS;

$T_{FES}(l)$ is the starting time of the fault effect for a waveform having $WT_F(l) \in \{R, F, 0^*, 1^*\}$;

$T_U(l)$ is the time period of uncertainty for a waveform having $WT_F(l) \in \{R, F, 0^*, 1^*\}$.

$T_{FES}(l)$ and $T_U(l)$ are only calculated for lines belonging to the descendent line set.

Now we will indicate how to calculate the components of the waveform-type descriptor. For an AND gate with n inputs $x_1, x_2, \ldots, x_n$ and an output y,

$WT(y) = (WT_I(y), WT_F(y), TK(y), TA(y), T_{FES}(y), T_U(y))$.

The operations to obtain $WT_I(y)$ and $WT_F(y)$ for an AND gate are shown in Fig. 4. When a table entry indicates a choice between two items, the one assigned to a line depends on the timing calculation.

For the faulty line FL, if $WT_I(FL) = 0$ (1), $WT_F(FL) = 1$ (0) and the delay fault is slow-to-rise (slow-to-fall) then R (F) is assigned to $WT_F(FL)$.

The formula to calculate TK(y), TA(y), $T_{FES}(y)$ and $T_U(y)$ for an AND gate are as follows. Preliminary values are calculated for members of the precedent line set:

$$\text{preTK}(y)=\begin{cases}\max\{TK(x_i)+d_r\} \text{ if } WT_I(x_i)=0, \\ \quad \text{for some } i \in \{1,...,n\} \\ \min\{TK(x_i)+d_f\} \text{ if } WT_I(x_i)=1 \text{ for all } i.\end{cases}$$

$$\text{preTA}(y)=\begin{cases}\min\{TA(x_i)+d_f\} \text{ if } WT_F(x_i)=0, \\ \quad \text{for some } i \in \{1,...,n\} \\ \max\{TA(x_i)+d_r\} \text{ if } WT_F(x_i)=1 \text{ for all } i.\end{cases}$$

Then the preliminary values are used:

$$TK(y)=\begin{cases}+\infty \text{ if preTK}(y) > \text{preTA}(y). \\ \text{preTK}(y) \quad \text{otherwise.}\end{cases}$$

$$TA(y)=\begin{cases}-\infty \text{ if preTK}(y) > \text{preTA}(y) \\ \text{preTA}(y) \quad \text{otherwise.}\end{cases}$$

For the line which does not belong to the precedent line set, TK(y)=TA(y)= -, where "-" means don't care.

Next, we consider the descendent line set. If $WT_F(FL)$ is not R or F, the fault is not sensitized, otherwise $T_{FES}(FL)$ = TK(FL) and $T_U(FL)$ = TA(FL)-TK(FL).

For the line y with $WT_F(y) \in \{R, F, 0^*, 1^*\}$ or $WT_F(y)$ requiring choice between 0 and 0*,

$$T_{FES}s(y)=\begin{cases}\max\{T_{FES}(x_i)+d_r\}, \text{ if } WT_F(x_i) \in \{0^*,R\} \text{ for some } i \\ \min\{T_{FES}(x_i)+d_f\}, \text{ if } WT_F(x_i) \in \{1^*,F\} \text{ and there} \\ \quad \text{is no } x_i \text{ with } WT_F(x_i) \in \{0^*,F\}.\end{cases}$$

$$T_{FES}f(y)=\begin{cases}\min\{T_{FES}(x_i)+d_f+T_U(x_i)\}, \text{ if there is at least one} \\ \quad x_i \text{ with } WT_F(x_i) \in \{0^*, F\}. \\ \max\{T_{FES}(x_i)+d_r+T_U(x_i)\}, \text{ if } WT_F(x_i) \in \{1^*, R\} \\ \quad \text{and there is no } x_i \text{ with } WT_F(x_i) \in \{0^*, F\}.\end{cases}$$

$$T_{FES}(y)=\begin{cases}T_{FES}s(y) \quad \text{if } T_{FES}s(y) <= T_{FES}f(y) \\ \text{don't care} \quad \text{if } T_{FES}s(y) > T_{FES}f(y)\end{cases}$$

$$T_U(y)=\begin{cases}T_{FES}f(y)-T_{FES}s(y) \quad \text{if } T_{FES}s(y) <= T_{FES}f(y) \\ \text{don't care if } T_{FES}s(y) > T_{FES}f(y)\end{cases}$$

For the line which does not belong to the descendent line set, the values of $T_{FES}(y)$ and $T_U(y)$ are set to -. If $T_{FES}s(y) > T_{FES}f(y)$, the choice between {0, 0*} in the waveform operation table of Fig. 4 is 0.

The calculation of waveform descriptors for OR, NAND, NOR and NOT gate can be obtained in similar way.

IV. APPLICATION

Waveform-type descriptors are used for delay fault testing.

Definition 4: A delay fault is said to be definitely detected at an output z with detection threshold ϵ if the fault-free and faulty logic value of z is different at the observation time for all $\delta > \epsilon$.

Definition 5: A delay fault is said to be possibly detected with a fault size range (a, b) at an output z if the fault-free and faulty logic value of z may be different at the observation time for all $a < \delta < b$.

For a primary output z the calculation of the detectable delay size threshold using the six waveform types, denoted by ϵ_6, is done as follows

$$\epsilon_6(z) = t_{obs} - T_{FES}(z) \text{ if } WT_F(z) \in \{R, F\}.$$

The calculation of the fault size range is done as follows,

$$T_{FES}(z) + \delta < t_{obs} < T_{FES}(z) + T_U(z) + \delta \text{ if } WT_F(z) \in \{0^*, 1^*\}.$$

Note that the calculation of these thresholds is done in linear time for definitely detectable faults because TK, TA, T_{FES}, and T_U are calculated at most once for each line.

Some faults which would be classified as possibly detectable by the two-state waveform method are classified as definitely detectable by the six-waveform-type method. This new method also provides an accurate threshold calculation.

Example: The slow-to-fall fault at line b of the circuit in Fig. 1 would be classified as being possibly detectable by two-state waveform method. Now, we show that it is definitely detectable. Assume that input a has a transition 1 to 0 at time 0 and let t_{obs} = 4. The waveform type simulation method gives:

WT(a) =(1,0,0,0,-,-) WT(b) =(1,F,2,2,2,0)
WT(a1) =(1,0,0,0,-,-) WT(c) =(0,1,-,-,-,-)
WT(a2) =(1,0,-,-,-,-) WT(d) =(0,F,-,-,3,0)

So, ϵ = 4-3 = 1. Any slow-to-fall delay fault at b with fault size larger than 1 can be definitely detected.

Example: In Fig. 2 assume that line b has slow-to-rise fault and inputs a and b have transitions 1 to 0 and 0 to 1 at time 0, and let t_{obs} = 9. The waveform type simulation method gives:

WT(a) =(1,0,-,-,-,-) WT(b2) =(0,R,-,-,0,0)
WT(b) =(0,R,0,0,0,0) WT(c) =(1,R,-,-,7,0)
WT(b1) =(0,R,-,-,0,0) WT(d) =(0,R,-,-,8,0)

So, the detection threshold is ϵ = 9-8 = 1. For the slow-to-rise fault at line b with size larger than 1, the fault can be definitely detected, and the threshold is accurate instead of pessimistic.

Example: Fig. 5 is a circuit used in [1], with line c having a slow-to-fall delay fault and t_{obs} = 11. The example is counter-intuitive because it demonstrates that detectability for a given fault size does not imply detectability of larger faults. It was shown that the fault is detectable when δ = 2 and undetectable when δ = 8 [1]. Now we use the waveform descriptor to accurately find the range of the fault size for which the delay fault is possibly detected.

WT(a) =(1,1,-,-,-,-) WT(d) =(0,1,-,-,-,-)
WT(b) =(1,1,-,-,-,-) WT(e) =(0,R,-,-,4,0)
WT(c) =(1,F,0,0,0,0) WT(f) =(0,F,-,-,2,0)
WT(c1)=(1,F,-,-,0,0) WT(g) =(0,R,-,-,8,0)
WT(c2) =(1,F,-,-,0,0) WT(h) =(0,1*,-,-,4,6)

The fault is possibly detectable if

$$4 + \delta < t_{obs} < 4 + 6 + \delta$$

or $1 < \delta < 7$. This example shows that a fault size range can be calculated accurately for the possibly detectable delay fault.

V. CONCLUSION

The waveform-type method introduced in this paper was shown to give accurate, rather than pessimistic, results in comparison to the two-state method. It correctly identifies definitely detectable faults and determines an accurate detectable delay size threshold for definitely detectable faults, and an accurate delay size range for possibly detectable faults. The delay thresholds are also calculated in linear time. The method is under further investigation for use in a test generation system.

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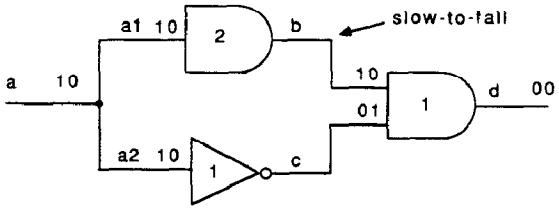

Fig. 1 Circuit with slow-to-fall fault at b

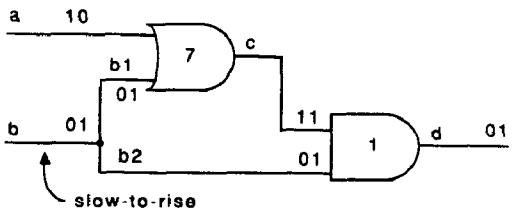

Fig. 2 Circuit with slow-to-rise fault at b

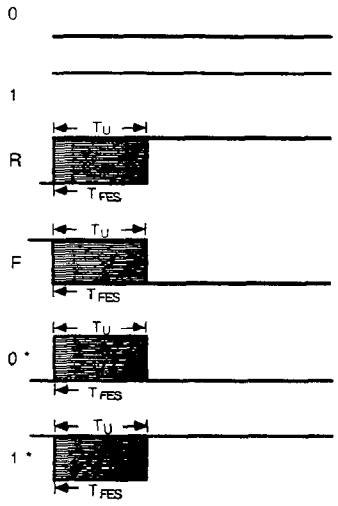

Fig. 3 Illustration of waveform types

AND	0	0*	F	R	1*	1
0	0	0	0	0	0	0
0*	0	0 or 0*	0 or 0*	0 or 0*	0*	0*
F	0	0 or 0*	F	0 or 0*	F	F
R	0	0 or 0*	0 or 0*	R	R	R
1*	0	0*	F	R	1*	1*
1	0	0*	F	R	1*	1

Fig. 4 Table of waveform type operations for two-input AND gate

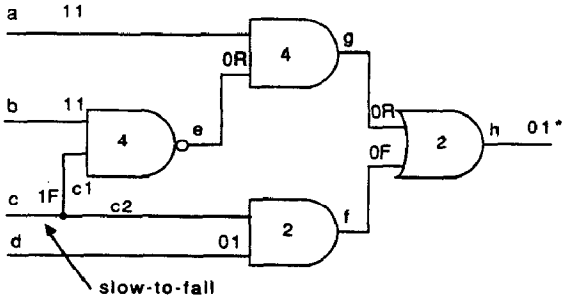

Fig. 5 Simulation of waveform types for slow-to-fall fault at c