DEVELOPMENT OF COMPUTER COMPONENTS

AND SYSTEMS

By

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1. INTRODUCTION

Work has been proceeding at Elliott Brothers Research Laboratories since 1948 on high-speed digital computing and data transmission techniques. The work was originally directed towards one particular special-purpose high-speed computing project, although it was hoped from the beginning that techniques and designs for general purpose machines would evolve naturally from the programme. Since the inception of this work there have been changes in the policy of the original project, together with additional commitments for new digital projects. Circuit and technique developments for these projects have resulted in the evolution of a range of sub-units from which a wide variety of computers may be constructed without further development.

Some parts of the work have already been reported in some detail[1],[2]. Mention of the work and aims was made at the Rutgers meeting in 1950[3]. The present paper is a progress survey and outlines future proposals for a range of packaged sub-units.

2. INITIAL WORK ON LOGICAL CIRCUIT DESIGN

The project for which the original work on circuit techniques was done required a reasonably high overall computation speed and a moderate amount of rapid-access storage space. Serial operation was chosen mainly because the most promising rapid-access storage system at the time appeared to be the Williams tube, and use of this in a parallel computer would have resulted in unnecessary bulk and over-generous storage capacity. First measurements on the system indicated the possibility of work at 660K digits/sec if the "anticipation pulse" method was used, and initial logical circuit design work was carried out at this frequency. It was proposed to obtain a high overall speed of computation in a serial machine by the use of a high-speed serial-parallel multiplier of "wiffle tree" type and to carry out simple addition by accumulation into storage locations on the CRT store. By these means an overall speed equal to that of a fast parallel machine could be achieved. The initial work on arithmetic units therefore had as its first targets (1) An adding circuit through which the overall pulse delay was sufficiently small to enable it to be included in the regeneration loop of a CRT store and (2) A compact adding circuit for the multiplier wiffle tree (which needed a total of fifteen such circuits).

Consideration of the first requirement led to a logical circuit for adding which is shown in fig.(1). It will be seen that the delay in going from Input 1 to the Sum Output is occasioned entirely by the two "anticoincidence circuits", and the best design achieved for these was a long tailed pair circuit in which simultaneous pulses are mutually cancelled. Such a circuit operates with a very small delay; the delay from input to output was measured as .07 μsecs. The circuit was operated successfully in an accumulating storage loop at 1000K digits/sec, but suffers from the disadvantage of requiring accurate pulse shape matching for satisfactory operation which is a limitation in other applications.

The design for the second target was based on the first, and an experimental 16 digit multiplier working at 660K digit/sec was operated in May 1949. In this design little attempt was made to rationalise the circuit elements, the various adders, delays, gates and staticisors were built as convenient into plug-connected chassis of the type shown in fig.2. A photograph of the experimental multiplier is shown in fig. 3.

At this stage (in September 1949) it became necessary to settle the general design of the computer, and the following decisions were made. (1) To change the digit frequency to 330K digits/sec because although the store had been operated at 660K digits/sec it was felt to have an inadequate safety factor at that speed.
(2) To construct the arithmetic units by a "printed circuit" technique, since this technique had reached a stage of development where a fairly large scale trial seemed desirable.
(3) To redesign the circuits for use with sub-miniature valves, since these had become available in pre-production quantities, and they offered the possibility of more efficient (in power consumption) circuits and more compact printed circuit layouts.

It was during the circuit redesign that serious thought was first given to the rationalisation of the circuits for economical production, and it was possible to reduce the number of designs for printed units to six.

(1) Adder plate - containing the coincidence and anticoincidence circuits of Fig.1.

(2) Delay plate - containing two identical delay circuits for performing the functions of "carry" in an adder, multiplication by two in the multiplier, "digit slip" for regenerating a distorted pulse after an adding or gating circuit and as a logical element in an order decoder.

(3) Commutator plate - containing two identical circuits of delay type, but with a simplified circuit capable of handling only single pulses in each word, and having a lower impedance output.

(4) Staticisor plate - containing two identical anode-coupled trigger circuits, for use in static registers or as scale-of-two circuits.

(5) Cathode follower plate - containing six independent cathode followers.

(6) Crystal gate plate - containing five diode coincidence gates for routing numbers under the control of three staticisors.

In addition to the six main circuits it was necessary in the computer to use seven other circuits in relatively small numbers, these were constructed by normal wiring techniques on plates which were mechanically interchangeable with the printed plates and used the same sockets. The circuits were all designed to work with H.T. supplies of + 100 and - 150V, and with a bias supply and square-wave clock supply of 6V. In the complete machine 75% of plates are of the six printed designs, the remainder being of the special types.

Photographs of a typical printed glass plate (a delay plate) and a typical wired plate (a staticisor) are shown in figs.4 and 5.

3. AN EXPERIMENTAL DATA-HANDLING MACHINE

The machine described in this section is the final outcome of the project towards which the work mentioned in Section 2 was directed. Its purpose is the analysis of large amounts of data. It is a 330K digit/sec serial machine with a word length of 20 digits, and working to an accuracy of 14 digits.

The machine comprises:-

(1) A fast multiplier capable of accepting two numbers in one word time and producing the rounded off product in the following word time.

(2) A single word accumulator consisting of a circulating loop of delay circuits with facilities for addition, subtraction, shift and collation.

(3) A double word accumulator (capacity 40 digits) for accumulating the results of analysis of large amounts of data.

(4) A rapid access store of Williams tube type with a capacity of 64 words on two tubes.

Input to the machine is by 35 mm photographic film scanned and searched under the control of the computer, the film carries thirty 14-digit numbers and their 14-digit tallies per inch. The order programme is repetitive and is scanned photo-electrically from a number of easily changed slides. Internal routing is by simultaneous multiple transfer.

As originally designed, the machine contained some 280 plates in the arithmetic and routing sections, and these were assembled in groups of eighteen in chassis which could be rapidly unplugged from their racks. Cooling of the chassis was by forced draught from ducts in the racks. The CRT stores, their address line-finders, the programme order generator, (and later the input film reader) were constructed of conventionally wired circuits on 19" racks.

The original mechanical design was unsuccessful owing to unreliability of the rack-chassis plugging, and insufficient cooling air supply which caused many printed circuit failures due to overheating. The machine was therefore rebuilt in the winter of 1950-1 with the chassis units wired in, and mounted directly on to a "wind chest" from which they obtained their cooling air. The computer was extended at the same time to a total of about 350 plates, and in addition the two accumulators were duplicated in a more conventional form of wired plate construction (Fig.6), to increase the mathematical facilities and also to afford a comparison of the reliability of the two methods of construction.

This machine has been in operation since the Spring of 1951, and we have gained considerable experience of its use (about 1500 hours' running, including development time). The arithmetic units and the store have proved somewhat susceptible to interference due to other electrical equipment in the building, and the printed circuits have given rise to significantly more troubles than the duplicate circuits constructed more conventionally. The interference problem has been tackled in the design of the newer circuit units described below; the weaknesses in the printed circuits have been noted and are not regarded as insuperable, but a report of the work on printed circuits is outside the scope of the present paper.

The present state of serviceability of the machine as described is of the order of 50% (on a useful time basis); the usefulness of the system is limited at present by defects in the original film recording. An investigation of these defects and possible ways of overcoming them is being carried out.

4. IMPROVED LOGICAL CIRCUITS

A series of new logical-circuit designs has been developed, based on experience with the earlier units and working at the same speed of 330K

digits/sec. The design of these units will be fully reported later by their designer, C.E.Owen, but a brief outline of their design philosophy, will be given here.

(1) Larger amplitudes of square-wave clock and bias are used (10V in place of 6V). Valves in the quiescent state are then well beyond their cut off, and much higher levels of interference can be tolerated before spurious pulses are generated.

(2) There is no longer a requirement for adders to work in CRT storage loops, so that it is possible to do all logical operations by means of crystal coincidence and mix circuits. (The operation "not" is performed by a coincidence with an inverted pulse at a suitable DC level).

(3) Signals are both routed and applied to logical circuits as pulses which are of greater amplitude than, and overlap in time, the clock pulses. Distortion of the pulses is unimportant since the effects may be removed by gating with clock before the signals are passed into a delay or a storage system.

(4) The delay circuit output is produced from a pulse lengthener, which is reset by a common reset pulse provided from the clock pulse generator. This minimises the use of frequency sensitive elements to provide correct delay times.

(5) The DC-coupled trigger circuit is no longer used as a staticisor. This circuit had proved particularly sensitive to triggering by interference. Its place as a one digit memory element is taken by a delay circuit circulating upon itself through a coincidence gate and mix circuit. Circulation may be started through the mix circuit, and inhibited by applying an inverted pulse to the coincidence gate.

This philosophy has resulted in the design of three basic circuit elements (two of four pentodes each, and one of two pentodes) by which all the logical, decoding and routing operations in a computer may be carried out. Only one valve type, the Mullard EF 73 is used. The price paid for this rationalisation is a small redundancy of components (about 2% of valves and 14% of crystal diodes in a typical application).

Work is now in hand on the engineering of these circuits for processed production, (Fig.7) and the design of a system of water cooled racking for them using "closed circuit" air ventilation, but the circuits themselves have been tried out in "bread-board" form as described in Section 6.

5. RECENT WORK ON STORAGE

The early data-handling machine (Section 3) used an anticipation-pulse Williams tube store at 448 digits per tube and 330K digit/sec. This store has been in operation for 2½ years. It has been quite workable and in general reliable. There have been periods when it was rather sensitive to interference and phoney-free tubes have not been freely available.

With the announcement of Perry's results on defocus-focus operation, M.V.Needham at Elliotts started designing a new CRT store on that principle, for our 330K digit/sec serial system. This design is going on now.

For general and special purpose machines requiring large main storage, research on the magnetic drum type of store was started in 1950 by R.C.Robbins and P.D.Atkinson. A prime requirement was to maintain the system digit rate of 330K digit/sec and this seems to have been achieved in a design for a magnetic disc store by P.D.Atkinson reported at the Pittsburgh meeting. A high peripheral speed is used making the 3/us digit time feasible and at this speed the disc is preferred to a drum.

Concurrently development of the delay type of store using the magneto-strictive effect in nickel wire was proceeding and has been shown to be thoroughly practical and very simple. Delay times are limited so far to about 1½ mS. Very large storage capacity is not practicable with the magneto-striction delay store, but it is especially attractive for single-word registers in arithmetic units and for small immediate-access stores. The technique has been developed by De Barr and Millership and was described in the same paper at Pittsburgh.

Future work on storage will be a continuation of the magnetic disc development and an attempt to operate the magnetostriction units at longer delays and with less electronics per unit.

6. APPLICATIONS OF THE NEW CIRCUIT ELEMENTS

The three new logical-circuit elements are being used in two machines at present under construction. The first of these is a large special purpose machine, having a large magnetic disc store in addition to a rapid access Williams store (of the type under development by M.V.Needham). Data input is by teleprinter tape, and output by teleprinter, and orders are stored permanently on the magnetic disc. The arithmetic units are a high speed multiplier and a circulating accumulator and multiple transfer is used.

The complete machine will use a total of 360 of the circuit units which will be of the fully-engineered form in water-cooled racks. In the meantime, to gain experience of inter-unit wiring and cable-form design a "bread-board" version of the arithmetic units has been built, using simple wooden racking and circuits wired on paxolin strips. (Figs.8 & 9). The cost of this bread-board is considered worth while to avoid modifications in the wiring of the final racking.

The second machine using these circuits is a small general purpose computer, which is being constructed in bread-board form to meet an urgent requirement for certain computations to be done and thereafter for general mathematical use. This machine has a main store consisting of magneto-

striction delay lines and capable of holding 1024, 32-digit words with an access time of about 12 mS.

The arithmetic unit contains about 75 plates of the "bread-board" type to do all the logical and gating operations except the gating inside the store loops.

7. FURTHER WORK ON PACKAGED UNITS DEVELOPMENT

Development work now in progress is aimed at the production of a range of plug-in units from which nearly the whole of any serial working computer at a 330K digits/sec rate may be constructed from the logical diagram without further engineering work. These units are being made in the laboratory using conventional components and wiring, and standard commercial connecting plugs (Fig.10). They are suitable for production in their present form and it is hoped to engineer them for processed circuit manufacture later.

Designs already completed are:-

(1) A variation of the three basic logical circuits using miniature valves instead of subminiatures, since in Britain these are at present more readily available and are very much less costly.

(2) Four units for generating clock and reset pulses. These comprise an oscillator plate, a squarer plate, a pulse generator plate for forming reset pulses or strobing pulses from the square wave, and a low impedance output plate. (The number of output plates used in any computer depends upon the load imposed by the logical circuits).

(3) Three plates forming the basis of a 32 digit accumulator register. These consist of a plate carrying a robust magneto-striction nickel delay line, a plate carrying the accompanying amplifier and regeneration circuits, and a plate carrying the input drive circuits. A photograph of these plates together with the logical plates required for the accumulating adder is shown in Fig.11.

Further designs to be undertaken on these units will be the amplifiers and gating circuits required for reading and writing with the magnetic disc, and also certain D.C. control circuits associated with fusing and protection of the various units of the computer.

The circuits described in this section are being tried out in a Mk I general purpose computer which is designed to contain the minimum of hardware consistent with simplicity of logic and ease of maintenance. The main store of this machine will be a 330K digits/sec magnetic disc with 8 heads available for storage, and others to provide clock and address tracks. The drum speed will be 75 R.P.S., giving a capacity of 1024, 34-digit words. Input will be by teletype tape, and output by an electrical typewriter. It is hoped that the whole of the circuitry of the machine with the exception of power supply, drum drive, and input/output mechanism will be on the standard range of plug-in units.

The machine will probably contain a total of 180 packaged units of standard size of which about 110 are logical circuits. These will occupy about three seven foot cabinets. The rest of the machine (the power supply, the magnetic disc and its accessories) will require a further two or three cabinets and the input-output and control panel will be mounted on a separate operating desk. This machine is being designed and made under a contract from the National Research Development Corporation.

8. CONCLUSION

Since 1948 we have followed a policy of developing a range of packaged components for the logical and storage parts of computers. One large machine, using process-manufactured circuits, has been run for some time on a data-processing problem. Two machines are now being made using a later system of packaged circuits. A fourth machine has been commenced in which virtually all circuits will be packaged into standard form. We believe we are within measurable distance of being able to construct from circuits available 'on the shelf' a wide variety of types of computer, the step from logical design to complete machine being taken without further engineering development.

REFERENCES

(1) Digital Storage Using Ferromagnetic Materials. P.D. Atkinson, et alii. (Pittsburgh Meeting of the Association, May 1952).

(2) Standardised Printed Circuit Units for Digital Computers. D.L. Johnston (Ibid)

(3) Circuit Standardisation in Series Working, High-Speed Digital Computers. W.S. Elliott (Rutgers Meeting of the Association, March 1950 & Elliott Journal Vol. 1 No. 2)

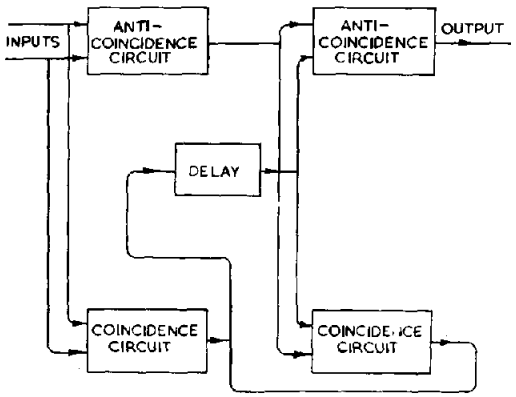

FIG.1 LOGICAL DIAGRAM OF EARLY ADDER

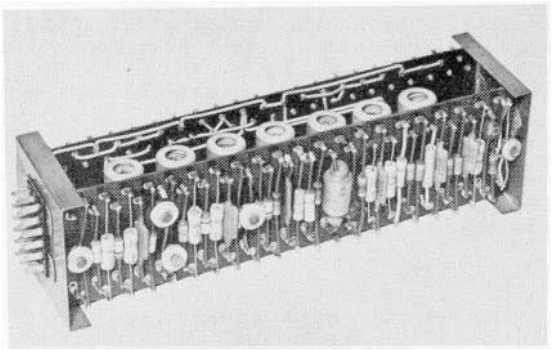

FIG. 2
EARLY ADDER CHASSIS FOR MULTIPLIER.

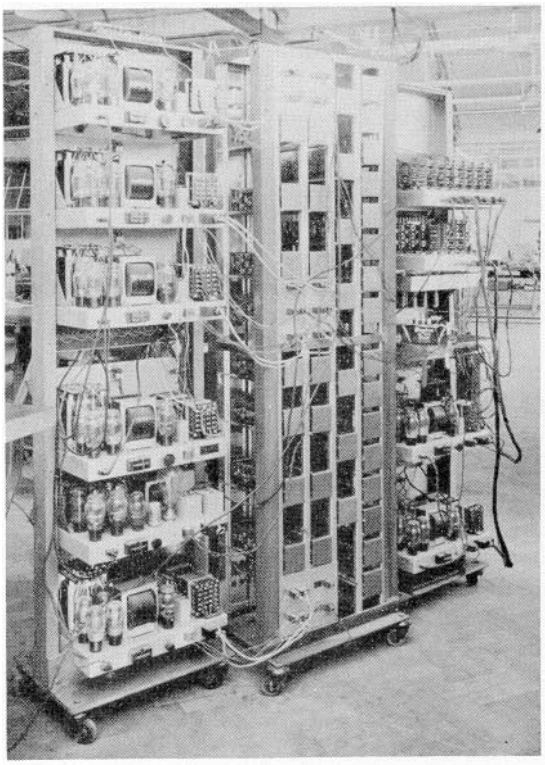

FIG. 3
EARLY MULTIPLIER.

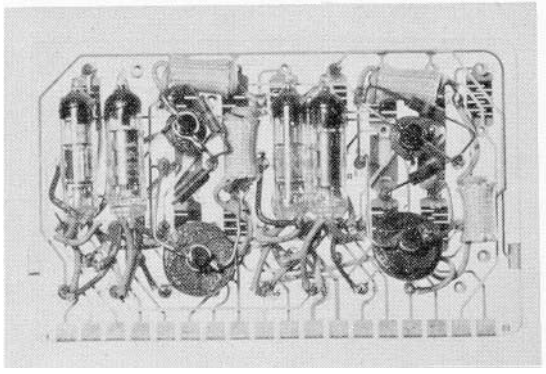

FIG. 4
5" x 3" PRINTED GLASS PLATE.
(Twin Delay)

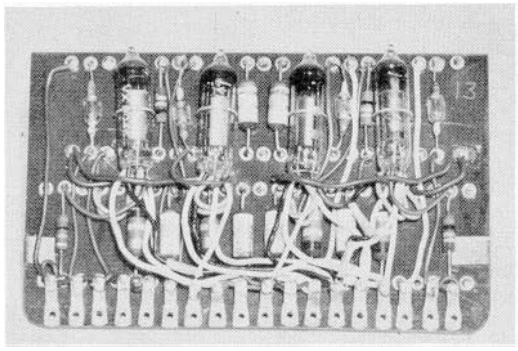

FIG. 5
5" x 3" WIRED PLATE.
(Twin Staticisor)

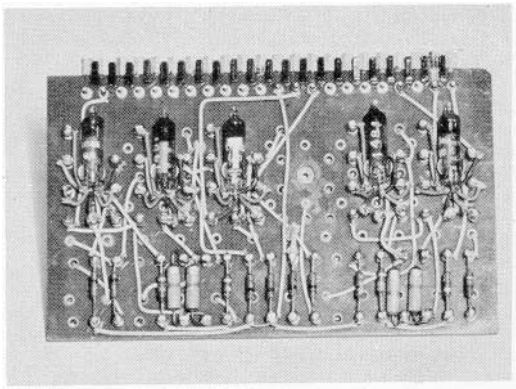

FIG. 6
$7\frac{1}{2}$" x $4\frac{1}{2}$" CONVENTIONALLY WIRED PLATE.
(Adder Logical Circuits)

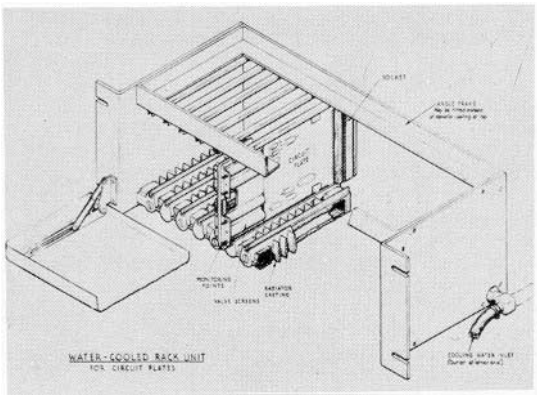

FIG. 7
NEW TYPE PRODUCTION PROCESS CIRCUIT PLATE
WITH SECTION OF WATER COOLED RACKING.

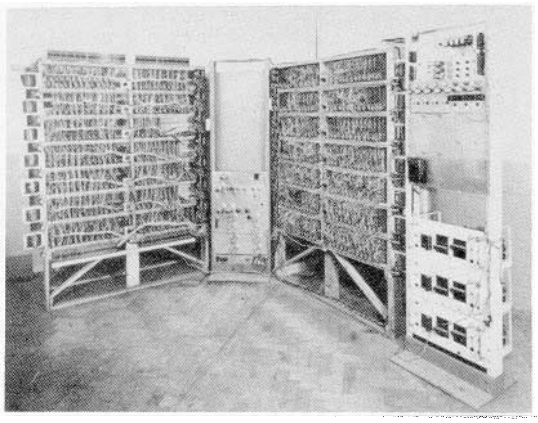

FIG. 8
"BREAD-BOARD" OF ARITHMETIC UNITS.
(Left-hand half not yet plugged up.)

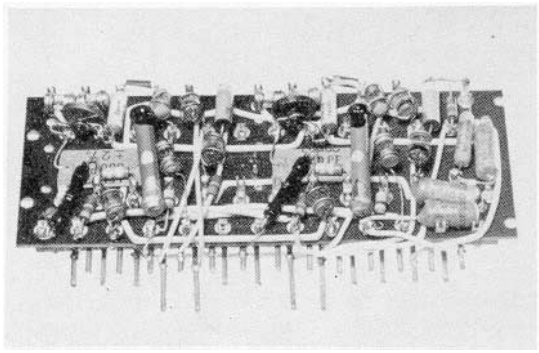

FIG. 10
PACKAGED UNIT WITH CONVENTIONAL WIRING AND PLUGS.

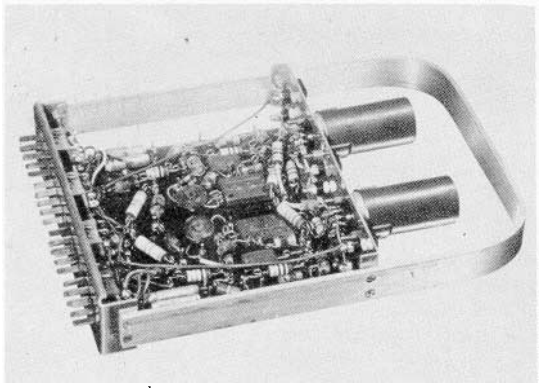

FIG. 9
"BREAD-BOARD" LOGICAL CIRCUIT UNIT.

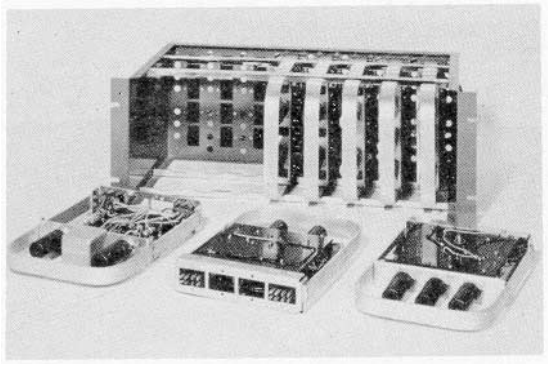

FIG. 11
GROUP OF PACKAGED UNITS IN SECTION OF RACKING.
(The components of a single word circulating nickel line have been unplugged)

OPERATING EFFICIENCIES AND CHARACTERISTICS OF THE COMPUTING MACHINES AT ABERDEEN PROVING GROUND

By

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The Computing Laboratory of the Ballistic Research Laboratories at Aberdeen Proving Ground has greatly expanded its computing facilities during the past year. The ORDVAC now has taken its place with the EDVAC, ENIAC, and the Bell Relay Computers.

The ORDVAC is a general purpose machine built by the University of Illinois for the Ballistic Research Laboratories. After reassembling at the Aberdeen Proving Ground during the latter part of February 1952, only five days of testing was required before satisfactory acceptance tests were completed. Since that time the ORDVAC has made a very commendable record. Additions have already been made to this machine in order to reduce the reading and printing time. A tape reader, approximately five times as fast as the original, and a punched card system for reading and printing have been installed.

Changes have been made in the EDVAC system since it was delivered to the Computing Laboratory by the University of Pennsylvania. Revision of the input-output system was discussed in a paper by R.L. Snyder, published in the A.I.E.E. Journal. Magnetic amplifiers were installed in the place of relays in order to control more precisely and reliably