FPGA Evening Panel

What is the Right Model for Programming and Using Modern FPGAs?

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Traditionally, FPGAs have been the bastard step-brother of ASICs. They have been forced to act like ASICs and fit themselves into the ASIC development model. This has meant ignoring their unique strengths: reprogrammability, late-binding and run-time reconfiguration. Today, however, FPGAs are becoming more acceptable for their own merits. The majority of new design starts are FPGA designs. As FPGAs rise from under the shadow of their aging brother, should they continue to try to wear his hand-me-downs? Or is it time to develop more suitable models that lets them shine? At the same time, the old ASIC model is not even serving ASICs well, and new models for developing ASICs are emerging. All of this may encourage us to rethink how we should be programming FPGA-based systems. Possibilities include:

- Using the traditional, ASIC model — it's tried and true, has demonstrated success
- Using the traditional, sequential processor model — Compile programs from C down to FPGAs...perhaps evolving FPGAs to better support
- Using the emerging C-level design tools
- Using concurrent and/or streaming models (incl. CSP, Matlab/simulink, Ptolemy, SCORE, Stream-C)
- Using a biologically inspired model (neural networks, genetic programming...)

This panel of FPGA and EDA experts will attempt to shed light on these possibilities, and explore, through an interactive debate, the merits and pitfalls of these different approaches.

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