A Noise Optimization Technique for Codesign of CMOS Radio-Frequency Low Noise Amplifiers and Low-Quality Spiral Inductors *

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ABSTRACT

Series resistance associated with inductor is usually ignored in noise optimization for CMOS low noise amplifiers (LNAs). With low-quality on-chip inductor the series resistance, however, degrades input matching and increases noise figure considerably. The LNA design is complicated by the fact that the series resistance varies with inductance in some specific pattern determined by physical implementation for on-chip inductor. This paper presents a novel noise optimization technique for the codesign of LNA and low-quality square spiral inductor. Theoretical derivation is given to model the tradeoff between thermal noise of series resistance and transistor channel noise for minimizing noise figure. A figure-of-merit (FOM) is proposed to characterize the relation between quality factor and effective inductance for square spiral inductor. The codesign of LNA and inductor is done by performing noise optimization for constant FOM. Design procedure is developed and validated by post-layout simulation in AMI 0.6um CMOS process with Cadence SpectreRF and Berkeley ASITIC tools.

Categories and Subject Descriptors

B.7.3 [**Integrated Circuits**]: Types and Design Styles – *standard cells, VLSI.*

General Terms

Design.

Keywords

CMOS, LNA, RF, inductance.

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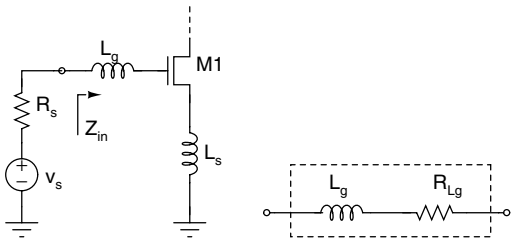
1. INTRODUCTION

The low noise amplifier (LNA) in CMOS is usually optimized for minimum noise since its noise figure dominates that of the receiver [8]. Meanwhile it is often infeasible to increase LNA power in exchange for lower noise figure because of the tight power budget of wireless communication headsets for which the LNA is typically designed [9]. To address this issue common-source LNA with inductive source degeneration has been widely used because of its potential to achieve best noise performance, and optimization techniques have been proposed to balance the tradeoff between gate-induced noise and channel noise of transistor for minimizing noise figure under power constraint [9, 4]. Integrated spiral inductor is widely used for LNA integration because of its advantages of low cost and ease of process integration [3]. Such inductor, however, exhibits very low quality factor (less than 10) and small effective inductance (less than 20 nH) at Giga-Hz frequencies [1]. Several predictive compact inductor models have been proposed to characterize inductor behavior at frequencies up to 10 GHz to good accuracy [3, 10].

The problem of codesign of LNA and spiral inductor has received little attention despite its importance. The series resistance of low-quality integrated inductor introduces significant thermal noise and degrades LNA input matching. Particularly, the noise optimization has to consider the fact that series resistance of inductor varies with inductance following specific pattern determined by physical implementation of inductor [1]. Failing to account for the characteristics of spiral inductor in LNA design will result in either considerable error in estimating noise figure and power, or values of inductance and quality factor (Q) that are impossible to realize for on-chip inductor in practice.

The noise optimization technique proposed in this paper addresses the codesign issue for the first time to the author's best knowledge. Mathematical derivation is given for modeling the effects of inductor resistance on LNA noise figure. The noise optimization is done by balancing the tradeoff between inductor thermal noise and transistor channel noise. A figure-of-merit (FOM) is proposed to characterize the relation between quality factor and effective inductance of spiral inductor, and is then used in noise optimization for the purpose of codesign. A design procedure based on proposed technique is developed for power-constrained LNA design. Three versions of 5-mW integrated LNA are designed in AMI 0.6-μm CMOS technology with various noise optimization techniques including the one proposed in this paper. The spiral inductor is designed with



(a) (b)

Figure 1: (a)A common-source LNA with inductive source degeneration; and (b) simple inductor model

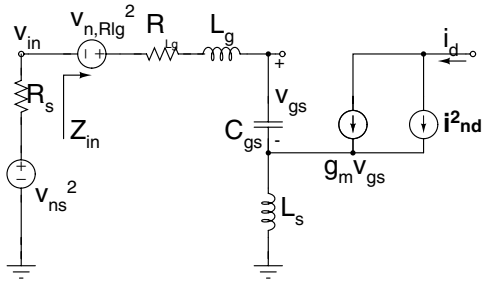


Figure 2: Small-signal equivalent circuit for LNA noise calculation

Berkeley ASITIC tool [7]. Finally a comparison of post-layout simulation results from Cadence SpectreRF tools is presented to validate the proposed work.

2. NOISE MODEL OF LNA

A source-degenerated common-source LNA is shown in Figure 1(a). Inductance L_s generates a real resistance at the gate of NMOS transistor M_1 for input matching. The gate-source capacitance of M_1 and parasitic capacitances at LNA input node are resonated out with inductance L_g. Values of L_s and L_g decrease as the working frequency ω_0 increases. For on-chip integration, both L_g and L_s are implemented with square spiral inductors for which a quality factor of 3.0 is common [1]. With the simple inductor model in Figure 1(b) for hand calculation, Q_L, quality factor of integrated inductor, is defined as

$$Q_L = \frac{\omega_0 L}{R_L}, \tag{1}$$

where L is the effective inductance, and R_L is the series resistance of inductor. For Q_L of 3.0, an 1-nH inductance introduces a 5-Ω series resistance at 2.4G Hz. Consequently the several-nH gate inductance L_g introduces a series resistance comparable to standard 50-Ω source impedance at M_1 gate. Meanwhile the series resistance due to L_s can be safely ignored in LNA noise calculation since L_s is much less than L_g.

Based on above analysis the small-signal equivalent circuit for LNA noise calculation is drawn in Figure 2. R_{Lg} is the series resistance associated with L_g. $v^2_{n,Rlg}$ is the thermal noise source caused by DC resistance (R_{Lg0}) of L_g. Though R_{Lg} becomes higher than R_{Lg0} as the frequency increases due to the skin effect and current crowding, the two resistances are close at low Giga-Hz frequencies that are of interest in this paper [3]. Therefore the power spectrum density (PSD) of the thermal noise is approximated as

$$v^2_{n,Rlg} \approx 4kTR_{Lg} = 4kT\frac{\omega_0 L_g}{Q_{Lg}}, \tag{2}$$

where k is the Boltzmann constant, T is the absolute temperature, and Q_{Lg} is quality factor of the gate inductor L_g. The thermal noise of M_1 is modeled as a current source with the PSD [8]

$$i^2_{nd} = 4kT\gamma g_m, \tag{3}$$

where g_m is the transconductance of M_1. γ is $\frac{2}{3}$ for long-channel transistors in active region, and even higher for short-channel transistors. In Figure 2 both induced gate noise and gate resistance noise of M_1 are omitted because the former is overwhelmed by the significant thermal noise of low-Q gate inductor L_g, while the latter can be minimized through careful layout [8]. Then the derived noise factor is

$$F = 1 + \frac{R_{Lg}}{R_s} + \frac{\gamma g_m}{G^2_m R_s}, \tag{4}$$

where G_m is the transconductance of LNA R-L-C network at resonance shown in Figure 2, and R_s is the source impedance. The calculation of G_m has been presented in the reference [9]. The noise contribution of low-Q gate inductor L_g is represented by the second term on the left of (4), and the third term characterizes the noise contribution of transistor M_1.

To reveal the implications of (4) under power constraint, the noise factor can be further developed by considering perfect input matching and transconductance g_m as a function of drain current I_d. In the case of perfect input matching at frequency ω_0, inductances L_g and L_s have to satisfy following relations

$$L_g + L_s = \frac{1}{\omega_0 C_{gs}}, \tag{5}$$

$$R_s = \frac{\omega_0 L_g}{Q_{Lg}} + \omega_T L_s. \tag{6}$$

This gives

$$L_s = \frac{R_s - \frac{1}{\omega_0 C_{gs} Q_{Lg}}}{\omega_T - \frac{\omega_0}{Q_{Lg}}}, \tag{7}$$

$$L_g = \frac{\frac{\omega_T}{\omega_0^2 C_{gs}} - R_s}{\omega_T - \frac{\omega_0}{Q_{Lg}}}. \tag{8}$$

Compared with g_m of long-channel transistor, g_m of short-channel transistor for specific power consumption is considerably reduced because of two important second-order effects : mobility degradation and velocity saturation. Mobility degradation is caused by the increasing vertical electric field in the channel, and can be modeled as [5]

$$\mu_{eff} = \frac{\mu_0}{1 + \theta_1 V_{od}} \tag{9}$$

where μ_0 is the mobility with zero vertical field, V_{od} is the gate overdrive, and θ_1 is inversely proportional to the oxide thickness. Similarly, the velocity saturation caused by the increasing horizontal field along the channel can be modeled as [5]

$$I_d = \frac{I_{d0}}{1 + \theta_2 V_{od}} \tag{10}$$

where I_{d0} is the drain current without considering velocity saturation, and θ_2 is inversely proportional to the effective channel length and the critical electric field value.

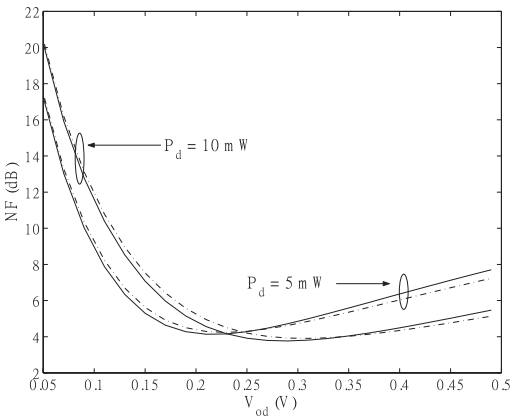


Figure 3: Noise figure versus gate overdrive for different power consumptions

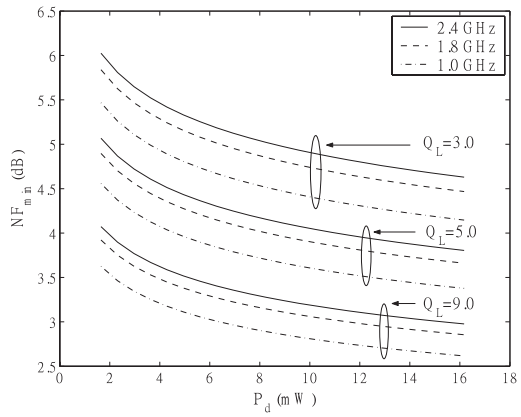


Figure 4: NF_{min} versus P_d for different Q-values and frequencies

For AMI 0.6-μm digital CMOS process θ_1 is less than 0.1 V^{-1} and θ_2 is around 0.31 V^{-1}. Then to the first order g_m is approximated by

$$g_m \approx \frac{2I_d}{V_{od}(1+\theta V_{od})}, \tag{11}$$

where

$$\theta \approx \theta_1 + \theta_2. \tag{12}$$

It can be shown that with (4), (7-8), and (11) the noise factor is given by

$$F \approx 1 + \frac{\omega_0}{R_s Q_{Lg}} \frac{V_{od}^2}{K_1(1+\theta V_{od})} + 4\gamma R_s \frac{K_1}{K_2} \frac{(1+\theta V_{od})^2}{V_{od}^3}, \tag{13}$$

where K_1 is proportional to power consumption, and K_2 is determined by characteristics of the CMOS technology in use. In practice, V_{od} is usually chosen around several hundred milli-volts for low power consumption [6] such that

$$\theta V_{od} \ll 1. \tag{14}$$

The noise figure is plotted as the function of gate overdrive for different power values as is represented by solid line in Figure 3. For small V_{od} value the drain noise of M_1 dominates LNA noise figure under power constraint because of the large device width used. As V_{od} value increases, the thermal noise of inductor tends to dominate LNA noise figure because of the larger L_g value. Consequently, there exists a minimum noise figure for specific power, and the minimum noise figure decreases as power increases. For the purpose of hand analysis, the term θV_{od} in (13) is assumed to have zero value. This results in an error less than 10 percent for V_{od} smaller than 0.5 V, as is illustrated by the dotted line in Figure 3. With the term θV_{od} being zero (13) can be solved to find the minimum noise factor for given power as well as the corresponding value of gate overdrive:

$$F_{min} = 1 + 3.41\gamma \frac{\omega_0^{0.6}}{K_1^{0.2} R_s^{0.2} K_2^{0.4} Q_L^{0.6}}, \tag{15}$$

$$V_{od,opt} = \left(\frac{6\gamma R_s^2 K_1^2 Q_{Lg}}{K_2 \omega_0}\right)^{0.2}. \tag{16}$$

3. EFFECTS OF LOW-Q INDUCTOR ON LNA NOISE FIGURE

It is seen from equations (7-8) that the use of low-Q inductor reduces L_s and increases L_g for given ω_0 and P_d. This is because the series resistance associated with L_g contributes to the input matching of LNA. Particularly, for given Q_{Lg} there exists an upper bound for L_g beyond which perfect input matching is impossible. The bound is given by

$$L_g \leq \frac{R_s Q_{Lg}}{\omega_0}. \tag{17}$$

For ω_0 of 2.4 GHz and Q_{Lg} of 3.0, the upper bound for L_g is around 10 nH. For required inductance exceeding the upper bound, external inductor has to be used.

The use of low-Q inductor substantially increases NF_{min}, the minimum noise figure calculated with (15) for given power, as shown in Figure 4. Particularly, to reduce NF_{min} it is much more effective by increasing inductor quality than by increasing power. For example, NF_{min} reduces by no more than 0.5 dB as P_d goes from 4 mW to 12 mW, meanwhile an 1-dB reduction is expected as Q_{Lg} increases from 3.0 to 5.0. It is also observed in Figure 4 that NF_{min} increases with ω_0 for constant Q_{Lg} and P_d.

The integration of inductor is restricted by the required inductance and allowed inductor quality. Generally it is more difficult to design spiral inductor of higher quality or larger inductance [1]. For specific Q_{Lg}, it is seen in Figure 5 that larger P_d results in smaller L_g and larger L_s. Therefore the integration of L_g becomes easier as power increases. However, in the power-constrained case of practical interest, higher Q_{Lg} results in larger L_g which is not desirable for on-chip integration. To solve this issue becomes the major driving force behind the the proposed codesign technique that shall be detailed in later sections.

4. FIGURE OF MERIT FOR SPIRAL INDUCTOR

The need for codesign of LNA and low-Q inductor becomes clear by examining Figure 6, in which the L_g required to maintain specific power and minimum noise figure is plotted as the function of Q_{Lg}. The figure shows that higher Q_{Lg} demands a larger L_g for constant power consumption to maintain minimum noise figure. And the trend becomes even stronger as the power consumption reduces. For practical spiral inductor in CMOS, however, the relation between Q_{Lg} and L_g exhibits a quite different pattern, as illustrated

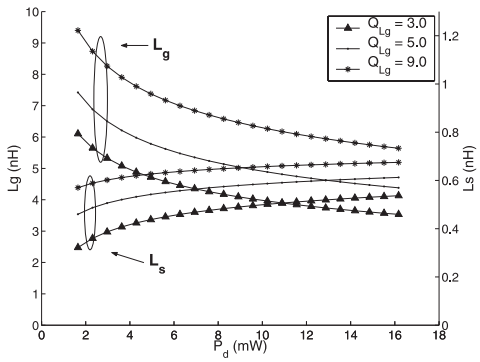


Figure 5: L_g **and** L_s **versus** P_d **for different** Q_{Lg}

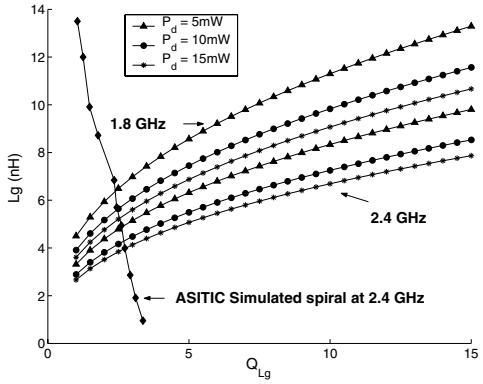


Figure 6: Lg **versus** Q_{Lg} **for different** P_d

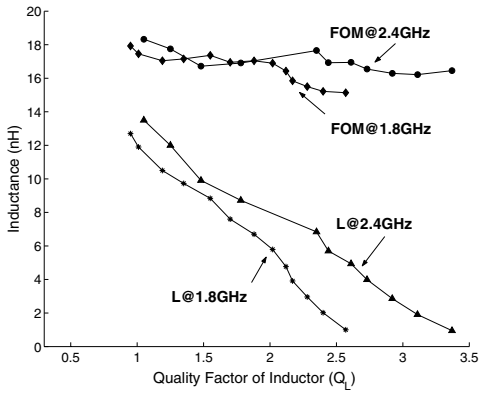


Figure 7: Simulated L **and** FOM **versus** Q_L **for different frequencies**

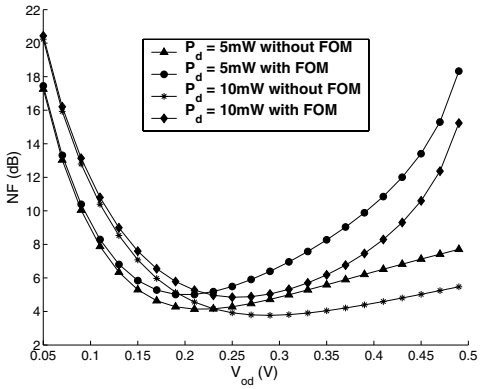


Figure 8: NF **versus** V_{od} **with and without** FOM

by the simulated curve in Figure 6. The simulation is performed with ASITIC [7] using AMI 0.6-μm CMOS process and the square inductor is implemented on metal-one layer. Consequently the L_g-Q_{Lg} pattern assumed by the "ideal" noise optimization process for LNA is no longer valid in the presence of low-quality inductor, and the codesign of LNA and inductor is needed to solve this problem.

The key to the codesign issue is to find a way that characterizes the Q_L-L (e.g. Q_{Lg}-L_g) relation for practical spiral inductor to good accuracy and is simultaneously suitable for design analysis of LNA. Previous analytical compact models for spiral inductor [3, 10] provide good accuracy yet are too complicated to be used in design analysis.

This paper employs a novel figure-of-merit (FOM) to model the Q_L-L behavior exhibited by spiral inductor

$$FOM = L + \zeta Q_L, \tag{18}$$

where ζ is a positive constant that can be determined by simulating L for two different Q_L values. For AMI 0.6-μm CMOS process, ζ is 4.6 nH for metal-one-layer square inductor simulated with ASITIC. The corresponding FOM is plotted in Figure 7 for different working frequencies. It is seen that the value of FOM remains constant despite the varying Q_L value and the varying frequency. Note that (18) can be proved employing the analytical inductor models presented in [10].

Therefore (13) is modified to give

$$F \approx 1 + \frac{\zeta \omega_0 V_{od}^2}{R_s(F_{om}K_1 - V_{od}^2)} + 4\gamma R_s \frac{K_1}{K_2}\frac{1}{V_{od}^3}, \tag{19}$$

It is seen in Figure 7 that the use of FOM increases NF_{min} by around 1 dB. However, the required V_{od} remains the same to maintain NF_{min} for given power consumption. This observation suggests that the bias condition for transistor can still be calculated with (16).

5. PROCEDURE FOR CODESIGN OF LNA AND SPIRAL INDUCTOR

Based on our analysis, a four-step procedure is developed for power-constrained codesign of LNA and spiral inductor.

1. Determine ζ and FOM. Q_L values are extracted using ASITIC for two different L values (for example, 1 nH and 10 nH). Then (18) is solved for ζ and FOM.

2. Determine device bias and geometry. With calculated ζ and FOM, curves similar to those in Figure 8 can plotted with (19).

	T1D	T1S	T2D	T2S	T3D	T3S
$W_{M1}(\mu m)$	353	353	405	405	435	435
L_g(nH)	8.17	8.01	6.57	6.49	6.2	6.01
Q_{Lg}	–	2.24	3.0	2.37	2.5	2.6
NF(dB)	3.3	7.1	3.9	6.1	4.4	5.4
$S11$(dB)	-17	-10	-34	-18	-32	-20
$S21$(dB)	21	15	20	18	19	18

Table 1: Design and simulation results for 5-mW LNA with different noise optimization techniques

Then NF_{min} as well as the corresponding V_{od} can be figured out by examining the curves. The device geometry is calculated from power and V_{od} using transistor I-V equations considering velocity saturation and mobility degradation [5].

3. Determine L_g and Q_{Lg}. C_{gs} is calculated using the device geometry, then it is straightforward to derive the values of L_g and Q_{Lg} by solving (5), (6), and (18).

6. SIMULATION RESULTS

To verify the proposed design concepts and procedure, three versions of integrated LNA are designed using different techniques for noise optimization. The first version uses the classic technique presented in [9]. The quality factor for R-L-C network of LNA input stage is 5, which predicts a noise figure of 3.3 dB for 5-mW power consumption. Note that the effects of low-quality inductor are not considered *in* the optimization process [9]. The second version uses the results in (15) and (16) while assuming a constant Q_{Lg} of 3.0. The third version is designed with the proposed codesign procedure for noise optimization. ζ and FOM are found to be 4.6 and 18 nH, respectively.

The designed LNAs are laid out and the parasitic parameters are extracted, both with Cadence Virtuoso tools. The post-layout simulation is performed with Cadence SpectreRF tools. The square spiral inductors are designed to have outer dimension less than 200 μm, and are optimized for maximum quality on metal-one layer in AMI 0.6-μm CMOS technology with ASITIC tool. The design values for LNA and inductor parameters are shown in those columns marked by "T*D" in Table 1, and post-layout simulation results are shown the columns marked by "T*S"in the same table.

The first version of LNA has the highest NF as well as the largest error in NF estimation (3.3 dB designed, 7.1 dB simulated), because series resistance of 8-nH L_g is not considered in noise optimization, which accounts for a 2.5-dB increase in simulated NF. The second version improves LNA noise performance by considering the low-Q effects due to spiral inductor. This not only reduces the simulated NF, but also reduces the error in NF estimation (3.9 dB designed, 6.1 dB simulated). However, simulated NF still differs from designed NF by a considerable margin of 2.2 dB. This is because the assumed constant Q_{Lg} of 3.0 can not be achieved in practice for 6.5-nH square inductor. The third version further considers specific Q_{Lg}-L_g pattern, and therefore achieves the lowest NF and the smallest design error (4.4 dB designed, 5.4 dB simulated) despite the use of a lower Q_{Lg} of 2.5.

7. CONCLUSION

The importance of codesign of LNA and low-quality spiral inductor has been demonstrated for minimizing LNA noise figure. A novel figure-of-merit for spiral inductor as well as a novel noise optimization technique has been presented. Three versions of LNA have been designed and laid-out using different noise optimization techniques. Post-layout simulation results show that the proposed technique effectively reduces LNA noise figure as well as design complexity. Compared with conventional techniques for noise optimization, the proposed technique results in wider transistor width and smaller gate inductance. Consequently, higher quality factor can be designed for spiral inductor to reduce its noise contribution. The LNA designed with the proposed technique has been submitted to MOSIS for fabrication.

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