Designing Robust Microarchitectures

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ABSTRACT

A fault-tolerant approach to microprocessor design, developed at the University of Michigan, is presented. Our approach is based on the use of *in-situ* checker components that validate the functional and electrical characteristics of complex microprocessor designs. Two design techniques are highlighted: a low-cost double-sampling latch design capable of eliminating power-hungry voltage margins, and a formally verifiable checker co-processor that validates all computation produced by a complex microprocessor core. By adopting a "better than worst-case" approach to system design, it is possible to address reliability and uncertainty concerns that arise during design, manufacturing and system operation.

Categories and Subject Descriptors

B.8.1 [**Performance and Reliability**]: reliability, testing and fault-tolerance.

General Terms

Computer System Design, Microarchitecture, Reliability.

Keywords

Low-power, system-on-a-chip, reliable microarchitecture design.

1. INTRODUCTION

An old adage says, "If you're not failing some of the time, you're not trying hard enough." To address the reliability and power challenges that current on-chip densities pose, we have adapted this precept to system design. We present two new design techniques, based on a "better than worst-case" design approach, that optimize most components for common case operation (i.e., typical energy, fabrication variance, or correctness), while ensuring a robust system through the introduction of error detection and correction mechanisms. With this approach, most designers are concerned primarily with performance, while comparatively fewer designers are shouldered with the responsibility of implementing correct error recovery components. Two error detection and correction mechanisms are presented: a low-cost timing error detector for low power design, and a functional checker capable to correcting design errors in complex systems on the fly.

Razor, a voltage-scaling technology based on dynamic detection and correction of circuit timing errors, permits design optimizations that tune the energy in a microprocessor pipeline to typical circuit operational levels [1]. This approach to system energy management eliminates the voltage margins that traditional worst-case design methodologies require and allows digital systems to run correctly and robustly at the edge of minimum power consumption. Occasional heavyweight computations may fail and require additional time and energy for recovery, but the overall computation in the optimized pipeline requires significantly less energy than traditional designs. Razor supports timing speculation through a combination of architectural and circuit techniques, which we have implemented in a prototype Razor pipeline. Results of the Razor prototype and simulation studies will be highlighted.

DIVA, an on-line checker component inserted into the retirement stage of a microprocessor pipeline, fully validates all computation, communication, and control exercised in a complex microprocessor core [2]. The approach unifies all forms of permanent and transient faults, making it capable of correcting design faults, transient errors (like those caused by natural radiation sources), and untestable silicon defects. We will highlight studies demonstrating that DIVA checkers preserve system performance while keeping area overheads and power demands low. Furthermore, checkers can be implemented with simple state machines that can be formally verified and effectively scaled for higher-performance designs. A physical design of a checker processor for the Alpha instruction set will be described.

2. ACKNOWLEDGMENTS

This work is supported by grants from ARM Ltd., the National Science Foundation, and the Gigascale Systems Research Center.

3. REFERENCES

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DAC2004, June 7–11, 2004, San Diego, CA, USA.