Phase Correct Routing For Alternating Phase Shift Masks

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ABSTRACT
In this paper, we investigate routing restrictions that enable the generation of "correct by construction" layouts for Dark Field AltPSM. Existing routers produce designs in which coloring errors are numerous, and up to 15% of the pin locations in macros may cause unavoidable coloring errors. We identify routing restrictions which produce 100% phase-correct results, and quantify the impact on wire-lengths and via counts.

Categories and Subject Descriptors
B.7.2 [**Design Aids**]: Layout.

General Terms
Algorithms, Design, Experimentation.

Keywords
Resolution Enhancement Techniques (RET), Lithography, Routing, Layout.

1 Introduction
With each new technology node, the use of Resolution Enhancement Technology (RET) has become more aggressive. Designers are being exposed to new RET related layout restrictions [5,7]. One of these RET related restrictions has been the introduction of Alternating Phase Shift Masks. This paper presents a Phase Correct Router for Bright Field and Dark Field Alternating Aperture Phase Shift Masks (AltPSM), with a concentration on the Dark Field wiring problem.

The definition of Bright Field AltPSM (Alternating Aperture AltPSM for Polysilicon layers) is relatively settled. The exact details of Dark Field AltPSM usage in metal wiring layers are still unsettled and the exact implementation details may differ somewhat. However the concept remains that Dark Field AltPSM imposes graph colorability constraints on the metal wiring layers of a chip layout. These layers have commonly been designed using automated wiring programs, making it important to understand the implications of graph colorability constraints on wiring algorithms and layout methodologies. Work has been done in the area of defining methods for producing phase-correct results for custom layout, primarily with respect to transistors, in the context of Bright Field [6]. In [8], it was observed in a footnote that ground rule restrictions may suffice in dealing with some RET details. Our research defines a set of wiring and pin layout restrictions for routers in Bright Field and Dark Field, with a concentration on the Dark Field wiring problem. We quantify the number of Dark Field coloring errors which are created when layouts are completed by routers which do not understand Dark Field colorability. We show that traditional routers produce results which are far from phase correct, and that introducing routing restrictions does not significantly impede the wirability of layouts.

DAC 2004, June 7-11, 2004, San Diego, California, USA

2 Alternating Phase Shift Masks
AltPSM is a form of strong RET which has been discussed extensively in the literature [1,3,4]. AltPSM will be widely used for the polysilicon layer at the 65 nm node, and may become important for metalization at future technology nodes [9]. There are numerous styles of AltPSM. We will be dealing with ***Bright*** Field and ***Dark*** Field Alternating Aperture PSM. We use the definitions of Bright and Dark field which are presented in [12].

In Bright Field AltPSM, a critical feature is a design shape, known as a critical wire. Each critical feature is flanked by two phase shapes, which must be assigned opposing phases in order to create destructive interference between them. In Dark Field AltPSM, the critical feature is the minimum size space between two design shapes. Alternating phases are assigned to the design shapes. The destructive interference between the light passing through the design shapes creates (or defines) the space between them [12]. Each unioned design shape must have the same phase for its entire extent.

Both Bright and Dark Field require that the phase shapes be ***colored*** in a way which guarantees that all critical features are flanked by opposing phases that alternate across each critical features. This coloring problem creates topological constraints. There are shape topologies which cannot be colored, meaning that the alternating phase requirement cannot be met.

2.1 Bright Field Mask Phase Conflicts
Bright Field conflicts are caused by design shapes, or groups of shapes, which induce phase shapes that cannot be 2-colored. There are several typical types of Bright Field phase conflicts and methods for breaking those conflicts [3,4]:

- The "T" conflict, caused by a "T" shaped critical wire.

- The “Odd-Even” conflict, where an odd number of critical wires at minimum spacing become an even number of critical wires while maintaining minimum spacing, through a line-end and a jog.
- The “Line-End” conflict, where two orthogonal critical wires are placed closely enough to cause a phase conflict.

2.2 Dark Field Mask Phase Conflicts

Dark field conflicts occur when the unioned design shapes which are within the critical distance of each other cannot be 2-colored. The space between these shapes is the critical region, known as a critical space [12].

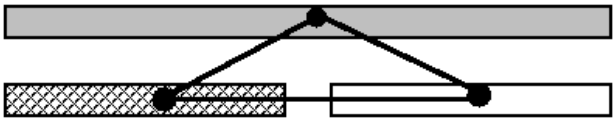

Figure 1

In Figure 1, we see a Dark Field phase conflict which is caused by two wires ending too closely together, while a third wire passes the gap at minimum spacing. In this case, there is a “T” shaped space created, with the base of the “T” being the gap between the wires.

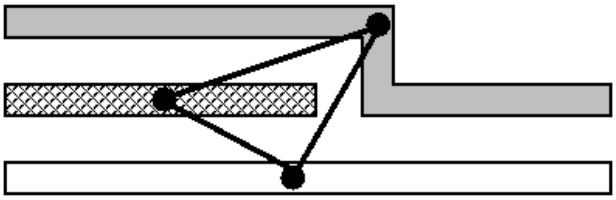

Figure 2

Figure 2 shows the Dark Field equivalent of an “Odd-Even” run. In this case, the phase conflict is caused by the requirement that the top wire (the wire which bends) must carry the same phase for its entire length. This creates the 3-cycle shown, since the top wire cannot have an alternating phase from both the middle wire and the bottom wire, if the middle wire and bottom wire also have differing phases.

3 Phase Correct Routing

Our research investigates the feasibility of performing Phase Correct Routing. We demonstrate that it is possible, using a set of layout restrictions, to route wires such that the results can always be phase shifted. We demonstrate this for Bright Field and Dark Field phase shift masks. We then quantify the impacts of these restrictions on the quality of the layouts.

The routing restrictions that we propose are all local in nature, yet they lead to a globally colorable solution. These restrictions have the effect of making the routing more “conservative” in nature, in that potential phase conflicts are avoided. This lowers the routing density slightly, due to the fact that certain routing topologies are forbidden.

In the following, we primarily concentrate on the Dark Field routing problem. Bright Field phase shift masks are primarily used in the gate layers of designs. Automated routing is performed in that context, but in many cases these layers are laid out by hand or by using parameterized cell generators.

3.1 Bright Field Routing Restrictions

For Bright Field routing, we require two restrictions:

1. All wires in the primary wiring direction must be on a uniform wiring pitch and may be critical or non-critical. This allows phase shapes to be laid out in parallel stripes.
2. All wires running orthogonal to the primary wiring direction (also known as "wrong-way") must be non-critical. This prevents “T”, “Odd-Even”, and “Line-End” conflicts, by preventing phase relationships from following wrong-way wires.

These restrictions are similar to design restrictions which have been proposed in order to create correct by construction gate layouts [10] and for technology migration [3].

3.2 Dark Field Routing Restrictions

For Dark Field routing, we require the following three wiring restrictions:

1. All wiring must run in the primary wiring direction, with a uniform spacing or pitch. Wires running orthogonal to the primary wiring direction are forbidden.
2. Any location where a wire ends must have an extra space inserted beyond the wire end, effectively doubling the free space between the end of one wire and the end of the next wire.
3. Pins cannot be aligned in the primary wiring direction (for the pin layer), at minimum spacing. Two such pins create a minimum width spacing, violating restriction 2.

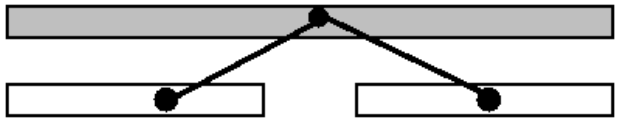

Figure 3 – “T” Conflict Corrected

On a Dark Field mask, a “T” conflict is caused by a minimum width gap between two wire ends, where there is a third wire running continuously in either of the tracks adjacent to the gap. In Figure 3, we show how restriction 2 prevents a “T” shaped gap (as shown in Figure 1) by widening the distance between two line ends, thereby making the space between the line ends non-critical.

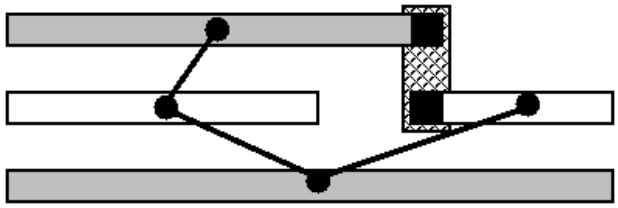

Figure 4 - "Odd/Even" Conflict Corrected

Correcting or preventing an Odd-Even run in a Dark Field mask is achieved by prohibiting any wrong-way wires [1]. By preventing any wrong way wires, we prevent a critical edge from ever occupying more than one phase stripe. In the example shown in Figure 4, we break the phase conflict shown in Figure 2 by moving the wiring jog to a separate wiring layer which runs orthogonal to the primary wiring direction of the non-jogged portions of the wire.

There is an additional complication for Dark Field masks, pin access. If we have two or more pins on minimum pitch, aligned in the primary routing direction, they may not be accessible. Whether the pins can be routed or they create an intrinsic phase conflict will depend upon the details of how Dark Field masks are implemented. In the worst case via arrays may not be possible depending upon whether the via layer is phase shifted. Two pins aligned in the primary routing direction would require wires which terminate at the pins, leaving a minimum size space. This wire configuration violates restriction number 2.

3.3 Correctness

In both the Bright and Dark Field implementations, we create a layout in which the phase shapes are generated in stripes running parallel to the primary wiring direction. The phases in each of these stripes are consistent across the wiring region. We prevent any topologies which cause the phase in a stripe to change, such as a critical edge which jogs. Another way of saying this is that ***all*** critical features are designed parallel and on a uniform pitch or periodicity.

3.4 Implementation

The implementation of these algorithms was prototyped in C++ within an existing interactive layout system. The base algorithm used is a gridded multlayer router using best first search [11]. The major difference between the base algorithm and the phase correct algorithm lies in choosing which moves can be explored. The restrictions noted earlier are implemented as limitations in the search phase of the algorithm. During the retrace stage, the blockages on extra grids are inserted. For a Bright Field wire which is routed perpendicular to the preferred direction, a double width wire is inserted and two side-by-side grid points are blocked at each point along the wires length. For a Dark Field wire, a blocked grid point is placed on the grid which lies one beyond each end of a wire, in the preferred routing direction.

3.5 Test Cases

Two groups of testcases are used. The first set of testcases are classic routing examples taken from the literature [2], S1-5. The switchboxes are all routed using two levels of wiring. These testcases required some modification, in that some placed pins on one routing layer on all four sides of the switchbox. This pin arrangement violates Dark Field wiring restriction 3. The pins in these test cases were assigned to the layer which is wirable in the direction the pins are aligned. The second set of test cases, P1-8 are macros taken from two completed microprocessor designs. P1 through P4 are routed on two levels, P5 through P8 are routed on three levels.

[1] An "Odd-Even" run does not necessarily create a phase error if the jog spans an even number of wiring channels and Dark Field restriction 2 is respected along the wrong-way section.

4 Phase Assignment and Checking

Bright Field phase coloring tools are available, and verifying the colorability of the Bright Field layouts is now relatively straightforward. Methods such as those in [1] can be applied to Dark Field layouts as well. The obvious difference between Bright Field and Dark Field is that the Dark Field phase coloring program does not need to create phase shapes. Each unioned wire in the layout, which has a minimum spacing to another wire, must be assigned a color. A wire's color must be different from the color of every other wire at minimum spacing. If the layout is assumed to be Dark Field correct, the layout can be checked for correctness by verifying compliance with the routing restrictions from Section 3.2. The coloring can then be applied in rows (for a horizontal layer, columns for a vertical layer), and be known to be conflict free.

4.1 Performance of Existing Routers

The test cases that were taken from completed chip designs were run through both of the Dark Field checking methods in order to determine "how close" their existing routings are to being phase correct. In Table 1, the phase routing errors for the pre-existing routing is broken out into three types of errors. The first type of errors are odd-cycles in the phase conflict graph. The second type of errors are violations of the routing restrictions defined in section 3.2. The third error class is Illegal Pins. These are pins which violate restriction 3 in section 3.2. Illegal pins represent unavoidable violations of the phase correct routing restrictions. Illegal pins, in some cases, indicate a methodology issue that needs to be addressed in the definition of how the elements of the hierarchy interact.

Table 1: Phase Coloring Violations from Traditional Router

Average Violations	P1-3	P4	P5-8
M1 Odd Cycles	245.3	786	6.0
M1 Routing Restriction Violations	749.7	4008	9.0
M2 Odd Cycles	107.3	0	22.5
M2 Routing Restriction Violations	157	13	42.0
M3 Odd Cycles	n/a	n/a	0.75
M3 Routing Restriction Violations	n/a	n/a	2.5
Illegal Pins	121.3	1450	46.5

Test case P4 is interesting in that it represents a bitstack type topology, where there is a great deal of regularity to the routing. Much of P4 may have been wired by hand. Any error which occurs once in P4 occurs many times, with some regularity. In P4, many of the pins (nearly 15%) are illegally located, and there are 2495 shapes which contain wrong-way wiring.

5 Routing Results

The results of the wiring show very interesting trends with respect to the classic switchboxes. The success rate with routing restrictions is relatively low. This appears to be due to the fact that the switchboxes are very densely filled, and the blocked but

unused grid points required by Dark Field restriction 2 leave little room for the final wires to complete routing. In [2], the provided solutions leave as little as 4% of the grid points on a layer available, with an average of around 17%. In the phase correct routing, each wire segment within the switchbox blocks its own length, plus two additional grid points. None of the switchboxes has an extent of more than 23 wiring tracks, meaning that a wire which runs in a track will block approximately 10% of that track with unused and blocked grid points, over and above the actual extent of the wire. When these additional grid point blockages are not inserted, test cases S2, S3, and S5 achieve better routing results.

Overall, the phase correct router performs very well, leaving few incomplete routes.

Table 2: Routing Results for Phase Correct Routing

Name	Nets	Pins	Wiring Levels	Unrouted Nets	Unrouted Pins
S1	6	19	2	1	2
S2	10	24	2	6	10
S3	10	30	2	3	7
S4	22	57	2	5	10
S5	25	66	2	6	14
P1	1956	5103	2	8	12
P2	1987	5227	2	9	12
P3	234	972	2	6	8
P4	2892	9811	2	28	40
P5	526	1301	3	0	0
P6	389	908	3	0	0
P7	147	351	3	0	0
P8	130	377	3	0	0

6 Design Impact

It is reasonable to expect that these routing restrictions will cause an increase in via counts, due to the inability to insert jogs without changing wiring layer. It is possible that the wiring lengths will also be impacted. In order to quantify the impact, the router was run on each design using non-phase correct rules, with jogs discouraged, but allowed. This allows a direct comparison between the results with and without routing restrictions. The number of vias increased by an average of 16.5%, while net lengths decreased by 5.5%. Larger via count increases were seen in the 2-level wiring cases, smaller increases in the 3-level wiring cases.

In [10], an argument is made for "Radical Design Restrictions", in order to minimize the risks associated with strong RET implementations. One way of looking at this tradeoff is to consider aggressive design versus conservative design. The conservative layout restrictions identified here guarantee a phase-correct routing solution. These restrictions are not absolutely necessary in order to produce a phase-correct layout. An aggressive design, which makes tradeoffs in favor of higher density by not using layout restrictions, will likely require iteration post-layout to resolve phase conflicts.

7 Acknowledgements

The author would like to thank Prof Sartaj Sahni for his guidance, and Lars Liebmann, Fook-Luen Heng, Gustavo Tellez, and John Cohn for sharing their insights and for many helpful discussions.

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