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An Ultra-Low Power Charge Redistribution Successive Approximation Register A/D Converter for Biomedical Applications

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Abstract

Power consumption is one of the key design constraints in biomedical devices such as pacemakers that are powered by small non rechargeable batteries over their entire life time. In these systems, Analog to Digital Convertors (ADCs) are used as interface between analog world and digital domain and play a key role. In this paper we present the design of an 8-bit Charge Redistribution Successive Approximation Register (CR-SAR) analog to digital converter in standard TSMC 0.18μm CMOS technology for low power and low data rate devices such as pacemakers. The 8-bit optimized CR-SAR ADC achieves low power of less than 250nW with conversion rate of 1KB/s. This ADC achieves integral nonlinearity (INL) and differential nonlinearity (DNL) less than 0.22 least significant bit (LSB) and less than 0.04 LSB respectively as compared to the standard requirement for the INL and DNL errors to be less than 0.5 LSB. The designed ADC operates at 1V supply voltage converting input ranging from 0V to 250mV.

Keywords

Low Power; Charge redistribution; Successive Approximation; ADC; Comparator; INL; DNL

1. INTRODUCTION

Analog to Digital Converters (ADC) are one of the main functional blocks in many applications such as biosensors and biomedical devices that operate on a non-rechargeable battery. One such example is a pacemaker that is powered by a small sized battery over its entire operating lifetime. Therefore, power consumption and the battery lifetime determines the usability and cost of these implantable devices and hence designing a very low power consuming circuit is of high importance and main design criteria for these devices.

The bioelectric analog signals such as electrocardiogram (ECG), electromyogram (EMG), electrooculogram (EOG), and electroencephalogram (EEG) vary slowly with amplitude ranging from 10 μV to 100 mV. These analog signals are converted to digital code using ADCs for further processing of data in a digital processing unit. To reduce the power

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consumed by the ADC in these sensors, SAR-ADCs are widely used [1–13, 22–27]. In Ref [1–4] SAR ADC uses a separate digital to analog converter (DAC) and sample and hold (S/H) circuit which makes the entire input capacitance independent of DAC capacitor array. The disadvantage of this configuration is that it consumes higher power due to additional S/H circuit. Ref [5–6] describe the time-interleaved SAR ADC which can operate at high speed with considerable power consumption but these SAR ADC suffer from channel matching, time matching and occupy large area. To overcome these disadvantages, Ref [7–13] describe the design of capacitive DAC with an inherent S/H circuit which uses only one binary weighted capacitor array, one comparator and digital circuit for low power operation. Making use of the advantages of the capacitive DAC with inherent S/H circuit, it's simple architecture and most of the circuit being scalable with technology, in this paper we present the design of a CR-SAR ADC to reduce the power consumption. Except for the comparator, the designed circuit is all digital. Comparator in the ADC consumes more power compared to other blocks and hence the circuit is operated with low sampling rate, low power supply voltage and uses smaller channel length transistors.

The rest of this paper has been organized as follows. Section 2 describes the CR-SAR ADC architecture. Section 3 describes the design of each module in the ADC and Section 4 elaborates on the ADC simulation results and its performance. Finally, conclusions are presented in section 5.

2. ARCHITECTURE

The ADC circuit design presented in this paper uses a charge redistribution successive approximation architecture which is widely used in most biosensors and biomedical system on chip applications where signals are extremely weak and usually changes very slowly. Hence the speed characteristic of the circuit is of minimum importance but the designed ADC should have a low power consumption, and must occupy small die area [15].

The designed SAR ADC architecture consists of a binary weighted capacitor array which forms a DAC where it is compared with the input sampled analog signal through a comparator. Also, the whole process is managed through shift register and switch array that is needed for the SAR-ADC. This architecture provides low power consumption because it only requires one comparator, no separate S/H circuitry, and it uses low frequency CMOS digital logic unit [18]. Figure.1 shows the complete block diagram of this design that includes a comparator, switch array module, binary weighted capacitor array, SAR logic and control units. The SAR logic and control unit consists of customized delay flip flop and basic gates.

There are four main phases during the conversion cycle [15]:

1. Sampling the analog data onto the bottom plate of the capacitors as V_{in}, while the top plate is grounded.
2. The charge is then held as the bottom plates of each capacitor becomes grounded, forcing the top plate to reach negative V_{in}.

3. In the approximation stage, the digital SAR logic controls the switching starting from the most significant bit (MSB) and the comparator compares whether the voltage is positive or negative at the top plate of the binary weighted capacitor array. If the voltage on the top plate is positive then the approximation was too high, so this bit is considered to be a 0 and the top plate is returned to its negative value as before. If the voltage stays negative, then this bit is considered to be a 1 and the new negative voltage on the top plate is retained. This is repeated for each bit, thus the conversion phase will take n-clock cycles, where n is the number of ADC output bits.

4. After the least-significant bit (LSB) is reached, the digital data is valid and a new conversion cycle begins. The full conversion should take approximately n+2 clock cycles, one for sampling (Start) the analog signal, n for approximating (D_7-D_0), and one for outputting the digital data (Ready).

Table I, shows the order of extracting digital bits during each sequential cycles and their availability. The first cycle is for sampling phase and next N cycle is for extracting digital bits during the hold period. Finally, in the last cycle, all digital bits are ready for transfer to the next stage's buffer. Also, the MSB bit is evaluated first and LSB bit is evaluated at the end.

3. DESIGN OF CR-SAR ADC

The low number of transistors used in this design is one of the key factors in reducing the power consumption and the silicon area. Other factors in reducing the power consumption of the ADC circuit design are the use of low power supply voltage (1V), clock gating, and the moderate resolution of 8-bits. The following sections gives the detail of the sub-modules used in the ultra-low power ADC design.

3.1 The Comparator

Figure.2 shows the design of a high speed CMOS comparator [17]. This comparator consists of a differential input pair at input stage, a CMOS latch circuit as flip-flop stage, and an S-R latch. The CMOS latch is composed of an n-channel flip-flop with a pair of n-channel transfer gates for strobing and an n-channel switch for resetting, and a p-channel flip-flop with a pair of p-channel precharge transistors. $\phi 1$ and $\phi 2$ are the two non-overlapping clocks ($\phi 2$ is inversion of $\phi 1$). The dynamic operation of this circuit is divided into reset time interval and regeneration time interval. Comparison occurs at positive edge of $\phi 1$ due to the regeneration phase happening when $\phi 1$ is high and the reset phase happens when $\phi 2$ is high.

This comparator is designed for high speed sampling rate due to its high sensitivity and low propagation delay. Though it is used for high speed applications, it still supports the comparison of very low voltage differences at low supply voltage while generating a stable output with minimum delay. Also, it is possible to reduce total used current by increasing the channel length of transistors in the SR-Latch. A 1V supply voltage is used in our design even though standard recommended supply voltage for 180nm technology node is 1.8V and hence could help reduce the overall power consumption.

The current source used in the comparator provides 75nA. The size of the transistors used in our design are listed in Table II. According to the design specification, the implemented comparator should have sensitivity less than 0.97 mV because the V_{LSB} = 250mV/256 = 0.9765625 mV. This was verified using simulations. The simulation results show that the sensitivity of the comparator implemented using appropriately sized transistors to be less than 0.95mV.

3.2 The Digital to Analog Converter

The design of the DAC is based on charge scaling method which is the combination of a binary weighted capacitor (BWC) array and switch array module. The equivalent analog output V_{out} of DAC is given by:

$$V_{out}=V_{ref}.\frac{1}{2^N}\sum_{i=0}^{N-1} b_i.2^i \quad (1)$$

Where V_{ref} is full scale input voltage equal to 250mV, N is 8 bits, b_i is the binary value either 0 or 1 which is evaluated by the comparator output.

From Figure 1 the BWC array uses a terminating capacitor ($C_{¢}$) of size equal to 900fF and hence the C_0 is 900fF, C_1 is 1.8pF, C_2 is 3.6pF and so on for C_7 it is 115.2pF.

Switch Array Module has three different operating conditions in which it either connects each of the BWC array to V_{in}, V_{ref}, or to GND by multiplexing the capacitor connection pin between the three different voltage levels. Figure 3 shows the schematic of switch array module which includes D_0 to D_7 as input bits. In hold mode, each Di bit makes decision about its corresponding capacitor Ci connection either to V_{ref} or GND. If Di=1 then capacitor will be connected to V_{ref} else, it will be connected to GND. In the sampling mode capacitors are charged to V_{in}. S_0 to S_7 and $S_{¢}$ are the outputs of the switch array module that are connected to their corresponding capacitors. Totally ten 2:1 MUXs and eight NOR gates are used in this switch array module. Table III shows the functionality of the switch array module for the sampling/hold input circuitry.

3.3 The Successive Approximation Register

Figure 4 shows the schematic diagram of the SAR logic unit. D_0 to D_7 are the valid digital output bits when the ready signal is active. B_0 to B_7 are inputs from control unit which are active from the second cycle to the ninth cycle where only one line is high at a time and rest of them in the low state. During 1st cycle, the analog input signal is sampled and B_0-B_7 is reset. During 10th cycle, ADC output digital code is available for transferring to the next stage and B_0-B_7 is again set low.

The ReStart signal is an asynchronous input signal that resets all DFF outputs. The Compare_Bit is input to the SAR logic unit which is the output from the comparator module. The value of the Compare_Bit will be stored on to the DFF on negative edge of clk_Q2. The clk_Q1 is for synchronizing SAR logic unit with control unit. Table IV shows the Function Table of the customized DFF. The frequency of clk_Q1 and clk_Q2 are same

with different phase. There are 8 customized DFF as required by the ADC resolution of 8 bits.

3.4 The Control Unit

The control unit is implemented using a shift register as shown in Figure 5 with 10 DFF registers. There are 9 resettable DFF while the first DFF is settable because this DFF has to be set whenever ReStart input signal is active and rest of the 9 DFF should be cleared. All the units are connected as shown in Figure 1. The output voltage of BWC array is VDAC and has to be shifted up to the minimum biasing point of input common mode voltage range of the comparator. A DC voltage source of 442mV is used for biasing, V_{ref} is equal to 250mV, terminating capacitor is equal 900fF, and sampling rate is 1KS/s.

There are four clock pulse sources which have different phases. Clk_Q1 is for control unit. Clk_Q2 is the main clock pulse signal for SAR logic unit. Clk_Comp is another clock pulse that is used for sending command to comparator for starting a new comparison where it pushes comparator from resetting time interval to regenerate time interval. Clk_Q1, Clk_Q2, and Clk_Comp operate at a frequency of 10 KHz.

Sampling/Hold is another clock pulse for switching between sampling mode and hold mode with an operating frequency of 1 KHz. All SAR logic unit and control unit will be reset by active restart signal (1 KHz). The D_0 to D_7 are the digital output code that is extracted and it is valid when Ready output signal is high.

4. SIMULATION RESULTS

The designed ADC is implemented in 180nm TSMC CMOS technology process and simulated using HSPICE. Though the recommended supply voltage for 180nm CMOS process is 1.8V, 1V supply voltage was used for the entire design of ADC and hence could reduce the overall power consumption of the ADC. All the individual units were simulated separately and then integrated for full functionality of the ADC. For the ADC to convert full range of analog input voltages to all the corresponding output digital levels, the comparator functionality has to be verified. The ideal V_{LSB} = (250mV/256) = 0.9765625mV and hence the comparator should be able to detect voltage changes less than V_{LSB}. Figure 6 shows the simulation result of the comparator for a ramp input with a sampling rate of 10 KHz. Once the ramp input voltage goes higher than the constant reference voltage, the comparator output toggles from high to low. It is evident from the simulation result that the comparator has sensitivity in the range of few μV and delay less than one half the clock cycle and hence meets the design requirements of this ADC. To simulate the ADC, input V_{in} can be a sinusoidal signal or a ramp voltage source whose peak to peak signal voltage varies from 0V to 250mV. For an 8-bit ADC the output digital code ranges from 00h (0d) to FFh (256d) which corresponds to the analog input voltage from 0V to 250mV (=V_{LSB}*256). Hence for output digital code to be 00h, the analog input voltage has to be less than 0.9765625mV and to get the output digital code of FFh, the analog input voltage has to be greater than 249.023mV. This has been verified from the simulation results shown in Figure 7 which was obtained by providing a ramp input signal to the ADC. The output digital code ranges from 00h to FFh for input ramp voltage varying from 0V to 250mV. The output digital code

ranges from 00h to FFh and it does not have any codes repeated or any codes being missed for the continuous analog ramp input signal sampled at 1 KHz. Hence the plot contains 256 samples which when plotted will be a linear.

The extracted first step input voltage range and the last step input voltage range are used for calculating the offset error and the full scale error which is given as follows:

$$Offset\,error = \frac{V_{in\ (\text{First step})} - \mathrm{V}_{ideal}}{LSB} = \frac{(0.960984m - 0.9765625m)}{0.9765625m} = -0.01626\mathrm{LSB}$$

$$FullScale\,error = \frac{V_{in\ (last\ \ step)} - V_{ideal}}{LSB} = \frac{(0.249671 - 0.24902344)}{0.0009765625} = 0.664LSB$$

Figure 7 and Figure 8 shows the static performance metrics namely INL and DNL error for the full scale output digital codes in terms of LSB. The maximum |INL| error measured is less than 0.218 LSB and maximum |DNL| error measured is less than 0.038 LSB which satisfies the ideal ADC design requirement of INL and DNL errors to be less than |0.5 LSB|. From Figure 9, it can be observed that its transfer function has no missing code and the ADC is monotonic. The transfer function is linear because each sampled input gives only one digital code. The ramp input provided for this simulation has a slope of 250mV/256ms and it is sampled at 1 KHz and hence gets only one input sample for each output digital code. Figure 10 shows the stair case waveform of the ADC for input voltage ramp of 250mV/1.024s, sampled at 1 KHz. Each code is obtained for four sampled inputs.

The average power consumption of the digital circuits and the total average power consumption of the ADC is measured and tabulated in Table V and Table VI respectively. Table V shows both dynamic and static power of the digital logic circuits. The total average power consumption of the designed CR-SAR ADC is 250.44 nW.

Figure 11 shows the layout of the designed CR-SAR ADC in standard TSMC 1P6M 180nm technology process occupying an area of 120μm × 55μm. For the capacitor array, first a unit capacitor C₵ (C0) is designed and then the larger capacitors are designed by connecting the unit capacitors in parallel in numbers of power of two in a common centroid structure. The unit capacitor is a parallel plate capacitor formed using Polysilicon-Insulator-Metal1 layer, octagon in shape to reduce the charge leakage in corners and the array is placed on n-well which is connected to V_{dd}. Using the unit capacitors to make the larger (n^{th} weighted) capacitors reduces the impact of process variations on the capacitors [20] [21]. A dummy capacitor array is placed around the capacitors for matching purpose.

Parasitic extraction is performed for this layout and post layout extraction simulation is performed to verify the simulation results. The post extraction simulation results are shown in Figure 12. For this simulation, the input voltage ramp of 250mV/1.024s is provided and it is sampled at 1 KHz. The transfer curve shows that the ADC does not have any missing codes and hence the ADC is monotonic which is similar to the schematic simulation results

shown in Figure 10. The simulation results also satisfy the ideal ADC requirement of INL and DNL errors to be less than |0.5 LSB|.

Monte Carlo simulations were performed on the RC extracted (post layout) layout considering a Gaussian distribution of all circuit parameter variations (PVT variations). Various circuit non-idealities such as capacitor mismatch, comparator input transistor mismatch, threshold voltage variations and temperature variations were considered for the simulations. A total of 300 iterations of Monte Carlo simulations were performed. The histogram and scatter plots of INL and DNL errors for all the 300 iterations are shown in Figure 13 and Figure 14 respectively. Out of the 300 Monte Carlo simulations that were performed, a total of 292 simulations had INL less than |0.5 LSB| and a total of 292 simulations had DNL less than |0.5 LSB|. Out of the 300 simulations that were performed, DNL and INL were more than |0.5 LSB| (out of range) only in 8 simulations. This corresponds to a yield of more than 97.33%. The peak-to-peak INL and DNL variations for corresponding simulations were less than 1 LSB for all the 300 simulations. Average power consumption of the designed CR-SAR ADC remained less than 250nW.

5. CONCLUSION

An ultra-low power 8-bit 1KS/s CR-SAR ADC was designed in 180nm TSMC CMOS process for ultra-low power biomedical applications. The ADC presented in this paper operates at an input signal voltage ranging from 0–250 mV which is beneficial for most of the biomedical devices and biosensors. The CR-SAR ADC designed in this paper is summarized in Table VII. As the speed performance is of least importance for most biomedical applications, a supply voltage source of 1V instead of 1.8V is used in our design which aided in the reduction of the total power consumption of the designed ADC. Following the design strategy of maximum simplicity in the architecture, the designed ADC consumes 250.44 nW of total power by using a binary-weighted capacitive DAC and by the elimination of separate S/H circuit. This ADC has no missing codes and it is linear and monotonic. In comparison to other published ADC designs shown in Table VIII, the ADC design presented in this paper has lower power consumption and occupies less chip area.

Acknowledgments

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References

1. Mortezapour S, Lee EKF. A 1-V, 8-bit Successive Approximation ADC in Standard CMOS Process. IEEE Journal of Solid-State Circuits. 2000; 35(4):642–646.
2. Maxim. Understanding SAR ADCs. Application Note 1080. Mar.2001
3. Sauerbrey J, Schmitt-Landsiedel D, Thewes R. A 0.5-v 1-μW Successive Approximation ADC. IEEE Journal of Solid-State Circuits. Jul.2003 38(7)
4. Ch Hong H, Lee GM. A 65-fJ/Conversion-Step 0.9-V 200-kS/s Rail-to-Rail 8-bit Successive Approximation ADC. IEEE Journal of Solid-State Circuits. Oct.2007 42(10)
5. Ginsburg BP, Chandrakasan AP. Dual Time-Interleaved Successive Approximation Register ADCs for an Ultra-Wideband Receiver. IEEE J Solid-State Circuits. Feb; 2007 42(2):247–257.

6. Louwsma SM, van Tuijl AJM, Vertregt M, Nauta B. A 1.35GS/s, 10b, 175mW Time-Interleaved AD Converter in 0.13μm CMOS. IEEE J Solid-State Circuits. Apr; 2008 43(4):778–786.
7. Mccreary JL, Gray PR. All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques – Part 1. IEEE Journal of Solid-State Circuits. Dec.1975 sc-10(6)
8. Fayomi CJB, Roberts GW, Sawan M. A 1-V, 10-bit Rail-to-Rail Successive Approximation Analog-to-Digital Converter in Standard 0.18μm CMOS Technology. IEEE International Symposium on Circuits and Systems. 2001; 1:460–463.
9. Promitzer G. 12-bit Low-Power Fully Differential Noncalibrating Successive Approximation ADC with 1MS/s. IEEE J Solid-State Circuits. Jul; 2001 36(7):1138–1143.
10. Scott MD, Boser BE, Pister KSJ. An Ultralow-Energy ADC for Smart Dust. IEEE Journal of Solid-State Circuits. Jul.2003 38(7)
11. Vermna N, Chandrakasan AP. A 25μW 100kS/s 12b ADC for Wireless Micro-Sensor Applications. ISSCC Dig Tech Papers. Feb.2006 :222–223.
12. Abdelhalim K, MacEachern L, Mahmoud S. A Nanowatt Successive Approximation ADC with Offset Correction for Implantable Sensor Applications. Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on. 2007:2351–2354.
13. Elzakker MV, et al. A 1.9μW 4.4fJ/Conversion-step 10b 1MS/s Charge-Redistribution ADC. ISSCC Dig Tech Papers. Feb.2008 :244–245.
14. Sauerbrey, Jens, et al. A 0.5V, 1uw Successive Approximation ADC. IEEE Journal of Solid-State Circuits. Jul.2003 38(7):1261.1265.
15. Zhong, Lungui, Yang, Haigang, Zhang, Chong. Design of an Embedded CMOS CR SAR ADC for Low Power Applications in Bio-Sensor SOC. IEEE, 1-4244-1132-7/07; 2007.
16. Karim A, MacEachern Leonard, Samy M. A Nanowatt ADC for Ultra Low Power Applications. IEEE, ISCAS, 0-7803-9390-2/06. 2006
17. Yin GM, Op't Eynde F, Sansen W. A High-speed CMOS Comparator with 8-bits Resolution. IEEE Journal of Solid-State Circuits. Feb.1992 21(2)
18. Kugelstadt, Thomas. The operation of the SAR-ADC based on charge redistribution. Texas Instruments Incorporated, Analog and Mixed-Signal Journal. Feb.2000
19. Hedayati, Raheleh. Master's thesis. Dept. of Electrical Engineering, Linköping Institute of Technology; Sep. 2011 A Study of Successive Approximation Registers and Implementation of an UltraLow Power 10-bit SAR ADC in 65nm CMOS Technology.
20. Shcherback I, Belenky AA, Yadid-Pecht O. Active-Area Shape Influence on Dark Current of CMOS Imagers. Proceedings of SPIE International Society of Optical Engineering. Apr.2002 4669:117–124.
21. Baker RJ. CMOS: Circuit Design, Layout, and Simulation (2nd Edition). Nov 1.2004
22. De Venuto D, Castro DT, Ponomarev Y, Stikvoort E. 0.8 μW 12-bit SAR ADC Sensors Interface for RFID Applications. Microelectronics Journal. 2010; 41:746–751.
23. Cheong JH, Chan KL, Khannur PB, Tiew KT, Je M. A 400-nW 19.5-fJ/Conversion-Step 8-ENOB 80-kS/s SAR ADC in 0.18-μm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs. 2011; 58(7):407–411.
24. Zhang D, Bhide A, Alvandpour A. A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13-μm CMOS for Medical Implant Devices. IEEE Journal of Solid-State Circuits. 2012; 47(7):1585–1593.
25. Kianpour I, Baghaei-Nejad M, Zheng L. 78 nW Ultra-Low- Power 17 kS/s Two-Step-Successive Approximation Register Analogue to Digital Converter for RFID and Sensing Applications. IET Circuits, Devices & Systems. 2012; 6(6):397–405.
26. Hu W, Liu Y, Nguyen T, Lie DYC, Ginsburg BP. An 8-Bit Single-Ended Ultra-Low-Power SAR ADC With a Novel DAC Switching Method and a Counter-Based Digital Control Circuitry. IEEE Transactions on Circuits and Systems I: Regular Papers. 2013; 60(7):1726–1739.
27. Yuan, C., Lam, YYH. A 281-nW 43.3 fJ/Conversion-Step 8-ENOB 25-kS/s Asynchronous SAR ADC in 65nm CMOS for Biomedical Applications. IEEE International Symposium on Circuits and Systems(ISCAS); Beijing, China. May 2013; p. 622-625.

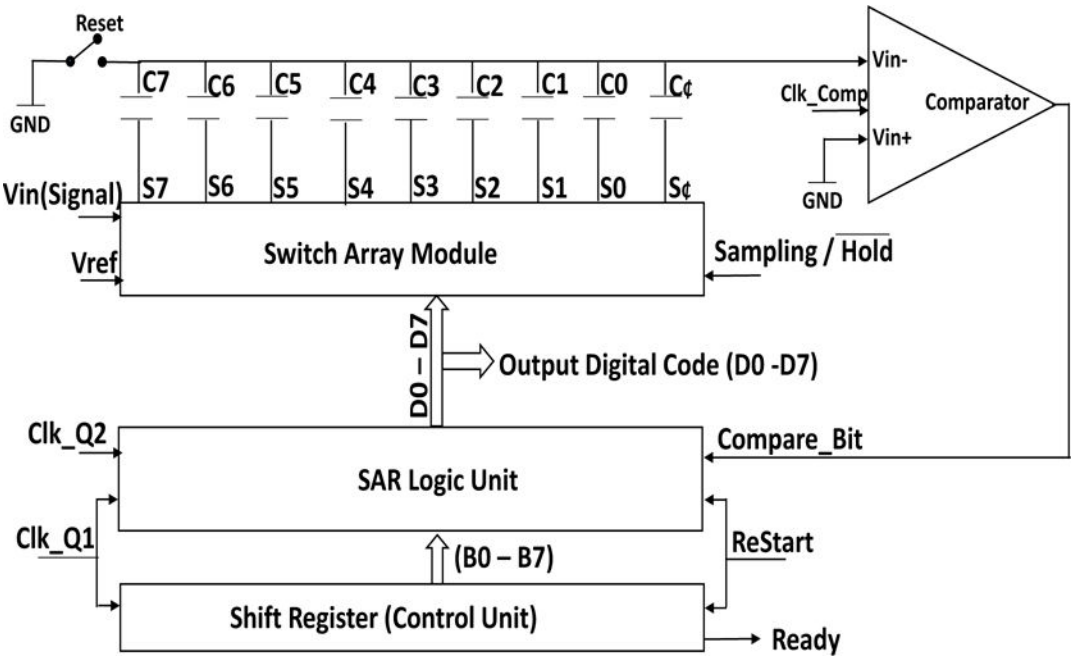


Figure 1.
Block diagram of the designed CR SAR ADC.

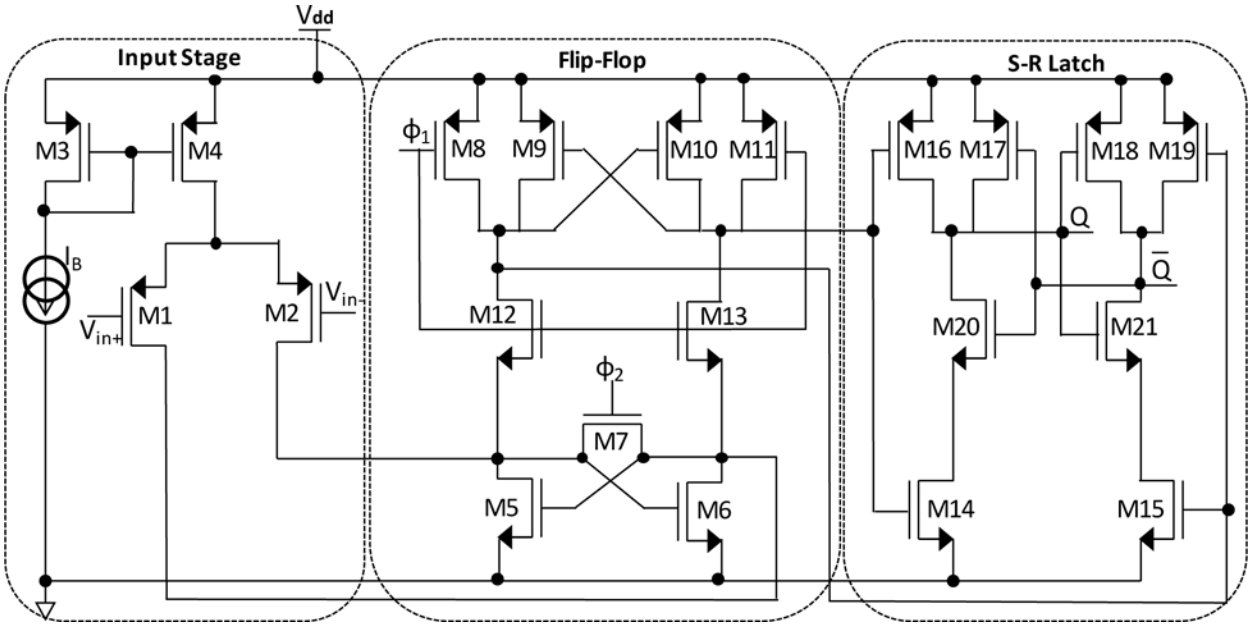


Figure 2.

Schematic design of the implemented high speed CMOS comparator with SR latch [17].

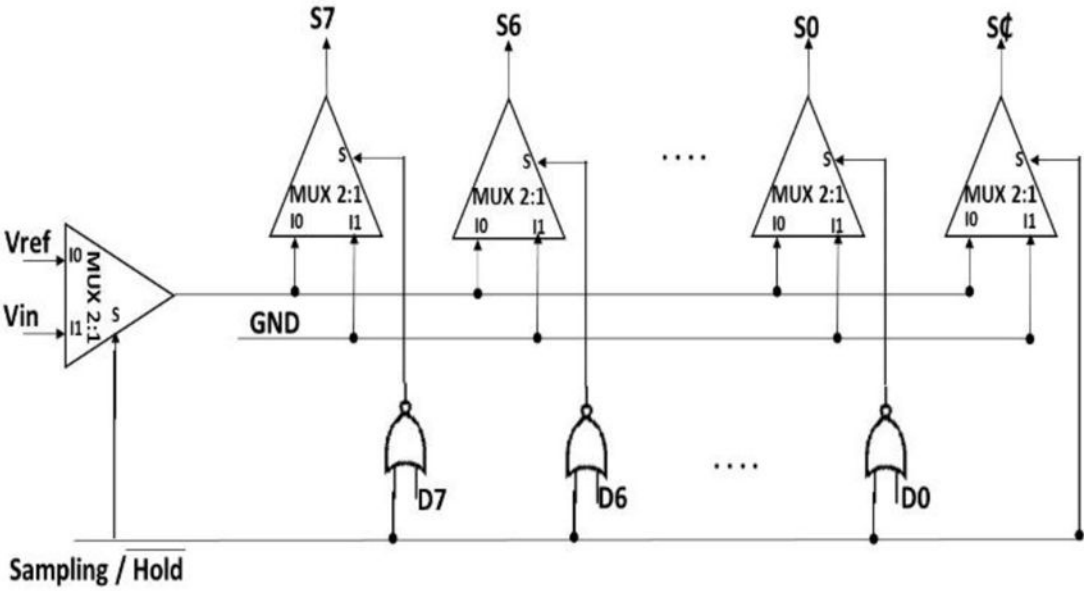


Figure 3.
Schematic diagram of the switch array module.

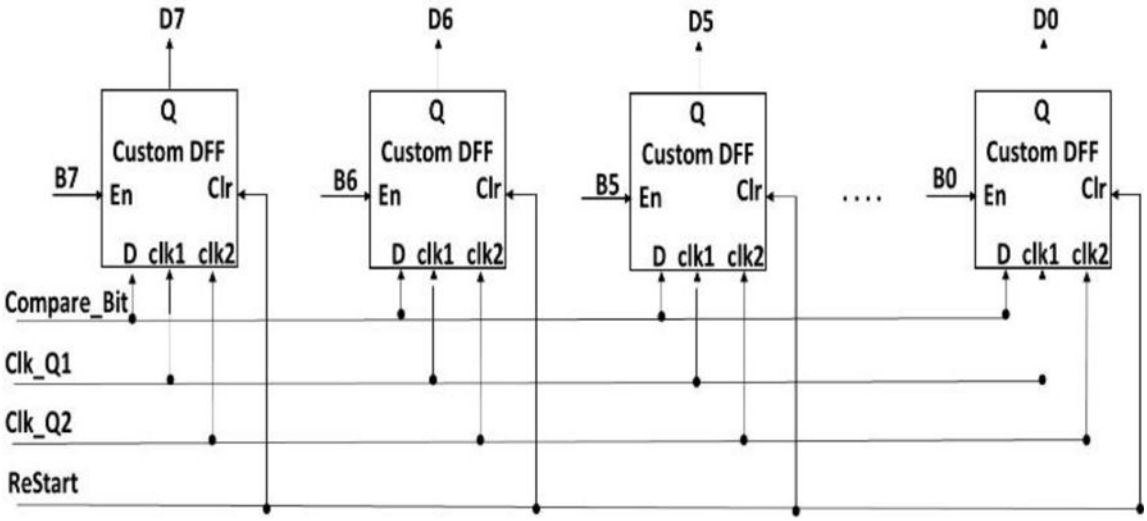


Figure 4.
Schematic diagram of the SAR logic unit.

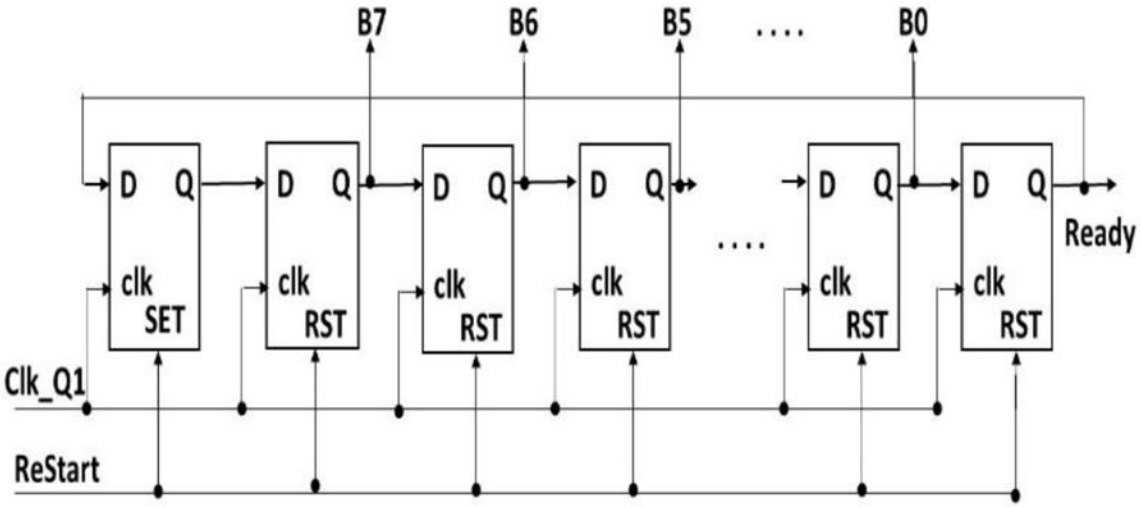


Figure 5.
Schematic diagram of the control unit.

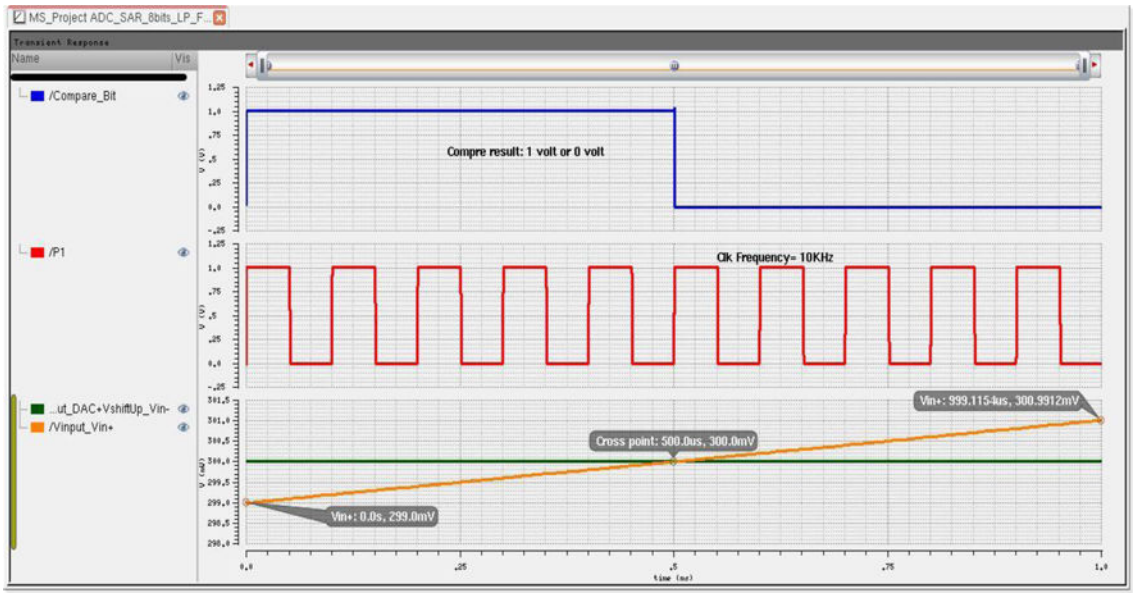


Figure 6.

Verification of comparator's propagation delay, with sensitivity <0.95mv and frequency =10 KHz.

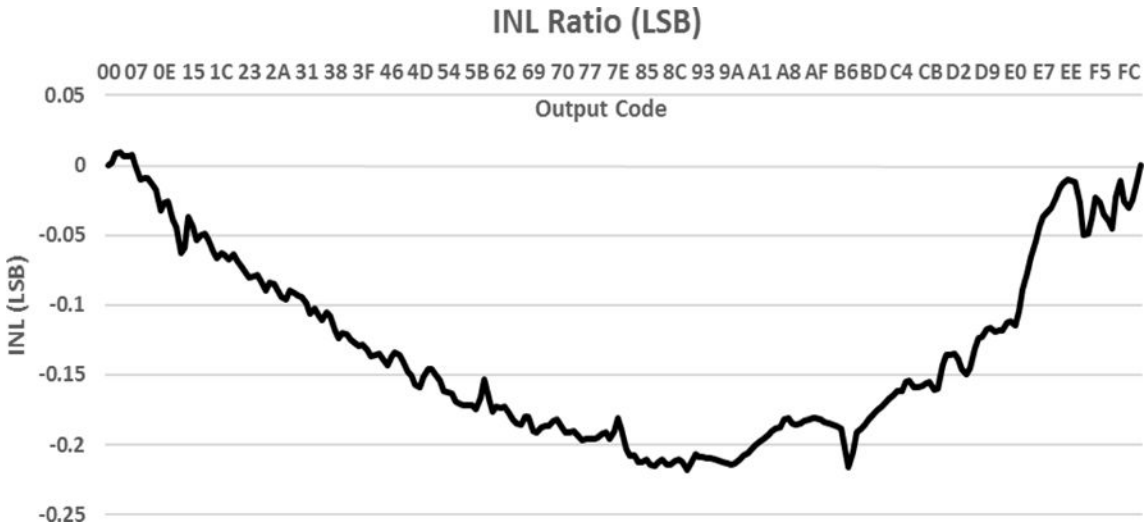


Figure 7.
Verification that |INL Ratio| is <0.218 LSB <0.5 LSB for CR SAR ADC.

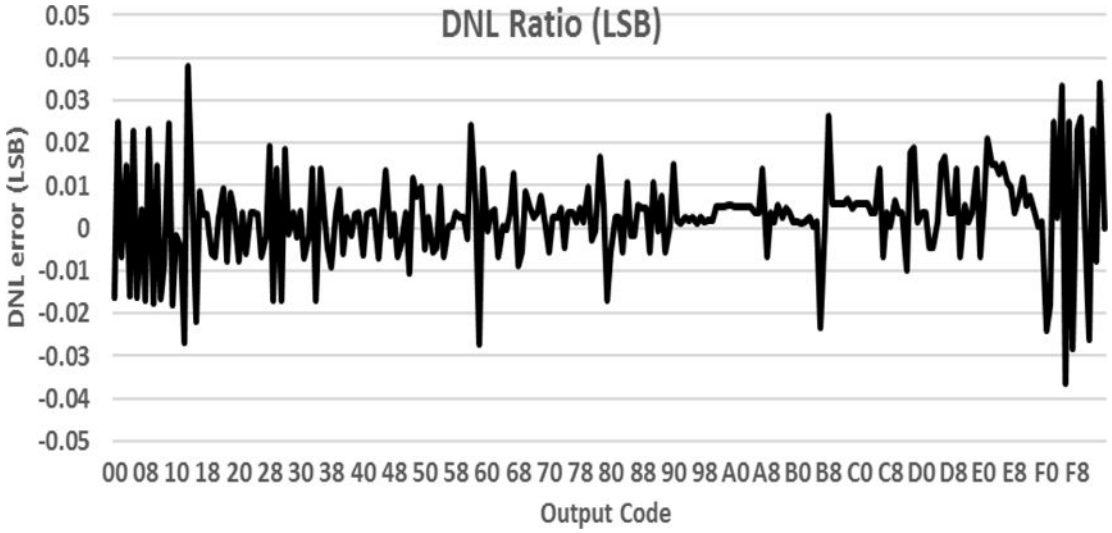


Figure 8.
Verification that |DNL Ratio| is < 0.038 LSB <0.5 LSB for CR SAR ADC.

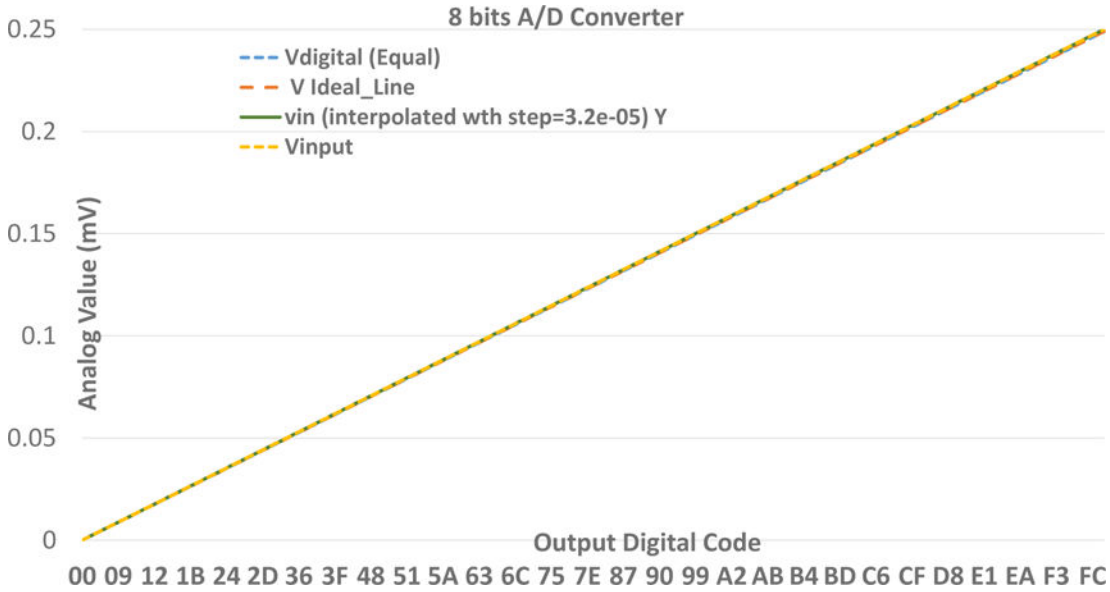


Figure 9.

The ADC transfer curve for 8-bit digital output code (00h to FFh) for input analog signal range (0mv to 250 mv, slope=976.56 mV/s), sampled at 1 KHz.

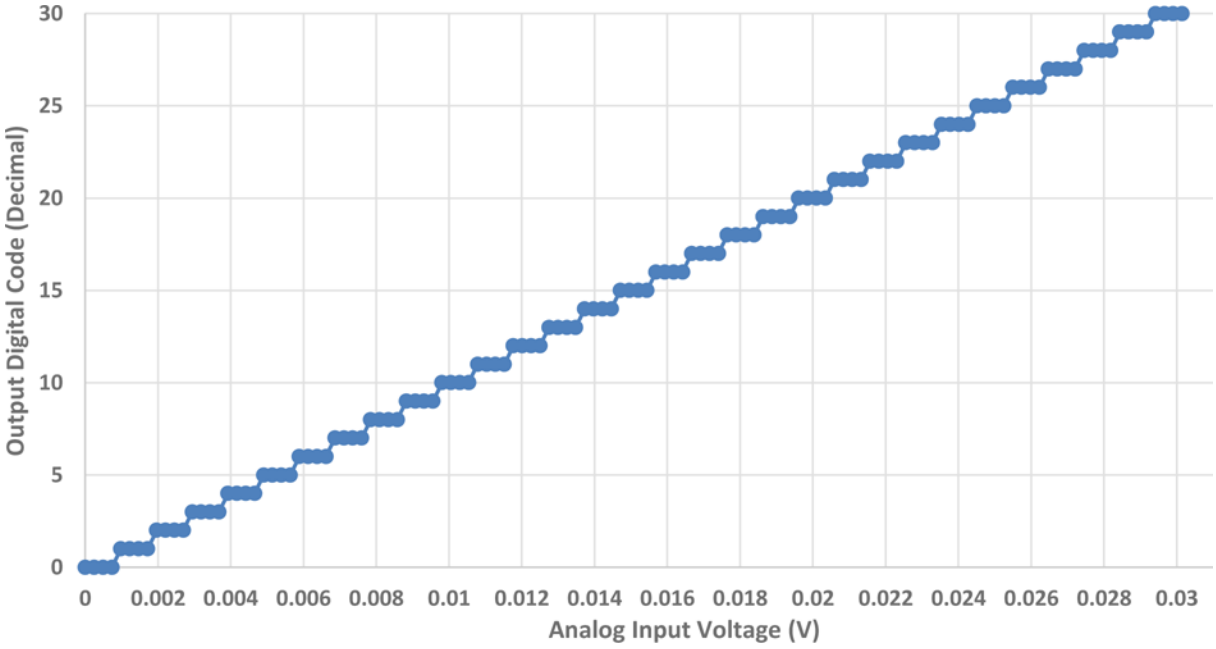


Figure 10.

The ADC transfer curve (Staircase waveform) for 8-bit digital output code (00d to 30d) for input analog signal with a slope of 244.14 mV/s, sampled at 1 KHz.

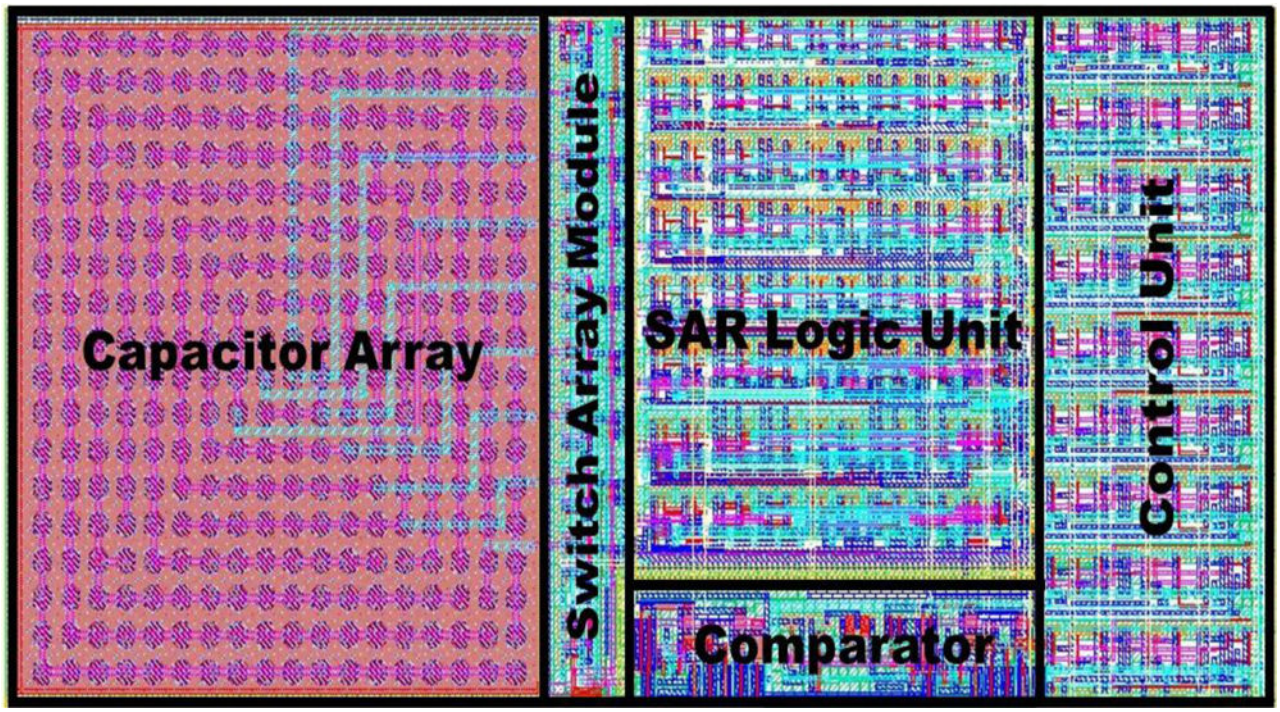


Figure 11.
ADC layout in standard TSMC 180nm technology (120μm × 55μm).

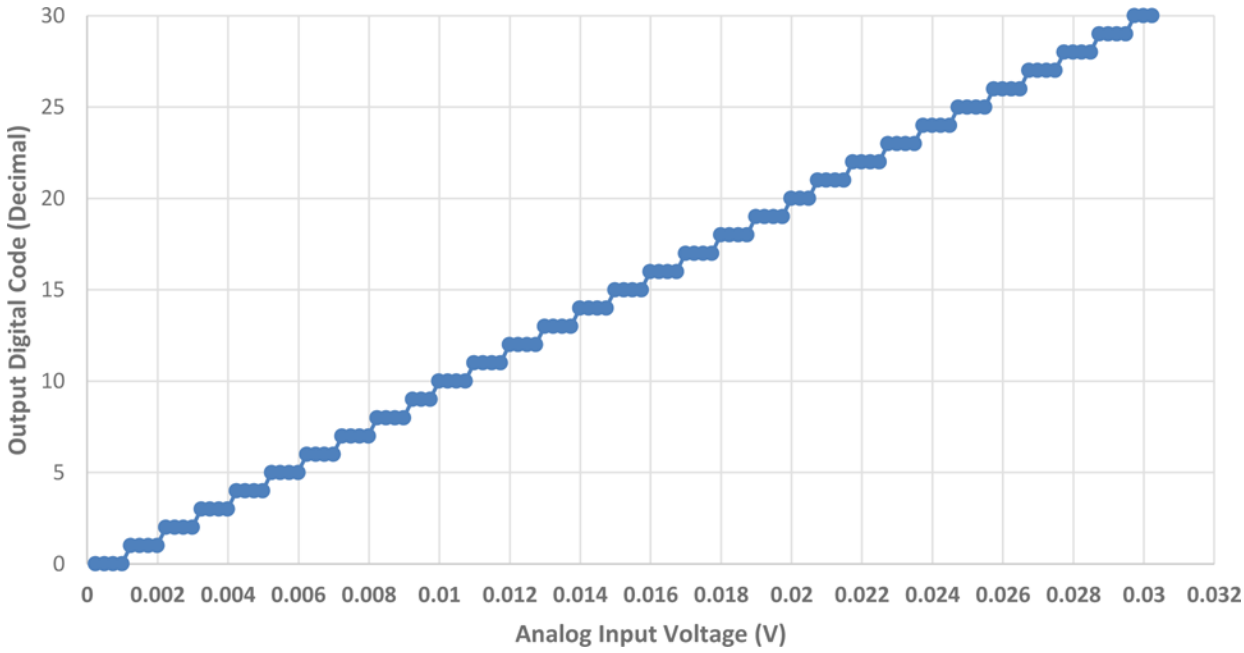
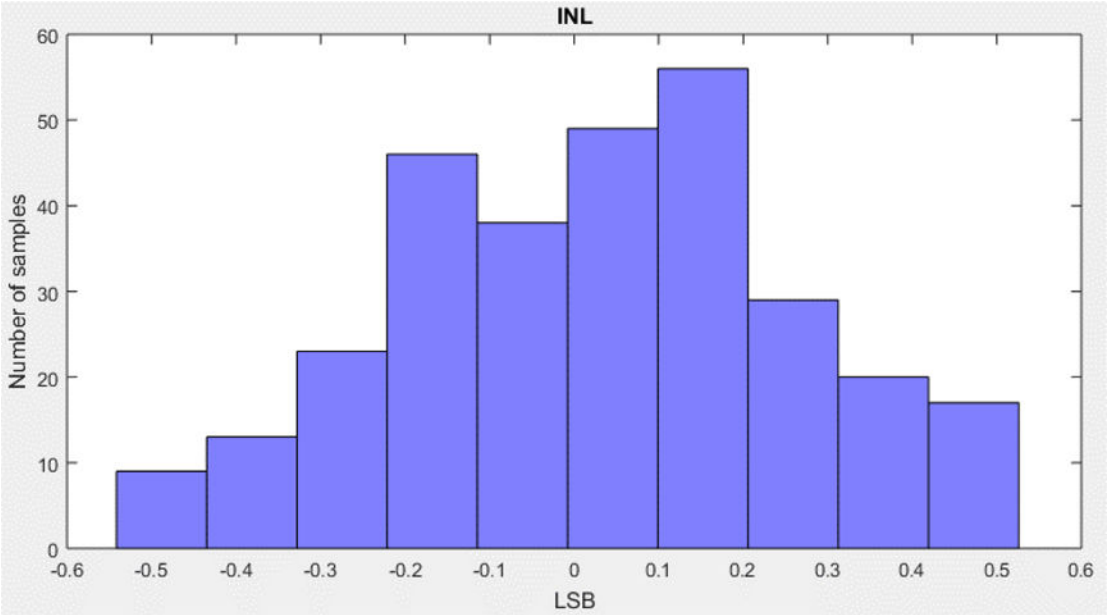
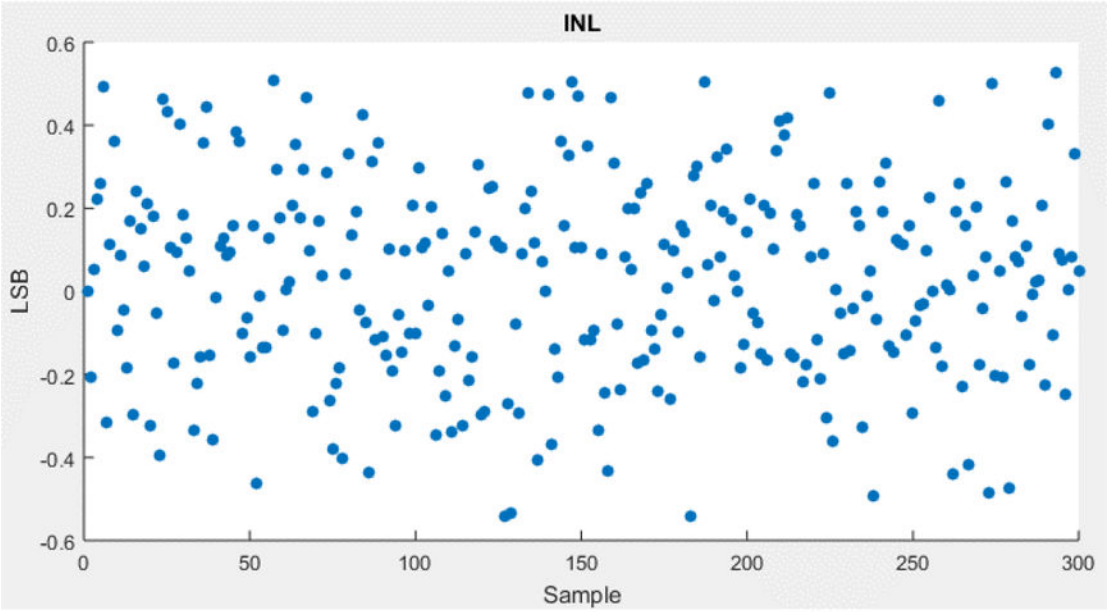


Figure 12.

Post layout extraction simulation: ADC transfer curve (Staircase waveform) for 8-bit digital output code (00d to 30d) for input analog signal with a slope of 244.14 mV/s, sampled at 1 KHz.



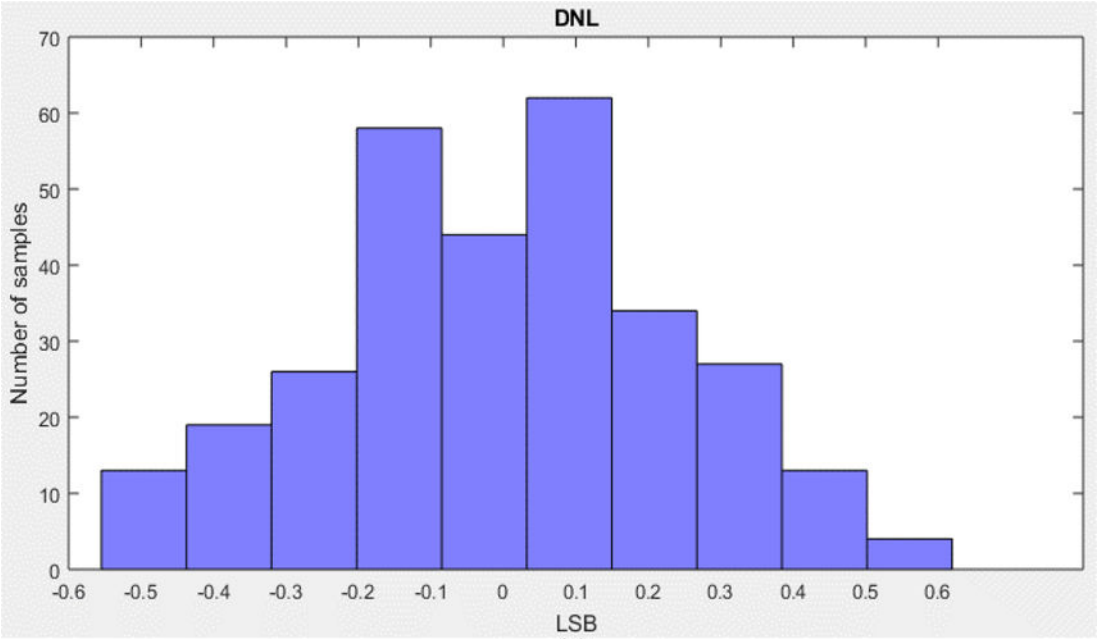
(a)



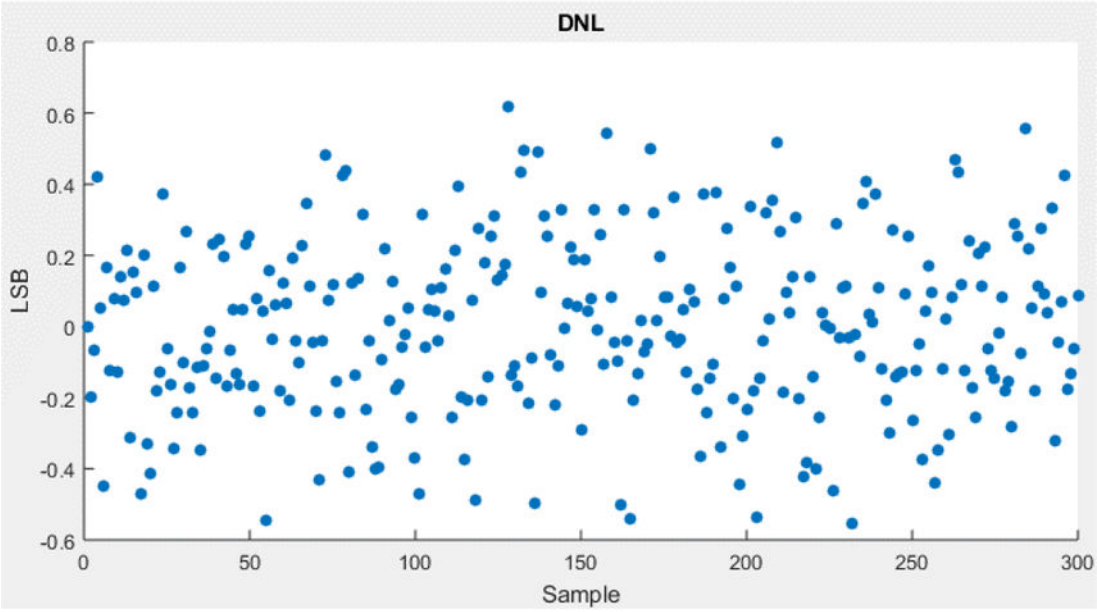
(b)

Figure 13.

Monte Carlo simulation results: (a) Histogram of INL error for 300 simulations (b) scatter plot of INL error for 300 simulations.



(a)



(b)

Figure 14.

Monte Carlo simulation results: (a) Histogram of DNL error for 300 simulations (b) scatter plot of DNL error for 300 simulations.

Table I

Orders of extracting digital bits for 8 bit ADC [19]

Cycle	Sample	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Comp
0	1	0	0	0	0	0	0	0	0	Start
1	0	1	0	0	0	0	0	0	0	a7
2	0	a7	1	0	0	0	0	0	0	a6
3	0	a7	a6	1	0	0	0	0	0	a5
4	0	a7	a6	a5	1	0	0	0	0	a4
5	0	a7	a6	a5	a4	1	0	0	0	a3
6	0	a7	a6	a5	a4	a3	1	0	0	a2
7	0	a7	a6	a5	a4	a3	a2	1	0	a1
8	0	a7	a6	a5	a4	a3	a2	a1	1	a0
9	0	a7	a6	a5	a4	a3	a2	a1	a0	Ready

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Table II

Transistors sizes for the designed comparator

Transistor type	Inverter	Input Stage	Flip- Flop	SR Latch
$PMOS\ \left(\frac{W}{L}\right)$	$\left(\frac{0.54\mu m}{0.18\mu m}\right)$	$\left(\frac{0.81\mu m}{0.81\mu m}\right), \left(\frac{0.27\mu m}{0.18\mu m}\right)$	$\left(\frac{4.05\mu m}{0.18\mu m}\right), \left(\frac{1.35\mu m}{0.18\mu m}\right)$	$\left(\frac{0.27\mu m}{0.72\mu m}\right)$
$NMOS\ \left(\frac{W}{L}\right)$	$\left(\frac{0.27\mu m}{0.18\mu m}\right)$	N/A	$\left(\frac{0.54\mu m}{0.18\mu m}\right), \left(\frac{2.43\mu m}{0.18\mu m}\right)$	$\left(\frac{0.27\mu m}{1.08\mu m}\right)$

Table III

Function table of the switch array module

Sampling/Hold	Di	Si / S¢
1 (Sampling Mode)	X	Vin / Vin
0 (Hold Mode)	0	GND / GND
0 (Hold Mode)	1	Vref / GND

Table IV

Function table of the customized DFF

Clk1	Clk2	Clr	Din	En	Function
X	X	0	X	0	No change
X	X	1	X	X	Clear DFF
0	1	0	X	1	Set DFF
X	↑	0	X	1	Load Din into DFF

Table V

Average power consumption of the digital circuits

Power	Measurements
Total dynamic power	115.2 nW
Total static power	741.52 pW
Total power consumption of digital part.	115.94 nW

Table VI

Average Power Consumption of the Designed ADC

ADC unit	Measurements
Total average power of digital circuits	115.94 nW
Average power of Comparator unit	134.5 nW
Total average power of the designed ADC	250.44 nW

Table VII

Summary of the designed CR SAR ADC specifications

CMOS Technology	0.18 μm TSMC process
Supply Voltage	1 V
Resolution	8 Bits
Input Range (Vpp)	250 mV
Conversion Rate	1KB/Sec
Power Consumption	250.44 nW
|INL| ratio	< 0.218 LSB
|DNL| ratio	< 0.038 LSB
Offset Error	− 0.01626 LSB
Full scale Error	0.664 LSB
Missing code	Does not occur

Table VIII

Comparison of the designed ADC with other publications

Publication	This Paper	Ref. [14]	Ref. [15]	Ref. [10]	Ref. [16]
Technology	0.18 μm	0.18 μm	0.35 μm	0.13 μm	0.13 μm
Supply Voltage	1 V	1 V	3.3 V	0.6 V	0.6 V
Resolution	8 bits	9 bits	10 bits	8 bits	8 bits
Input (Vpp)	250 mV	500 mv	1.5 v	300 mV	300 mV
Sampling Rate	10K S/s	150KS/s	1M S/s	100KS/s	60K S/s
Power	250.4 nW	30 μW	4.6 mW	950 nW	538 nW
FOM (fJ/Conv.)	97.6	390.63	4492.19	37.1	35.0
Active area (μm^2)	6600	110000	NA	52800	171000
FOM_{area} (μm^2/b)	825	12222	NA	6600	21375