Computación y Sistemas
ISSN: 1405-5546
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Instituto Politécnico Nacional
México

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Computación y Sistemas, vol. 20, núm. 4, 2016, pp. 723-728
Instituto Politécnico Nacional
Distrito Federal, México

ISSN 2007-9737

A 3μW Low-Power CMOS Class-AB Bilateral Current Mirror for Low-Voltage Applications

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Abstract. This paper presents a compact low-power bidirectional current mirror suitable for low-voltage applications. The key element is the use of a CMOS complementary input stage working in subthreshold regime; which allows setting a reduced bias current through the mirror. The circuit was simulated using LTSpice and presents class AB operation with a THD of 1% at 1MHz. The power consumption is close to 3μW as shown by simulations and experimental data from a fabricated prototype using 0.5μm CMOS technology.

Keywords. Analog integrated circuits, MOS integrated circuits.

1 Introduction

The current mirror is a basic analog building block which is widely used in OTA's, OP-AMP´s and other complex current mode circuits. Nowadays low-power requirements lead analog designers to consider class AB circuits due to their low quiescent current features and their capability to handle currents several times larger. Besides, voltage supply shrinking in modern fine line technology reduces considerably the voltage headroom for analog design; hence, solutions capable to work with a low-voltage condition and class AB operation are mandatory.

Many class AB current mirrors have been proposed in the past. In [1], extra circuitry was included for achieving class AB operation but, this extra complexity increases the minimum voltage requirement for the overall circuit. Other class AB approaches [2-6] improves the input/output impedance of the current mirror, however do not work for bidirectional currents and they are not able to work for low-voltage applications.

The low impedance output node of the Flipped Voltage Follower (FVF) has been extensively used for many applications including current mirrors [5-6]; in [6] the use of a FVF and a simple current mirror achieves class AB operation with low-voltage conditions. Although it is an interesting proposal, it is desirable to get simpler solutions at least for some applications. In this work, a very compact bidirectional current mirror is presented, which is able to deal with currents much larger than the bias current.

This paper is organized as follows: In the next section the proposed circuit is presented and explained. Section 3 presents electrical simulations; section 4 experimental results and discussion and finally; in section 5 conclusions are given.

2 Compact Class AB Current Mirror

According to [7], a given circuit works in low-voltage mode if its voltage supply V_{DD} is less than

ISSN 2007-9737

the sum of the complementary threshold voltages of NMOS and PMOS, i.e. $V_{DD}<|V_{THp}| + V_{THn}$.

In Fig. 1, a class AB current mirror proposed in [1] is shown. Here, transistors M3 and M4 set the bias current I_{bias} in the input branch. Therefore, these transistors can fix a reduced bias current for reduced static power consumption. Nevertheless, the branch of transistors M1 and M2 defines the minimum voltage supply requirement for the circuit, i.e. $V_{DDmin}=2V_{DSsat}+V_{GSp}+V_{GSn}$. Where V_{DSsat} is the minimum MOS overdrive drain-source voltage for saturation condition and considered for current sources I_{bias} implemented by a single MOS transistor. V_{GSp} is the MOS voltage gate-source which must fulfill $V_{GSp}>|V_{THp}|$ and $V_{GSn}> V_{THn}$ for operation in strong inversion regime.

Using 0.5µm CMOS technology with threshold voltages $V_{THn}=0.65V$ and $|V_{THp}|=0.95V$, the minimum supply for this circuit should be $V_{DDmin}=2V_{DSsat}+V_{GSp}+V_{GSn}$, i.e. $V_{DDmin} \geq 2V$. Thus, the proposal is not suitable for low-voltage applications.

The proposed current mirror is presented in Fig 2. This circuit is a simplified version of the previous circuit. From Fig. 1, the absence of transistors M3 and M4 lead to the circuit in Figure 2. Since for low voltage operation $V_{DDmin}<|V_{THp}| + V_{THn}$, must be fulfilled, this condition cause M1 and M2 in Fig 2, to work in moderate/weak inversion. The MOS subthreshold conduction at drain has an exponential dependency on V_{GS}, for $V_{DS}>200mV$ [8], this is:

$$I_D = I_0 \cdot \exp \frac{V_{GS}}{\zeta V_T}, \quad (1)$$

where $V_T = kT/q$, and $\zeta > 1$ is a nonideality factor.

This special feature sets a very small bias current on both branches, preserving the class AB operation. Thus, when a given current I_{in} is introduced into the circuit the input node goes high turning M1 PMOS “off” and turning M2 NMOS “on”. Therefore, the input current is well copied by the M2-M4 mirror. In case I_{in} is extracted from the circuit, input node goes low, therefore, M2 NMOS is turned off and M1 turned on bringing I_{in}. In this case the input copy is achieved by the PMOS counterpart to the output.

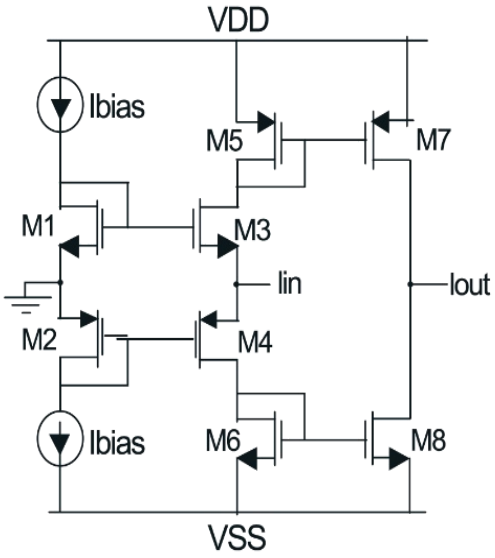

Fig. 1 Class AB current mirror

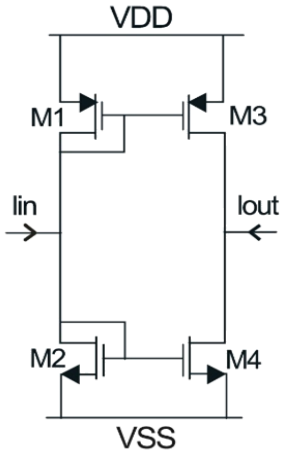

Fig. 2. Proposed current mirror

The input resistance of the circuit is given simply by:

$$R_{in} = \frac{1}{2 \cdot g_{mM1,2}}, \quad (2)$$

for the case $g_{mM1}= g_{mM2}$. The output resistance R_o is given in a similar way as $R_o=1/(2g_{dsM3,4})$.

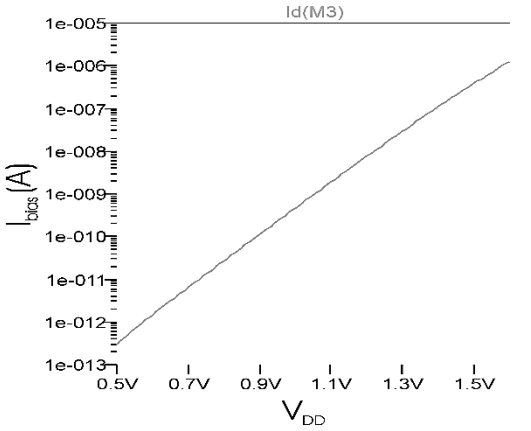

Fig. 3. DC simulations results, Bias current vs. V_{DD}

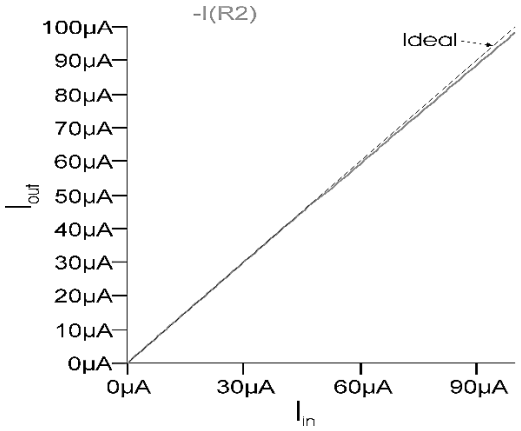

Fig. 4. Transfer function for different I_{in} values

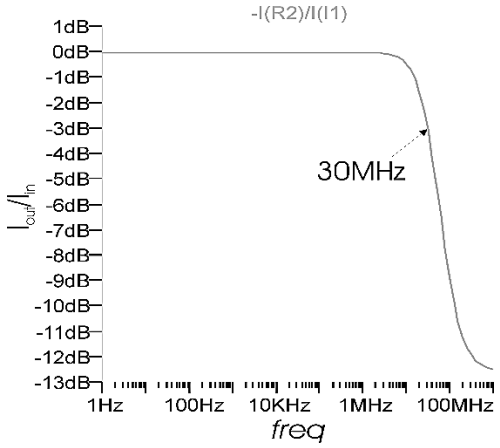

Fig. 5. AC simulation response

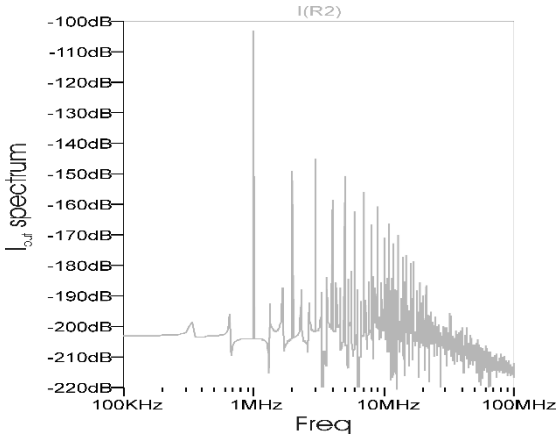

Fig. 6. Simulated output spectral response

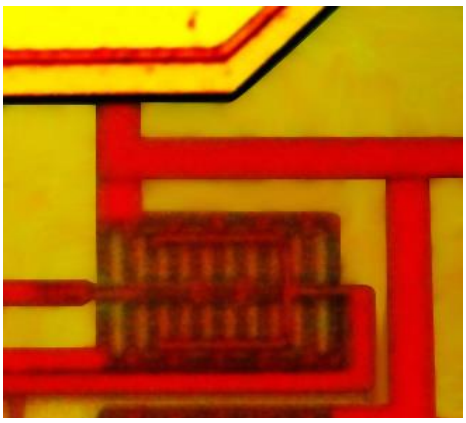

Fig. 7. Current mirror microphotograph

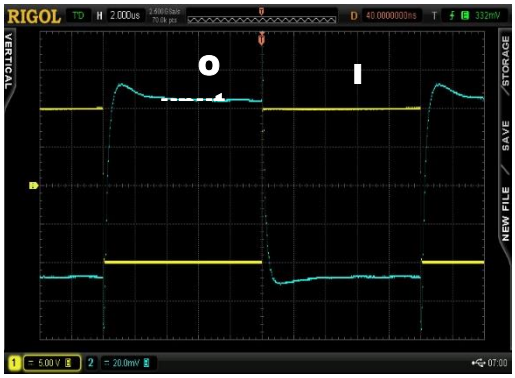

Fig. 8. Input/output traces of the current mirror considering a 1MΩ input series resistance and 47kΩ load resistance

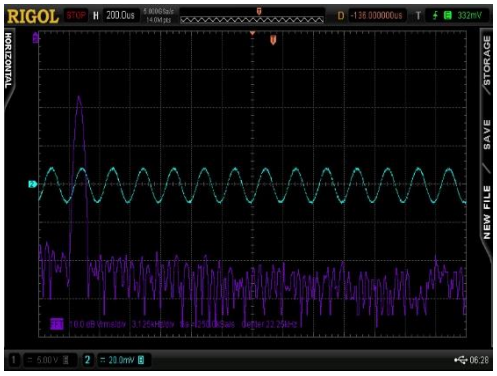

Fig. 9. Current mirror spectral response

3 Simulation Results

The circuit proposed in Figure 2 was simulated using Spice with BSIM3 version 3.1 model parameters from ON Semi 0.5µm technology available through MOSIS. Transistors aspect ratios are W/L=30µm/1.5µm for all NMOS and PMOS transistors.

In Fig. 3, the bias current of the circuit is plotted against different V_{DD} values. As can be noticed, bias current goes from several pA to µA. Nevertheless, in the range $1.4<V_{DD}<1.6$ the bias has a dependency on V_{DD} of 500nA/100mV.

For a V_{DD} = 1.58V, the bias current on both branches is close to 1µA. According to (1), the input resistance is close to R_{in}≈15kΩ and the output resistance R_{out}≈1MΩ.

In Fig. 4, a DC sweep simulation of I_{in} vs I_{out} is shown. The simulation shows the linearity of the current mirror for V_{DD} = 1.58V, since, the bias current is 1µA, the mirror can handle currents quite larger. In this plot, a comparison with the ideal behavior using a load of 1kΩ shows an error of 1.78%.

Fig. 5, shows the simulated AC response, the results show a cutoff frequency near to 30MHz for C_L=1pF and R_L=1kΩ. Since the circuit only presents a high impedance node at the output it has an unconditionally stable behavior.

The simulated output spectral response is shown in Fig. 6, for 10µA_p@1MHz input signal.

Distortion is introduced mainly by the third harmonic which is 42dB below the fundamental. The total harmonic distortion is close to 1%.

4 Experimental Results

The proposed current mirror was fabricated using 0.5µm CMOS technology. The circuit layout was developed using common centroid techniques and dummy structures in order to improve transistor matching. The microphotograph of the circuit is shown in Fig. 7, and the occupied silicon area was 37µm × 27µm.

The different tests were performed using a load of 47kΩ to measure the output current by a digital oscilloscope. The input current was introduced using a signal generator and a series resistance of 1MΩ.

In Fig. 8, the circuit was stimulated with an input square signal of 50kHz; the input current was 20µA_{pp} and the inverted output current shows a good performance with a 5% error in the copied current.

The spectral response was measured also with 5kΩ load and a sinusoidal input signal of 2µA_p@5kHz. The trace is shown in Fig. 9. THD was measured close to the simulations results, this is 1%.

Measurements were performed with V_{DD}=1.5V and 1µA bias currents. Hence, the circuit presents a static power consumption of only 3µW.

Table 1. Comparison among other CMOS current mirrors

work	[3]	[4]	[6]	This
R_{in}	18Ω	15Ω	-	15kΩ
R_o	11MΩ	650MΩ	-	1MΩ
BW (MHz)	120	100	10	30
Power (μW) consumption	165	264	~30	3
V_{DD} (V)	3.3V	3.3V	1.5V	1.58V
Silicon area	140× 130μm	295× 75μm	-	37× 27μm
Transistor Count	17	23	8	4

In Table 1 a comparison among other approaches is presented, as well know, there is a clear relationship between performance and power consumption. Nevertheless, each circuit has own properties in order to be used for a given application. The circuit proposed could be considered as a good choice for low-power and low complexity applications.

5 Conclusions

In this work, a very compact and simple low-voltage, class AB bidirectional current mirror is presented. The circuit can drive currents much larger than its static bias current as shown through simulations and experimental measurements. The circuit has an unconditionally stable behavior due to the existence of only one high impedance node, thus, no compensating passive elements are required.

The simplicity of the circuit makes it feasible for low-power/ low-voltage applications.

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Article received on 10/08/2016; accepted on 08/11/2016.
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