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High Resolution Digital Pulse Width Modulator Architecture using Reversible Synchronous Sequential Counter and Synchronous Phase-Shifted Circuit

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Abstract

Nowadays, the DC-DC converter digital control is more attracted due to its benefits, like programmability, enhanced control algorithms. As a vital part of digital control, the digital pulse width modulator (DPWM) is designed to satisfy various requirements for higher performance. The existing digital pulse width modulator architecture activated with higher resolution along higher switching frequency, also the mandatory counter clock frequency is higher. To overcome this issue, the hybrid digital pulse width modulator architecture is proposed that combines Reversible Synchronous Sequential Counter and synchronous phase-shifted circuit. The proposed architecture consists of 4 blocks, they are, decoder, synchronous reversible counter, Synchronous Phase- Shifted Circuit, Delay line. The decoder is used to divide the input duty cycle command (DCC) into three parts: most significant bits (MSB), secondary significant bits (SSB) and least significant bits (LSB). The Reversible synchronous counter is used to count trigger signal in every clock period. Here, synchronous phase shift circuit is utilized to select the clock through the quadrant phase-shifted clocks. The delay line is used to set the time resolution of DPWM. In this work, D-Flip flop is used to leave

sufficient slack among the set signal and reset signal for averting glitch. It can achieve high linearity resolution together with time resolution. The coding is done in Verilog and the proposed synchronous counter design has been synthesized using Xilinx ISE. Here, the assessment metrics, such as path delay, linearity, output duty cycle and time resolution are analyzed. The performance of the proposed SCD-MCT-MCF design shows higher output cycle 26.75%, 29.93% is compared with the existing design such as high resolution DPWM depending on synchronous phase-shifted circuit and delay line (Hyb DPWM-SPSE-DL), Delay-Line DPWM Architecture with Compensation Module and Delay-Adjustable Unit depending on Delay Line (Hyb DPWM-DLP) respectively.

Keywords: *Digital pulse width modulator, Decoder, synchronous reversible counter, Synchronous Phase- Shifted Circuit.*

1. Introduction

Generally, Digital pulse width modulator (Radhika et al,2021) is used in electronic devices that are power management chips (Rao and Chakravarthi,2020), LED drivers (Yu and Murari,2021), base band signal processing etc. In DC-DC (Rao and Chakravarthi,2020) converters are implemented using the DPWM with the advantages as insensitivity to process, voltage, temperature (PVT) variations (Papananos et al,2020), programmability advanced control algorithms, wide applicability while compare with the general analog DC-DC converters. DPWM act as a converter for the distinct duty cycle signal to an analog pulse width modulation signal that drives power transistors and it produce high resolution (Cheng et al,2020), good linearity and low power consumption. High-resolution pulse-width modulator (HRPWM) is has high precision in the pulses edges and the resolutions exceeds the period of the system clock. Counter-based DPWMs are direct signals for analog pulse width modulation, in which n-bit counter imitates triangular waveform that are likened to the digital code K[n] for producing output signal (Alzaher and Alghamdi,2020; Kipenskyi et

al,2020). Delay-line-based structures are used as the propagation delay in 2^n delay element (DE) linked in the cascade to produce the higher resolution pulse width modulation signal utilizing 2^n input multiplexer including input signal $M[n]$ to select various delay cells outputs (Crovetti et al,2020; Petric et al,2021).

In this manuscript, hybrid DPWM architecture is proposed which combines 4 blocks. Hybrid DPWMs are executed by incorporating reversible counter, synchronous phase-shift circuit, delay line and phase locked loop (PLL). Here, HDPWM is normally use this phase locked loop to create 4 phase-shift clocks, then the time resolution is equivalent to delay among 2 nearby phase-shift clocks. By using the delay cells, the delay line base hybrid structure is designed. The hybrid structures give the counter clock frequency requirement as well as upgrade the time resolution, linearity. The cascaded DCMs have been utilized to DCM-base and delay line-base design to maximize the resolution. These 2 models not only minimize the linearity of digital PWM, but also maximize the delay of critical path along resource (area). These designs are affected through the tradeoff between the linearity, time resolution, resolution, resource (area).

The main contributions of this manuscript is summarized as,

- In this manuscript, hybrid DPWM architecture is proposed which combines Reversible Synchronous Sequential Counter and phase-shifted circuit.
- The proposed architecture consists of 4 blocks such as Decoder, synchronous reversible counter, Synchronous Phase- Shifted Circuit, and Delay line.
- The decoder is used to divide the input duty cycle command (DCC) into three parts: most significant bits (MSB), secondary significant bits (SSB) and least significant bits (LSB).
- The counter is used to count trigger signal in every clock period. In this, synchronous phase shift circuit select the clock through quadrant phase-shifted clocks.

- For predicting the output, the circuits uses D-Flip flop to leave sufficient slack among the signal of set and reset for averting glitch.
- It can reach higher resolution when remains optimum linearity performance with time resolution.
- The delay line is used to set the digital pulse width modulator time resolution. The coding is done in Verilog and the proposed synchronous counter design has been synthesized using Xilinx ISE.
- Here, the assessment metrics such as path delay, linearity, output duty cycle and time resolution are analyzed.
- The efficiency of the proposed HRDPWM-RSSC-PSC design is likened to the existing methods, like high resolution DPWM depending on synchronous phase-shifted circuit and delay line (Hyb DPWM-SPSE-DL) (Cheng et al,2020), Delay-Line DPWM Architecture with Compensation Module and Delay-Adjustable Unit depending on Delay Line (Hyb DPWM-DLP) (Sun et al,2020) respectively.

Remaining manuscript is delineated as: section 2 reviews the recent studies, section 3 illustrates about the proposed design, section 4 proves the results with discussion, and section 5 concludes the manuscript.

2. Literature Survey

Among the frequent research work on DPWM; some of the latest investigations were assessed in this part,

In 2020, Cheng, et.al, (Cheng et al,2020)have presented the synchronous phase-shift circuit with delay line based higher resolution digital PWM. The critical path performance was analyzed by the synchronous phase-shift circuit then the resolution of time was improved with the help of delay line depending on carry chain. Similarly, the combined process shows

the hybrid DPWM. Finally it gives high linearity and the time resolution. This method was limited due to output variations.

In 2020, Sun, et.al. (Sun et al,2020) have presented a Delay-Line digital pulse width modulator with Compensation Module, Delay-Adjustable Unit depends upon Delay Locked Loop. While the Duty cycle resolution was increased, digital pulse width modulations affected on its clock frequency, temperature as well as time error and it becomes larger. Delay-adjustable unit was depending on multiplexer, delay paths along various delay time, which frequently reduce the temperature or frequency via the input clock. Error was reduced using the time compensation technique by the critical path. Its temperature was high.

In 2020,Morales, et.al., (Morales et al,2020) have presented a high-resolution all DPWM structure along tunable delay element in CMOS. It was depending on digitally controlled delay element which was the combination of the uneven time interval up to 54 picoseconds, adjustable against PVT variations. The Hybrid DPWM allows for getting the duty cycle with 18-bit resolution and it could not use the internal clock with high frequency and the low power dissipation also maintained. HDPWM has improved performances, but it was limited due to delay.

In 2021,Arora,,et.al., (Arora et al,2021)have presented the Digital Pulse Width Modulation Using Direct Digital Synthesis. DPWM was digitally controlled power converters. It was cost effective, high performance as well as functionally integrated with small packaged-sized. Where, delay was increased.

In 2021,Bhardwaj,,et.al., (Bhardwaj et al,2020)have presented a FPGA-Base High-Resolution DPWM Scheme utilizing Interleaving of Phase-Shifted Clock Pulses. The DPWM was utilized in switch mode power converts to make higher frequency pulses and to give the semiconductor switching circuit. DPWM was developed to generate the resolution of DPWM and the advanced FPGA clock management. The 13-bit digital PWM along 45 phase-shift

clock pulses interleaving was carried out in Spartan3AN FPGA kit utilizing 10 MHz clock frequency for obtaining 12.5 ns the DPWM resolution, which was 8 times superior to that acquired by the simple counter-base model. The presented method consumes high power dissipation.

In 2021,Nguyen, et.al., (Nguyen et al,2019) have presented the Phase-shifted carrier pulse-width modulation along enhanced dynamic performance for modular multiple level converters. The presented algorithm as well as capacitor voltage balancing control removes the tedious proportional-integral parameter tuning process requirement. It enhances the dynamic performance compared to the conventional methods. It consists of high modality, easy scalability. The presented method was limited due to low frequency.

In 2021,Cheng, et.al., (Cheng et al,2021) have presented the higher resolution hybrid DPWM (HRHDPWM) along dual-edge-trigger flip-with hardware compensation. HRHDPWM was designed using the counter, a phase shift circuit and carry chain. Dual-edge-triggered flip-flops were utilized to create the signals including 45^0 phase shift in the phase-shifted circuit and the hardware compensation was used to maximize the duty cycle which affect the regulation accuracy of the converters. It was used to reduce the resource compensation but it was consumes high power.

3. Proposed methodology

In this, the DPWM architecture is designed and it is given in Figure 1. It includes decoder, proposed reversible synchronous counter, phase-shifted block, delay line and D flip-flop. Here, the input duty cycle command is denoted as $dcc\left[a-1:0\right]$, input clock for phase locked loop is denoted as CLK_in and the output signal of digital pulse width modulator is denoted as $Output_{DPWM}$. The detail description about each blocks used in digital pulse width modulator is given below,

3.1. Decoder

The purpose of decoder is to divide the input duty cycle command $\{dcc[a-1:0]\}$ as $dcc_1[a-1:b]$, $dcc_2[b-1:b-2]$ and $dcc_3[b-3:0]$. Here $dcc_1[a-1:b]$ denotes input duty cycle command most significant bits, $dcc_2[b-1:b-2]$ denotes input duty cycle command secondary significant bits, $dcc_3[b-3:0]$ and denotes input duty cycle command least significant bits.

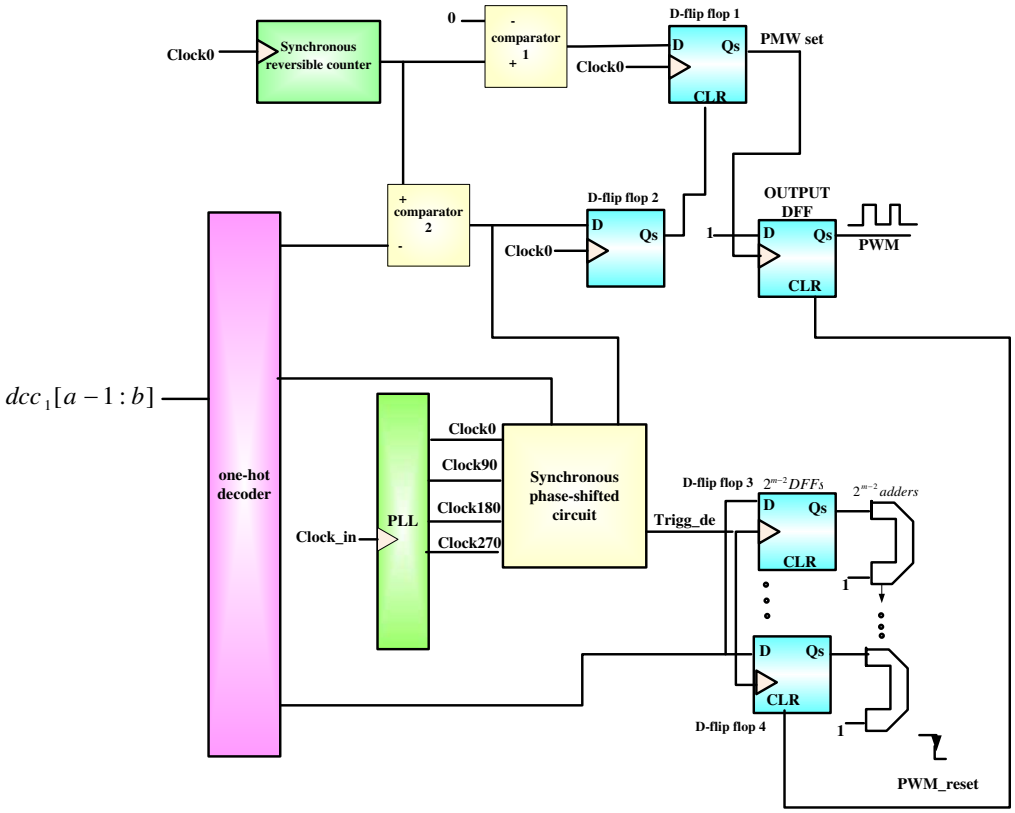

Figure 1: Proposed design of High Resolution Digital Pulse Width Modulator Architecture

3.1.1. Reversible synchronous sequential counter

In high resolution DPWM, the reversible synchronous sequential counter is proposed. The reversible logic is used because of its low power consumption and less delay. Here the reversible synchronous counters are designed using Multiple Controlled Toffoli (MCT) as well as Multiple Controlled Fredkin (MCF) reversible logic gates using 3- JK flip flops. JK_1 and Jk_2 flip flop is designed using the Multiple Controlled Toffoli (MCT). Similarly, JK_3 flip

flop is implemented using the multiple controlled Fredkin gate. Basically the MCT gate does the following gate functions, such as NOT, AND, NAND, XOR. For JK_3 flip flop, multiple controlled Fredkin gate is used. The reversible multiple controlled Fredkin gate does the following gate functions such as NOT, AND, OR, NOR. By this delay is reduced, power consumption is low and the speed is increased in Proposed Reversible Synchronous Counter with Multiple Inputs and Outputs. Figure 2 shows the Synchronous reversible counter design using MCT and MCF reversible logic gates.

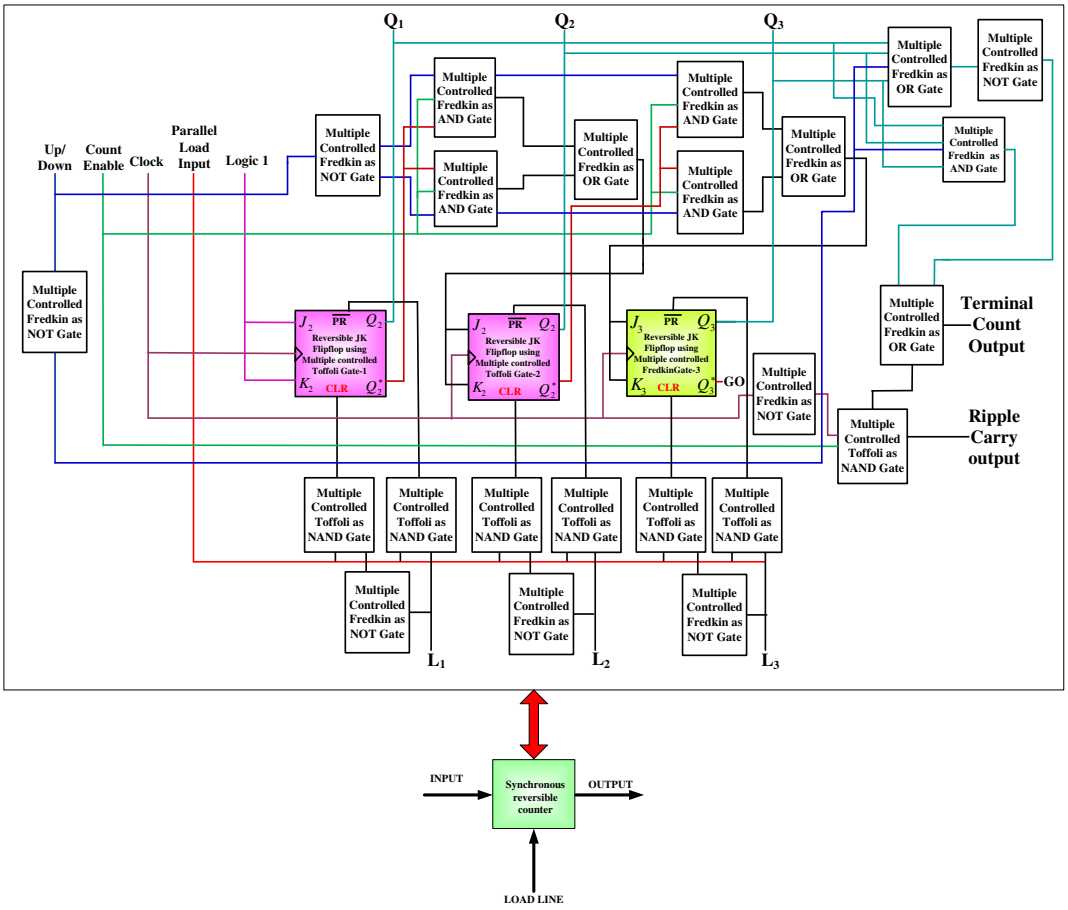

Figure 2: Synchronous reversible counter design using MCT and MCF reversible logic gates

The synchronous counter block is utilized to set PWM_SET signal for getting the D-flip-flop output as well as trigger signal $Trigger\_signal$ to the reversible synchronous phase shift circuit. At Figure 1, PWM_SET is produced while the output of counter is same as 0. At this time, the output of the comparator is compared with the decoder 1 $dcc_1[a-1:b]$ with

the comparator-2. If the counter is equal to $dcc_1[a-1:b]$, trigger signal ($Trigger\_signal$) is in active state. After that the 2-D-flipflops are provides as the synchronous process. In this P_S is represented as the relationship among the switching period, $CP_{counter}$ is represented as the clock period of the counter and its equation is given in equation (1)

$$P_S = 2^{a-b}.CP_{counter} \tag{1}$$

3.1.2. Synchronous Phase- Shifted Circuit

This circuit is selected the clock via the quadrant phase-shifted clocks. In the previous synchronous phase shift circuit 4:1 MUX is used, it cause unexpected nonlinearity problem, so that the MUX block is replaced with the D-flip flops. It consists of on-chip PLL, 4 D-Flip flop, 4 AND gate and 1 OR gate. The PLL is used to generate four quadrant phase-shifted clocks, such as $Clock\,0, Clock\,90, clock\,180,\ and\, clock\,270$ with 50% duty cycle. In this $Clock\,0$ represented as the counters clock signal of positive edge generator. In this 4 D-flip-flops are used and its clock inputs/signals are taken from the four phase-shifted clocks. From this the first D-flip flop 1 takes the $Trigger\_signal$ from the positive edges of the $clock\,1$ for generating the trigger signal-1 that is $Trigger\_1$. Similarly, D-flip flop 2, D-flip flop 3, D-flip flop 4 generates the Trigger signal 1, 2, 3, 4 that is $Trigger\_1, Trigger\_2, Trigger\_3$, $Trigger\_4$. While transmitting the trigger signal to the D- flip flops and it generate the trigger signal as $Trigger\_n(n=1\approx 4)$ only on phase shifted clocks positive edges. In this, $Trigger\_n(n=1\approx 4)$ is known as the optimum phase-shift clocks that synchronized the trigger signal and phase-shift clock propagation path. While using D flip flop, the clock delay problem is reduced, because the D-flip flops wait till the +ve edge of related phase-shift clock reaches for capturing the prior DFF output. And trigger signal $Trigger\_n(n=1\approx 4)$ problem also reduced, while crossing the two adjacent DPWM switching periods, therefore the D-Flip flops 1, D-Flip flops 2, D-Flip flops 3, D-Flip flops 4, are reset by $Clock\,90\, and\, clock\,180$,

$Clock\,180\,and\,clock\,270$, $Clock\,270\,and\,clock\,0$ and $Clock\,0\,and\,clock\,90$ respectively. After replacing MUX, the synchronous phase shift circuit utilizes 4 two-input AND gates together with 1 four-input OR gate. To assure these gate locations are set in location allocations, the restriction for global signal on every path is needed, thus creating every path equivalent delay. The 4 AND gates outputs are injected into 4-input OR gate. By then, Synchronous Phase- Shifted Circuit is designed for digital pulse width modulator (DPWM) design.

3.1.3. Delay Line

Delay line is used to set the time resolution of DPWM. The propagation delay of carry bit in every added is constant then it is able to predict the values from 10-100ps. Similarly, to check the linearity, the carry chain total delay is equivalent to delay among the 2 adjacent phase shifted clock (D_{CPS}). The carry chain uses 2^{b-2} adders and its equation is given in equation (2)

$$D_{CPS} = 2^{b-2}.D_c \tag{2}$$

Where, D_c represents carry delay of the adder. Figure 1 contains Reversible synchronous counter, delay line, synchronous phase-shifted circuit and resolution of this circuit is given as a and it is represented as the number of bits. Thus, higher resolution DPWM is recognized by maximizing the bits count of counter, count of cascaded phase-shifted circuits, or delay line length. When maintaining better presentation of linearity with time resolution, it reaches greatest 18-bit resolution.

By using Reversible synchronous counter, synchronous phase-shifted, delay line, and the resolution of this circuit is given as a and it is represented as the number of bits parameters the high resolution DPWM is designed. To design the high resolution DPWM with the needed time resolution D_c, first design parameter a. In this, a is designed for compromising resource (area) and power. If the power is increased more number of adders are included. For

reducing the power and area less number of adders are used according to the equation (2) therefore the use of counter is also lowered. Therefore, the counter's clock period is given in equation (3)

$$CP_{counter} = 2^{b-2}.D_c \tag{3}$$

The switching period of digital pulse width modulator is given in equation (1) that is $P_S = 2^{a-b}.CP_{counter}$. This block output denotes $PWM\_\mathrm{Re}set$ and it represents reset signal of output D-Flip flop. By this process, the negative edge of the DPWM pulse is generated.

3.1.4. Output of D-Flip flop

In this work, D-Flip flop is used to cause sufficient slack among the set signal and reset signal and to avert glitch. It can achieve high resolution of linearity and time resolution. While using RS latch, the slack is not able to predict, delay is non-negligible, and not able to calculate the time. So, the digital pulse width modulator with RS latch does not create small pulse width that restricts range of duty cycle. So, the proposed architecture D-Flip flop is used for predicting the output instead of RS latch. The output is predicted in the D flip flop, where set as each time of PWM_Set and reset positive edge at the same time, when $PWM\_\mathrm{Re}set$ in delay line is produced. By this process, the slack among the signal of set and reset requires to fulfill the set time as well as DFF hold time that is small duty cycle has permitted to attain.

4. Result and Discussion

In this section, hybrid digital pulse width modulator architecture is proposed that combines Reversible Synchronous Sequential Counter and synchronous phase-shifted circuit is discussed. The experiment results are obtained with an external clock of 50MHz internally multiplied to 188MHz by PLL, which means the counter clock frequency is 188MHz. A total of 290 LEs are used, and the resource usage is 5%. Here, the assessment metrics such as path

delay, output duty cycle, area, power and time resolution are analyzed. Then the proposed HRDPWM-RSSC-PSC design is analyzed and it was compared with the existing methods like high resolution DPWM depending on synchronous phase-shifted circuit and delay line (HybDPWM-SPSE-DL) Delay-Line DPWM Architecture with Compensation Module and Delay-Adjustable Unit depending on Delay Line (Hyb DPWM-DLP) respectively.

Table 1: Performance Analysis

Performance metrics	**Hyb DPWM-SPSE-DL**	**Hyb DPWM-DLP**	**HRDPWM-RSSC-PSC (Proposed)**
Path Delay	1.017	0.97	0.323
Area(mm^2)	0.077	0.059	0.0073
Output Duty Cycle	0.78	0.76	0.99
Time Resolution (ps)	600	90	40.1
Pulse width	115	120	136
Power (mW)	20.94	29.45	0.213

Table 1 shows the performance analysis of path delay, Area, output duty cycle, time resolution, pulse width, power, Frequency.

Here the performance of path delay of the existing design such as Hyb DPWM-SPSE-DL, Hyb DPWM-DLP design is found to be an ineffective one for designing synchronous counter with lower path delay. In addition, the existing Hyb DPWM-SPSE-DL design has offered moderate performance of path delay over the earlier model namely existing Hyb DPWM-DLP design. However, the proposed HRDPWM-RSSC-PSC design has outperformed existing design by offering a lower path delay. For instance, the existing Hyb DPWM-SPSE-DL design has attained a higher path delay 1.017, whereas slightly lower path delay value of 0.97 has been offered by existing Hyb DPWM-DLP design. But, the proposed HRDPWM-

RSSC-PSC model has exhibited superior outcome with the lower path delay value is 0.323. The proposed HRDPWM-RSSC-PSC design provides 53.09%, 34.86% lower path delay compared with existing designs like Hyb DPWM-SPSE-DL, Hyb DPWM-DLP respectively.

Here the performance of Area of the existing design such as Hyb DPWM-SPSE-DL, Hyb DPWM-DLP design is found to be an ineffective one for designing synchronous counter with lower Area. In addition, the existing Hyb DPWM-SPSE-DL design has offered moderate performance of Area over the earlier model namely existing Hyb DPWM-DLP design. However, the proposed HRDPWM-RSSC-PSC design has outperformed existing design by offering a lower Area. For instance, the existing Hyb DPWM-SPSE-DL design has attained a higher Area 0.077, whereas slightly lower Area value of 0.059 has been offered by existing Hyb DPWM-DLP design. But, the proposed HRDPWM-RSSC-PSC model has exhibited superior outcome with the lower Area value is 0.0073. The proposed HRDPWM-RSSC-PSC design provides 13.82%, 25.93% lower Area compared with existing designs like Hyb DPWM-SPSE-DL, Hyb DPWM-DLP respectively.

Here the performance of Output Duty Cycle of the existing design such as Hyb DPWM-SPSE-DL, Hyb DPWM-DLP design is found to be an ineffective one for designing synchronous counter with lower Output Duty Cycle. In addition, the existing Hyb DPWM-SPSE-DL design has offered moderate performance of Output Duty Cycle over the earlier model namely existing Hyb DPWM-DLP design. However, the proposed HRDPWM-RSSC-PSC design has outperformed existing design by offering a lower Output Duty Cycle. For instance, the existing Hyb DPWM-SPSE-DL design has attained a higher Output Duty Cycle 0.78, whereas slightly lower Output Duty Cycle value of 0.76 has been offered by existing Hyb DPWM-DLP design. But, the proposed HRDPWM-RSSC-PSC model has exhibited superior outcome with the lower Output Duty Cycle value is 0.99. The proposed HRDPWM-

RSSC-PSC design provides 23.43%, 32.09% lower Output Duty Cycle compared with existing designs like Hyb DPWM-SPSE-DL, Hyb DPWM-DLP respectively.

Here the performance of Time Resolution of the existing design such as Hyb DPWM-SPSE-DL, Hyb DPWM-DLP design is found to be an ineffective one for designing synchronous counter with lower Time Resolution. In addition, the existing Hyb DPWM-SPSE-DL design has offered moderate performance of Time Resolution over the earlier model namely existing Hyb DPWM-DLP design. However, the proposed HRDPWM-RSSC-PSC design has outperformed existing design by offering a lower Time Resolution. For instance, the existing Hyb DPWM-SPSE-DL design has attained a higher Time Resolution 600, whereas slightly lower Time Resolution value of 90 has been offered by existing Hyb DPWM-DLP design. But, the proposed HRDPWM-RSSC-PSC model has exhibited superior outcome with the lower Time Resolution value is 40.1. The proposed HRDPWM-RSSC-PSC design provides 32.87%, 26.87% lower Time Resolution compared with existing designs like Hyb DPWM-SPSE-DL, Hyb DPWM-DLP respectively.

Here the performance of power of the existing design such as Hyb DPWM-SPSE-DL, Hyb DPWM-DLP design is found to be an ineffective one for designing synchronous counter with lower power. In addition, the existing Hyb DPWM-SPSE-DL design has offered moderate performance of power over the earlier model namely existing Hyb DPWM-DLP design. However, the proposed HRDPWM-RSSC-PSC design has outperformed existing design by offering a lower power. For instance, the existing Hyb DPWM-SPSE-DL design has attained a higher power 20.93, whereas slightly lower power value of 29.45 has been offered by existing Hyb DPWM-DLP design. But, the proposed HRDPWM-RSSC-PSC model has exhibited superior outcome with the lower power value is 0.213. The proposed HRDPWM-RSSC-PSC design provides 24.85%, 27.93% lower power compared with

existing designs like Hyb DPWM-SPSE-DL, Hyb DPWM-DLP respectively. From the above table the proposed method reduces the critical path delay with higher linearity.

5. Conclusion

Nowadays, the DC-DC converter digital control is more attracted due to its benefits, like programmability, enhanced control algorithms. The coding is done in Verilog and the proposed synchronous counter design has been synthesized using Xilinx ISE. Here, the assessment metrics, such as path delay, linearity, output duty cycle and time resolution are analyzed. The performance of the proposed SCD-MCT-MCF design shows lower path delay 24.94%, 28.94%, is compared with the existing design such as high resolution DPWM depending on synchronous phase-shifted circuit and delay line (Hyb DPWM-SPSE-DL), Delay-Line DPWM Architecture with Compensation Module and Delay-Adjustable Unit depending on Delay Line (Hyb DPWM-DLP) respectively.

Compliance with Ethical Standards

Data availability statement

Data sharing is not applicable to this article as no new data were created or analyzed in this study.

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This article does not contain any studies with human participants performed by any of the authors.

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