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Development of Cryogenic Readout Electronics for Far-Infrared Astronomical Focal Plane Array

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SUMMARY We have been developing low power cryogenic readout electronics for space borne large format far-infrared image sensors. As the circuit elements, a fully-depleted-silicon-on-insulator (FD-SOI) CMOS process was adopted because they keep good static performance even at 4.2 K where where various anomalous behaviors are seen for other types of CMOS transistors. We have designed and fabricated several test circuits with the FD-SOI CMOS process and confirmed that an operational amplifier successfully works with an open loop gain over 1000 and with a power consumption around 1.3 μW as designed, and the basic digital circuits worked well. These results prove that the FD-SOI CMOS process is a promising candidate of the ideal cryogenic readout electronics for far-infrared astronomical focal plane array sensors.

key words: *far-infrared astronomy, cryogenic readout electronics, charge amplifier, VLSI, FD-SOI-CMOS*

1. Introduction

In far-infrared (FIR) observations, obscuration of Earth's atmosphere and thermal emission from the telescope itself are major problems. To overcome these obstacles, employing a cooled satellite telescope is desirable to conduct astronomical observation, but these technical difficulties have made FIR observations from space satellite possible only since early 1980's. Early infrared astronomical space telescopes [1]–[4] have carried out astronomical observations with single or small pixel array sensors and successfully discovered many interesting astronomical objects such as dust obscured starburst galaxies. Naturally, these successes have led to a requirement of a larger format 2-dimensional FIR sensor in order to carry out wide-field observations with a high spatial resolution.

Development of cryogenic readout electronics is one of the major issues to realize such a large formant FIR sensor. Astronomical FIR sensors such as Ge:Ga photoconductor are worked lower than 4.2 Kelvin (K), where their impedances are very high. Therefore, the preamplifiers should be placed in the very vicinity of these detectors in order to suppress the electromagnetic interference, microphonic noise and crosstalk. Because of the limited cooling power of the satellite to its focal plane, efficient multiplexing readout functions of the ROICs (readout integrated circuits) are also imperative to minimize the heat load due to wiring on the detector stage. So far, the trans-impedance amplifier (TIA), which consist of a discrete Si-JFET near the sensor and an operational amplifier (OP-amp) placed on the ambient temperature stage, have often been used for the FIR sensors. However, this type of TIA is not suitable for large formant FIR sensors, not only because it will require many wiring between the JFETs and Op-amps, but also because each Si-JFET should be warmed to around 100 K near the sensors, which accordingly produce large power consumption at the cold stage. It is currently the best solution to employ low noise and low-power cryogenic ROICs that can work around the optimum temperature of the FIR sensors.

However, the technology of such cryogenic ROICs has not established yet, mainly because FIR sensor technologies have had little demand except for a small amount of scientific applications. One of the difficulties in developing cryogenic ROICs is that the very low temperature operation limits the choice of semiconductor devices. For example, silicon-JFETs and silicon bipolar transistors do not work below 4.2 K due to the carrier freeze-out effect. Some compound semiconductor devices like n-type GaAs-FETs and HEMTs (e.g., [5]–[7]) have been reported to keep good characteristics even below 4.2 K, but p-type ones are not available. Actually, the silicon CMOS is the most possible candidate for large scale cryogenic ROICs because it has a great advantage that VLSI technology established for commercial use is available.

However, widely used bulk silicon CMOSs often suffer from anomalous current-voltage characteristics like the kink phenomena below 4.2 K, which makes it difficult to design reliable CMOS circuits [8]. There have been some studies to overcome the cryogenic anomaly of bulk silicon CMOSs. Young et al. [9] developed cryogenic ROICs by using the special wafer which has very thin lightly doped epitaxial layer over degenerate substrate. Merken et al. [10] overcame the problem and developed digital and analog circuits based on the modeling of cryogenic behavior, and on optimized circuit design and layout techniques. In Japan, the BiCMOS process was examined by the infrared astronomy group of Nagoya University, and it was found that only

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PMOS can keep good performance even at 1.8 K [11], [12]. This process was successfully applied (only with PMOS) for the FIR image sensors of the infrared astronomical satellite, AKARI [13]–[16]. Based on their recent achievements, a larger format FIR array sensor for the following infrared satellite mission, SPICA, has been being studied in collaboration between JAXA and IMEC [17].

On the other hand, we focus on the fully-depleted silicon on insulator (FD-SOI) CMOS [18], because the FD-SOI-CMOSs are considered to be immune to anomalous effects like kink phenomena in a condition of ambient temperature. If it is the case also below 4.2 K, we may be able to develop sophisticated cryogenic circuits without special optimizations needed for bulk-CMOSs. However, as far as we know, many of the studies on the cryogenic characteristics have been devoted to partially depleted SOI CMOSs (e.g. [19]), not to FD-SOI ones. The characteristics in the subthreshold region, where the cryogenic ROICs must be operated for low power consumption, have so far been unknown. We adopted the FD-SOI-CMOS process manufactured by OKI-semiconductor Co. Ltd., and evaluated the static characteristics for several samples at 4.2 K. The results showed that the FD-SOI-CMOSs with a source-tie or a body-tie kept relatively good performance even at 4.2 K [20].

In this paper, we report the recent progress on the development of cryogenic ROICs based on the FD-SOI-CMOS process. The description of test devices is given in Sect. 2. The cryogenic characteristics of the FD-SOI-CMOSs are presented in Sect. 3. Measurement results of the basic circuit components are shown in Sect. 4. The discussion is presented in Sect. 5.

2. Description of the Test Chips

Simple LSI circuits and basic elements were manufactured in 0.2 μm FD-SOI-CMOS process by OKI semiconductor in 2008 and 2009. Besides the normal type design of the FD-SOI-CMOS, there are source-tied and body-tied designs in the CMOS process. While the body of the normal type FD-SOI-CMOS is not directly connected with the drain or source terminals, that of source-tied one is electrically connected to the source terminal, and the body-tied one has a body terminal to control the body potential. Though both the source-tied and body-tied FD-SOI-CMOSs showed good performance at 4.2 K in the previous measurement [20], all the circuits consist of source-tied FD-SOI-CMOSs because of their simplicity in designing. Table 1 displays a summary of the manufactured circuits. Basic analog circuits like operational amplifier and capacitive transimpedance amplifiers (CTIAs) have been fabricated in 2008. On the other hand, in 2009, we have complementarily fabricated fundamental digital circuits (such as NAND or Flip-Flops) and 8 bit-successive approximation register (SAR) type A-D converter consisting of various digital and analog circuits. Figure 1 shows a chip photograph of the experimental production in 2008, whose chip size is 2.5 × 2.5 mm^2. We note that any FET model for applications below 4.2 K has not been established yet unlike development of custom LSIs at an ambient temperature. It is currently difficult to design sophisticated cryogenic circuits only with a circuit simulator. Therefore, we fabricated basic circuits components as the building blocks of the cryogenic ROICs at first in order to verify the dynamic characteristics at 4.2 K.

Table 1 Summary of the experimental productions.

Analog (2008)	Digital (2009)
Operational amplifiers	Basic logic components (e.g., NAND, INV, FF)
Single ended amplifiers	8 bit SAR ADC
DC-coupled CTIA	(DA converter, Registers)
AC-coupled CTIA	S&H, Multiplexer, and CTIA
Basic circuit elements	Basic circuit elements (FETs)
(R, C, FETs)	Other test circuits

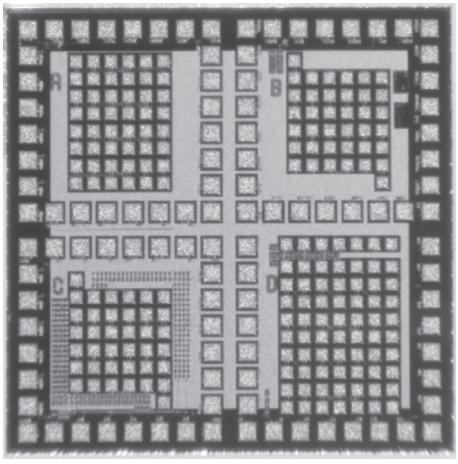

Fig. 1 Photograph of the manufactured cryogenic circuits "Analog" in 2008 [20]. The chip size is 2.5 × 2.5 mm^2. External large pads are connected to the test analog circuits and the basic circuits elements are fabricated around inner small pads.

3. Performance of Single FD-SOI-CMOSs at Cryogenic Temperatures

3.1 Static Performance

We evaluated source-tied FD-SOI-CMOSs in 0.2 μm process. The measured FETs are fabricated on the "Analog" chip in 2008. In order to measure the performance at 4.2 K, each "Analog" chip was mounted into a 48-pin ceramic dip package and wire bonded. The package was mechanically-fixed on a copper sample holder which was mounted on the copper cold stage of 8-inch liquid helium cryostat, and then was cooled down to a liquid nitrogen temperature (77 K) or a liquid helium temperature (4.2 K). We measured static characteristics of the FD-SOI-CMOSs at a room temperature (RT = 293 K), 77 K, and 4.2 K by using Agilent HP 4156C Semiconductor Parameter Analyzer. Most of the cryogenic circuits on "Analog" chip are designed using the source-tied FD-SOI-CMOSs with a gate length of 5 μm, which showed a good performance in the several test sam-

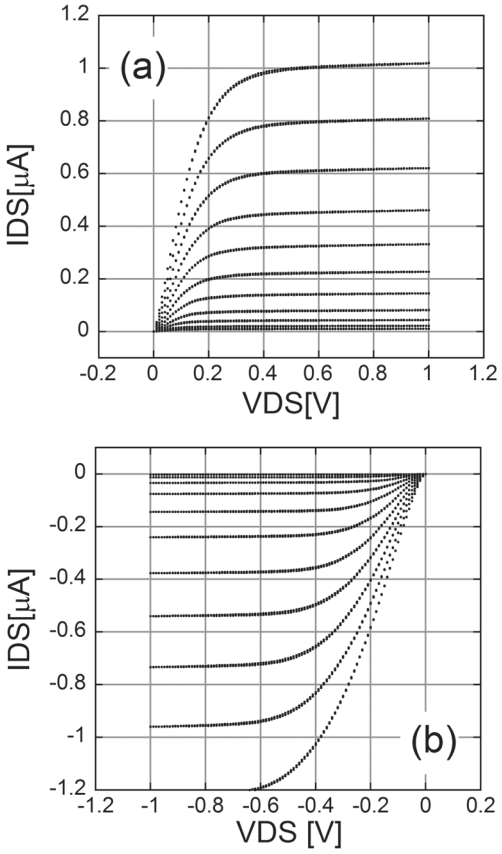

Fig. 2 I-V characteristics of FD-SOI-CMOS (source tied type) at 4.2 K for W(μm)/L(μm) = 0.63/5.0. (a) NMOSFET and (b) PMOSFET. VGS (from 1.05 to 1.23 V with 0.023 V) was given for the NMOS and VGS (−1.15 to −1.55 V in step of −0.04 V) was given for the PMOS. Forward and reverse sweep data of VDS were continuously measured to find hysteresis effects on the I-V curves.

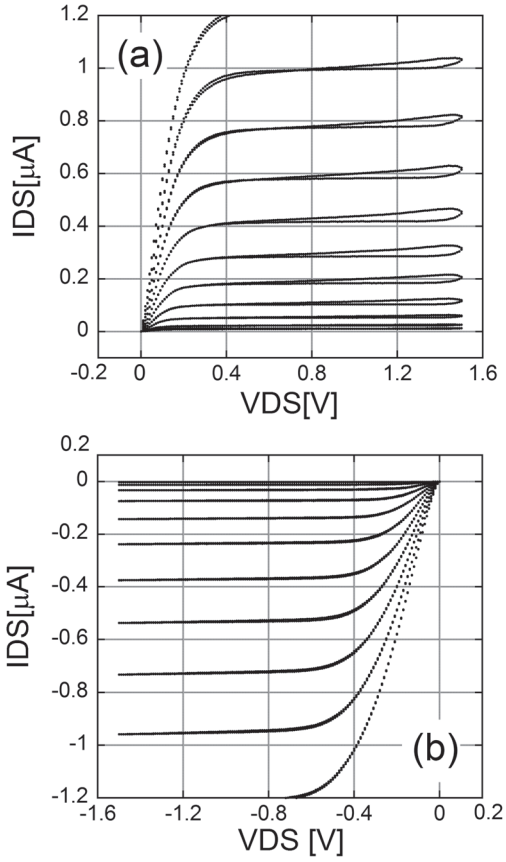

Fig. 3 I-V characteristics of the NMOS (a) and the PMOS (b) at 4.2 K for the same gate size as in Fig. 2, but |VDS| was swept between 0 and 1.5 V in the same way as in Fig. 2. The drain breakdown phenomena are seen around VDS = 1.4 V for the NMOS.

ples [20]. Here, we report on the measurement results for ones with that gate length. Panels (a) and (b) in Fig. 2 show examples of current-voltage (I-V) characteristics in the subthreshold region for the source-tied FD-SOI-CMOSs whose gate sizes are W(μm)/L(μm) = 0.63/5.0. Even at 4.2 K, no remarkable anomaly are observed on the I-V curves for $\left|\text{(drain − source voltage (VDS)}\right| \leq 1$ V except for the following weak one. The drain resistance becomes slightly larger near |VDS| = 0 especially for the PMOSs. This phenomena is due to the carrier freeze-out effect in lightly doped region near the drain [22]. On the other hand, the drain breakdown occurred at VDS = 1.4∼1.5 V for some of the measured NMOSs (Fig. 3) at 77 K and 4.2 K, but the PMOSs did not suffer from the phenomenon for below |VDS| of 1.5 V in the temperature range because of the larger effective mass of the holes.

Figure 4 shows typical IDS-VGS (gate-source voltage) characteristics. When the temperature decreases from RT to 4.2 K, |VGSs| at |IDS| = 0.1 μA increase by 90 mV and 290 mV for the NMOS and the PMOS. Table 2 shows small signal characteristics of the FD-SOI-CMOSs. The transconductance, g_{m}, increase as the operating temperature decrease. The g_{m} of SOI-NMOS is similar to twice of that of PMOS for these temperatures. The drain to source current in a condition where |VGS| is much less than the threshold voltage (off-state IDS) is an another important parameter especially for charge integration amplifiers. The off-state IDSs in Fig. 4, which are limited by the measurement system, are upper limits. Further measurements (for example, by using on-chip integrators) are needed to obtain this parameter.

3.2 Noise Performance

We measured the noise spectrum in the low frequency region at 4.2 K for the source tied FD-SOI-CMOSs with a gate size of W(μm)/L(μm) = 0.63/5.0. Figure 5 shows the measurement circuit. All measurements were carried out under the condition where drain breakdown phenomena did not occur. The applied voltages are 1.0 V, and 0.1 V for |VD| and |VS| in Fig. 5. The output voltage of the source follower was set to be ∼ 0 V (|IDS| of the measured FET was then biased to be 0.1 μA) by tuning |VG|, around whose condition analog circuits in the cryogenic ROICs will be operated. The output voltage was acquired by an FFT analyzer (ONOSOKKI CF-7200). In order to obtain the input referred noise voltages, the acquired output voltages were divided by the total

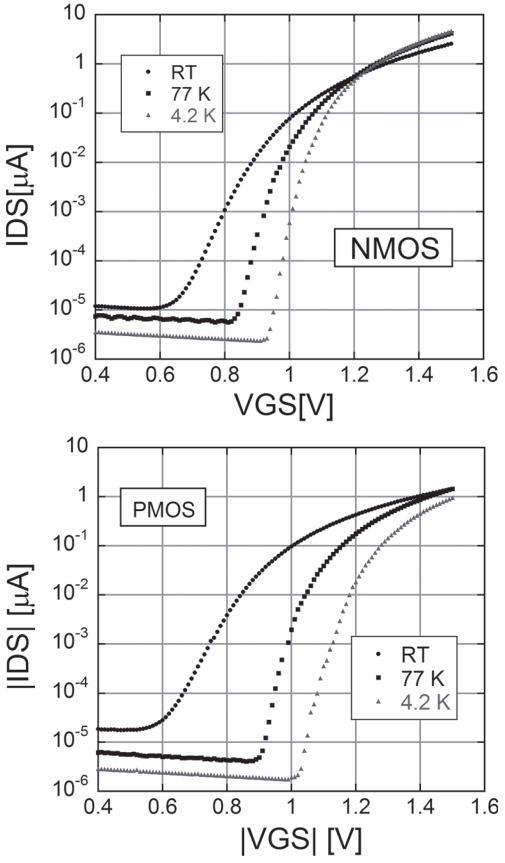

Fig. 4 Typical IDS-VGS (gate-source voltage) characteristics of the FD-SOI-CMOS at temperatures of RT, 77 K, and 4.2 K. The upper and lower panels show the plots for NMOS and PMOS, respectively.

Table 2 Small signal parameters on the FD-SOI-CMOSs with W(μm)/L(μm) = 0.63/5.0 in the saturation region (|VDS| ~ 1 V and |IDS| ~ 0.1 μA).

Temperature	NMOS		PMOS	
(K)	g_m (μS)	r_d (Ω)	g_m (μS)	r_d (Ω)
RT	1.3	> 100 MΩ	1.1	> 100 MΩ
77	2.0	> 100 MΩ	1.6	> 100 MΩ
4.2	3.0	> 100 MΩ	1.8	> 100 MΩ

gain measured prior to the noise measurements. The total gain is the product of the source follower gain (0.72 for the NMOS source follower and 0.63 for the PMOS one) and the gain of 110 for the subsequent amplifiers on the RT stage. Figure 6 shows the noise spectrum for one of the source tied FD-SOI-CMOSs. The noise spectrum densities at 1 Hz and at |IDS| = 0.1 μA are 7–10 μV/ $\sqrt{\text{Hz}}$ for both the PMOS and the NMOS. The discrete fluctuation on the output voltage was sometimes observed in time domain. It means the RTS (Random Telegraph Signals) noise sometimes occurred in the low frequency region as a dominant noise component. We did not measure the performance above 1 kHz due to the limitation of the frequency response on the measurement system. Instead, we estimated the input referred channel thermal noise, 8 kT/3 g_m, from the static characteristics of the FETs. In reference to Table 2, the noise floors are calculated to be 7 nV/ $\sqrt{\text{Hz}}$ for the NMOS and 9 nV/ $\sqrt{\text{Hz}}$ for the PMOS, respectively. Next, we show the result of the same configuration except that the bias current is 1 μA. The RTS noises on the low frequency spectra was not remarkable for the PMOSs and the noise levels decreased by approximately a factor of two. On the other hand, the noise levels did not show a clear dependence on the bias current for the NMOSs, because the low frequency noises were sometimes remarkable at IDSs of 0.5 μA or 1.0 μA due to the large RTS noises. We have not fully understood the RTS noise performance in this process yet. Therefore, further studies on the reduction method as well as on the noise performance are needed in order to realize an FIR preamplifier achieving a background limited performance.

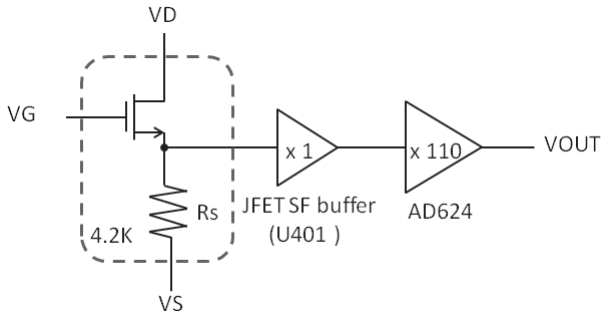

Fig. 5 Noise measurement circuit. The measured source follower amplifier consists of FD-SOI-CMOS and source follower resistor of 1 MΩ, which were placed on the 4.2 K stage. The output of the source follower was amplified by a low noise silicon JFET source follower buffer and then by an instrumentation amplifier. The measured total gain by the following two amplifiers on the RT stage, was, 110. The output signal was observed with an FFT analyzer.

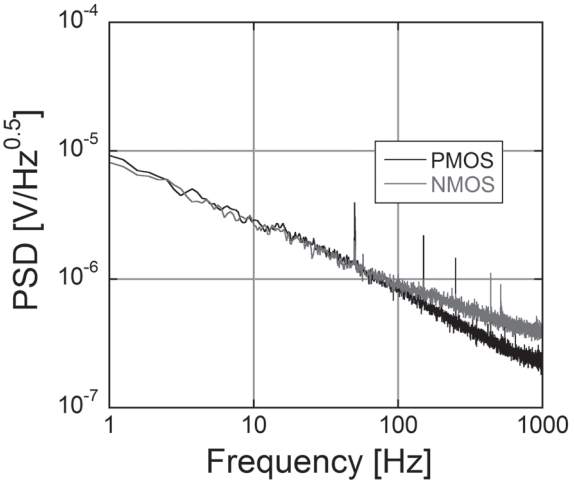

Fig. 6 Input referred noise spectra of the source-tied FD-SOI-CMOSs at 4.2 K. The gate size is W(μm)/L(μm) = 0.63/5.0. These noise spectra were measured in the configuration of Fig. 5. The bias current was |0.1| μA for the drain-source voltage of |1 V|. In these measurements, the output voltages of the source follower amplifier were set to be approximately 0 V by turning |VGS|. For the NMOS and the PMOS, the supplied VGs were 1.18 V and −1.23 V and the source follower gains (measured at 10 Hz) were 0.72 and 0.63. The sharp peaks are due to the electrical interference in the laboratory environment.

4. Measurement Results on Fundamental Circuits

4.1 Operational Amplifier

We evaluated the basic performance of the cryogenic operational amplifier on the test chip shown in Fig. 1. A two-stage cascode operational amplifier with PMOS input is shown in Fig. 7. This amplifier is composed of the source tied FD-SOI-CMOSs with a gate length of 5 μm. The source follower amplifier on the second stage is designed to convert a high impedance at the output node of the cascode amplifier on the first stage to a lower value. A non-inverting amplifier by the operational amplifier was fabricated to obtain an open-loop gain and noise spectrum (Fig. 8). An optimum set of bias voltages (VDD = 2.0 V, VCL = 0.8 V, VCA = −1.4 V, VSS = −2.9 V, VSFB = −1.5 V) was supplied to the amplifier. Then, the input referred offset voltage was 2.5 mV, and the power dissipation of the amplifier was 1.3 μW. A 11 Hz sine wave signal with a dc bias generated from a function generator (Wavefactory WF 1934A) was applied to the input node of the cryogenic amplifier as shown in Fig. 8. The output voltage was acquired by the same FFT analyzer as in the previous section. The maximum voltage swing of the amplifier was 1 V for the given condition. The upper panel of Fig. 9 shows the input and output signals of the non-inverting amplifier. The closed loop gain, CLG, of the amplifier was 99.6. The open-loop gain, A, is calculated from the closed-loop gain, using the Eq. (1). R_f and R_{in} are 1 MΩ and 100 kΩ respectively as give in Fig. 7.

$$A = \frac{\left(1 + R_f/R_{in}\right) \cdot CLG}{\left(1 + R_f/R_{in}\right) - CLG} \quad (1)$$

The open loop gain is estimated to be more than 7000. This value is consistent with the total gain of > 1000 calculated from the static characteristics of all elements. Subsequently, the frequency response of the non-inverting amplifier was measured. The frequency response was well fitted by a first-order low-pass filter model with a cut-off frequency of 4 kHz. This cut-off frequency is only a lower limit value of the frequency response of the amplifier, because the stray capacitance caused by wiring (from output node at 4.2 K stage to the buffer at room temperature stage) limited the performance in the configuration of Fig. 8. Consequently, these results show that this operational amplifier adequately works even at 4.2 K.

The noise spectrum of the amplifier was obtained using the same configuration as shown in Fig. 8. Instead of sine wave, attenuated dc bias voltage was only given to the positive input, VIN+. The input referred voltage noise was derived from the output noise signal divided by the measured closed loop gain. Figure 10 shows a spectrum of the input referred voltage noise on the cryogenic operational amplifier and it was obtained at 4.2 K. The noise voltage at 1 Hz was 19 μV/ $\sqrt{\text{Hz}}$. Each FET which contributed to the voltage noise of the cryogenic amplifier was then biased at |IDS| of

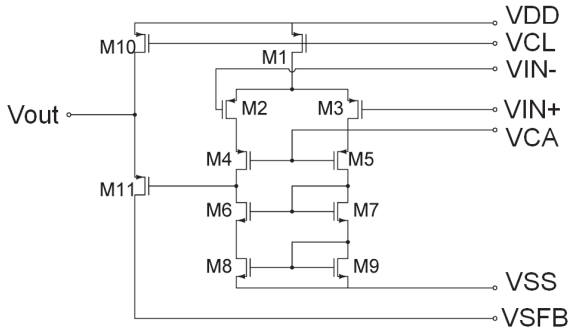

Fig. 7 Schematic diagram of the cryogenic operational amplifier. This circuit is composed of the source tied FD-SOI-CMOSs with a gate size of W(μm)/L(μm) = 0.63/5.0 except for M2 and M3 whose gate sizes are W(μm)/L(μm) = 5/5.

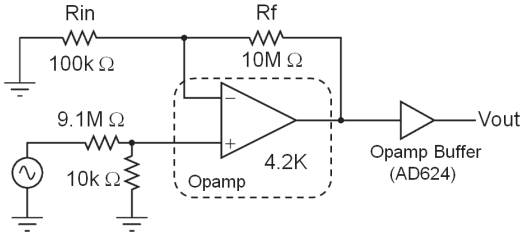

Fig. 8 Test configuration of the cryogenic amplifier. The test chip was installed into a liquid helium cryostat. The output signal was buffered by a low noise instrument amplifier.

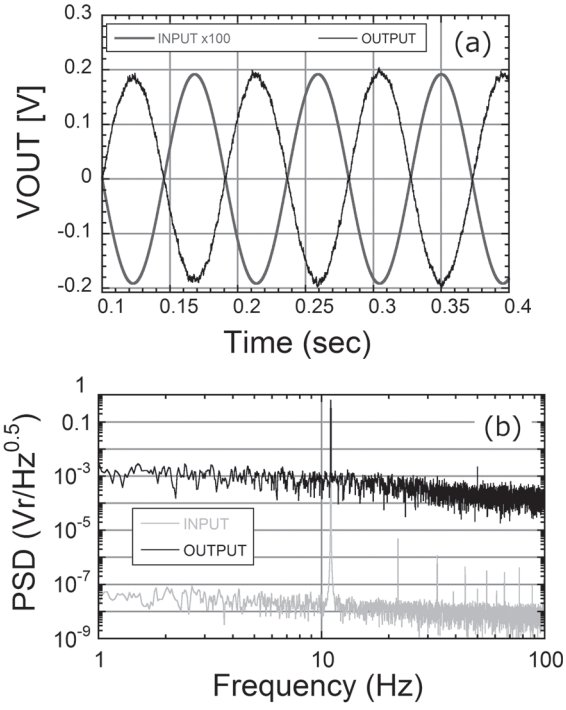

Fig. 9 Example of the input and output signal in Fig. 8. The upper figure shows the time waveforms with a ac-coupling mode (Fig. 9a). The input signal was magnified a hundred times. On the other hand, in the lower figure (Fig. 9b) the power spectra were shown. The attenuations of these signals by the ac-coupling mode are negligible in this case.

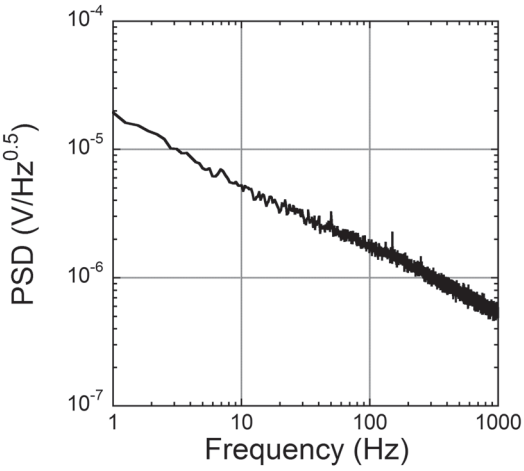

Fig. 10 Input referred noise of the cryogenic operational amplifier at 4.2 K.

Table 3 Summary of the performance measurement on the cryogenic amplifier.

Parameters	result
Operating temperature	4.2 K
open loop gain	7000
Voltage swing	1 V
Input referred noise voltage at 1 Hz	$19\,\mu\mathrm{V}/\sqrt{\mathrm{Hz}}$
Power consumption	$1.3\,\mu$W
Input referred offset voltage	2.5 mV
Gain-bandwidth product	> 0.4 MHz

0.1 μA. Assuming that the input referred noise of each FET composing the cryogenic operational amplifier is inversely proportional to the square root of the gate area at 4.2 K, the input referred noise of the amplifier, $v_{n,opamp}$, is given as follows [23],

$$v_{n,opamp} \approx \sqrt{2v^2_{\mathrm{n,\ W/L=0.63/5}} + \frac{2v^2_{\mathrm{n,\ W/L=0.63/5}}}{(5/0.63)}}, \qquad (2)$$

where $v_{\mathrm{n,\ W/L=0.63/5}}$ is the noise of a single FET whose gate size of W(μm)/L(μm) = 0.63/5.0. Considering that the input referred noise of a single FET is 7–10 $\mu\mathrm{V}/\sqrt{\mathrm{Hz}}$ at 1 Hz for the |IDS| of 0.1 μA, $v_{n,opamp}$ is estimated to be 11–15 $\mu\mathrm{V}/\sqrt{\mathrm{Hz}}$ at 1 Hz. The measured noise is slightly higher than the expected one. If the assumption is correct, the input referred noises of the FETs composing the amplifier may be higher than those of single FETs described in Sect. 3.2. Further studies on the variation and on the gate area dependency of the noise performance are needed to compare the amplifier design with measurement results. Here, we note that the total thermal noise generated by resistors, R_{in}, R_{f} in Fig. 8 is $40\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ as an input referred value. The noise components are, therefore, negligible in these measurements. The performance of the cryogenic operational amplifier described in this section is summarized on Table 3.

4.2 Basic Digital Circuits

We measured the basic digital circuits fabricated on the other chip "Digital" in Table 1. These digital circuits are designed with the source-tied FD-SOI-CMOSs whose gate sizes are W(μm)/L(μm) = 1.0/5.0 for the NMOS and 1.9/5.0 for the PMOS, respectively. The supply voltage is set to be 2 V. Open IPs [24] were used to design these digital circuits. The test chip was cooled down to 4.2 K and operated in low frequencies to check the performance there. Clock and logic signals were acquired by the Keyence date recorder (GR-7000). Figure 11 shows a circuit diagram of NAND. Logic signals with 43 Hz and 83 Hz were fed to the IN_A and IN_B nodes. As the test result shows in Fig. 12, the NAND worked correctly for the supply voltage of 2 V. Furthermore, we evaluated a D-Flip Flop with Enable input (EDFF) consisting of NANDs, inverters, and some other digital components (See the p.57 in [24]). Figure 13 shows the test result on the EDFF for the enable signal of true, when the clock and input logic signal (D-INPUT) frequencies were 210 Hz and 73 Hz. The result shows that the output signal (Q-OUTPUT) takes the state of D-INPUT at a positive edge of the clock (CLK) and keep it for one clock cycle. On the other hand, Q-OUTPUT hold the LOW state when the

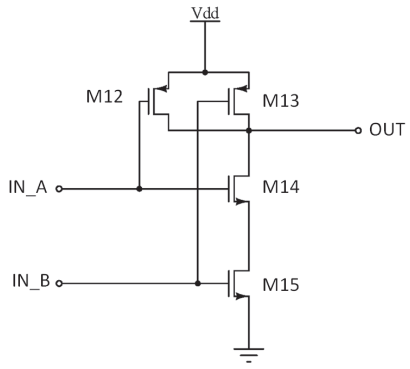

Fig. 11 Schematic diagram of NAND. The basic digital circuits are composed of the source tied FD-SOI-PMOSs with a gate size of W(μm)/L(μm) = 1.9/5.0 and the NMOSs with W(μm)/L(μm) = 1.0/5.0.

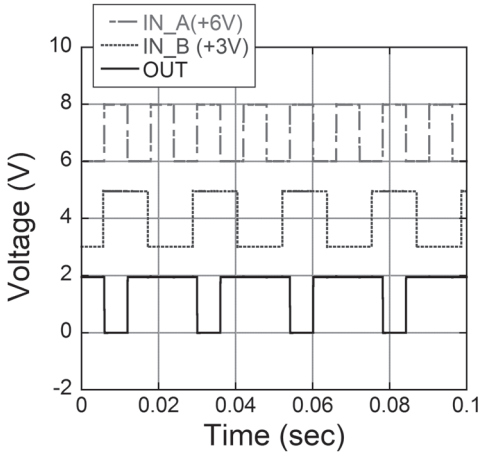

Fig. 12 Measurement result of the NAND at 4.2 K. Input logic signals are plotted with offsets in this graph in order to show these logic signals separately.

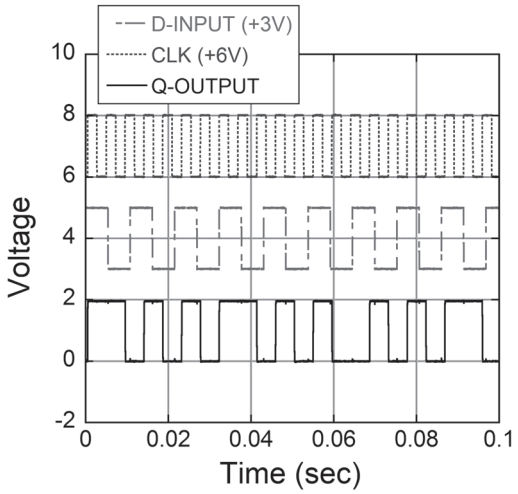

Fig. 13 Measurement result of a D-Flip Flop with Enable input (EDFF) at 4.2 K. Input logic signal (D-INPUT) and clock (CLK) are plotted with offsets in this graph. Q-OUTPUT means the output signal.

enable signal was false. The EDFF worked reasonably at 4.2 K. Consequently, the designed basic digital circuits can work at 4.2 K as designed at least in low frequency region.

We also measured the delay times, τ_{LH} and τ_{HL}, from the rising and falling edges of the measurements in Fig. 13. τ_{LH} (τ_{HL}) is defined as the time between the midpoint of the falling (rising) edge of the clock and that of the rising (falling) edge of the following Q-OUTPUT. In this measurement, τ_{LH} and τ_{HL} are 17 μs and 23 μs, respectively. The reason why τ_{LH} is shorter than τ_{HL} is possibly because the NMOS in the EDFF had a higher driving capability than the PMOS. Therefore, the higher frequency limit of the EDFF, $1/(\tau_{LH} + \tau_{HL})$, is 25 kHz. This result is a lower limit value, because the frequency responses of these digital circuits were limited by the output load capacitance caused by the wiring as described in Sect. 4.1.

5. Discussion

We measured the cryogenic performance of the FD-SOI-CMOSs in the sub-threshold region. They keep good static characteristics between RT and 4.2 K. According to [20], the static and noise performances of the FD-SOI-CMOS produced by OKI semiconductor did not change between 4.2 K and 2 K. Therefore we expect that the ROIC based on the process can work at 2 K where infrared sensors should be operated. In reference to [20], we can expect that the read noise of a proper designed preamplifier employing the FD-SOI-CMOSs will achieve a background limited performance when a Ge:Ga photoconductor is operated under a typical background condition. Therefore, the FD-SOI-CMOS is an emerging candidate as a basic component of cryogenic preamplifier for FIR image sensors. Combination with Ge Blocked Impurity Band (BIB) detectors that is recently emerging with surface-activated wafer bonding (SAB) technology and molecular beam epitaxy (MBE) technology are urgent targets [25]–[27]. The FD-SOI-CMOS has another merit that the temperature variation on the threshold voltage is relatively small, compared with bulk CMOSs [22]. For example, the variations on |VGS| at |IDS| of 0.1 μA for the FD-SOI-CMOS were 90 mV for the NMOS and 290 mV for the PMOS, while that of a bulk PMOS was $\sim$ 600 mV [28]. This characteristic will help us to develop VLSIs that can be operated over a very wide temperature range (from 300 K to 4.2 K) without tuning bias voltages. Furthermore, FD-SOI-CMOS devices have resistance characteristics against high energy particle radiation. Hirose et al. [29], [30] have shown that 128-Kbit SRAMs using a rad-hard circuit design in a 0.2 μm FD-SOI-CMOS process have high tolerance for Single Event Latch up, Single Event Upset, and Total Ionizing Dose. Low power VLSI with high tolerance for temperature variation and high energy particle radiation should be useful for various scientific field including space explorations or astronomy.

Based on the above mentioned CMOS characteristics, we first developed cryogenic operational amplifier in the FD-SOI-CMOS process, which means that various analog circuits can be developed with this process. The cryogenic operational amplifier itself, of course, can be used for versatile applications like preamplifiers, switched capacitors for S&H circuits, and Wilkinson ADCs. The basic digital circuits as complicated as EDFF also operated correctly at least in the low frequency region for the supply voltage of 2 V. These results will lead us to sophisticated circuits consisting of analog and digital components without special optimizations.

Some unevaluated parameters still remain. The gate leakage and the off-state drain-source currents of the FD-SOI-CMOS are critical parameters to operate very high impedance detectors like BIB type ones. Moreover, measurement on the noise performance under a high impedance configuration should be needed because some kind of noise like dielectric polarization noise appears in such a configuration [31]. Thus, these parameters should be obtained to estimate the practical performance of the cryogenic integrated circuits.

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