

Techniques of Reducing Switching Artifacts in Chopper Amplifiers

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SUMMARY Chopping technique up-modulates amplifier's offset and low-frequency noise up to its switching frequency, and therefore can achieve low offset and low temperature drift. On the other hand, it generates unwanted AC and DC errors due to its switching artifacts such as up-modulated ripple and glitches. This paper summarizes various circuit techniques of reducing such switching artifacts, and then discusses the advantages and disadvantages of each technique. The comparison shows that newer designs with advanced circuit techniques can achieve lower DC and AC errors with higher chopping frequency.

key words: amplifier, chopping, switching artifact, charge injection

1. Introduction

Chopping is a circuit technique that involves up-modulating amplifier offset and low frequency noise to higher frequencies, and which therefore can achieve microvolt-level offset with very low temperature drift [1]. On the other hand, it causes switching artifacts such as AC ripple and glitches at the amplifier's output, which usually need to be attenuated by low-pass filtering, thus decreasing the usable signal bandwidth [2]. This paper introduces advanced circuit techniques to reduce such switching artifacts over the past years as well as their advantages and disadvantages.

1.1 Principle of Chopping and Up-Modulated Ripple

Figure 1 (a) shows a circuit diagram of a chopper operational amplifier (op-amp) in a closed-loop. The chopper op-amp consists of an input chopper CH_{IN} , an input transconductor G_{m1} with its undesired offset V_{os1} , an output chopper CH_{OUT} , and an output transconductor G_{m2} . The choppers CH_{IN} and CH_{OUT} perform the modulation by two phase clocks Φ_{CH} and Φ_{CHINV} operating at a chopping frequency f_{CH} as shown in a timing diagram Fig. 1 (b). Provided that f_{CH} is well below the closed-loop bandwidth around the op-amp, the amplitude of up-modulated ripple $V_{out,rip}$ is given by:

$$V_{out,rip} = A_{CL} V_{os1} \quad (1)$$

$$A_{CL} = (1 + R_F/R_G), \quad (2)$$

where A_{CL} is the closed-loop gain determined by external resistors R_G and R_F .

1.2 Glitches

In addition to the ripple, charge injections of input chopper switches introduce glitches as shown in Fig. 2. First, Φ_{CH} drops, injecting negative charge on the differential input pins. Soon thereafter, Φ_{CHINV} rises, injecting almost the same amount of charges but with positive polarity. Ideally, these negative and positive charges cancel out instantaneously at each input pin, if the transitions of the two clocks occur at the exact same time. In practice, however, there must be some dead time between the two clocks, in order not to short the differential input pins with the switches. The glitch amplitude depends on the source impedances, the dead time, and the amount of charge injection. Similarly, after a half chopping period, Φ_{CHINV} drops and Φ_{CH} rises, resulting in another glitch.

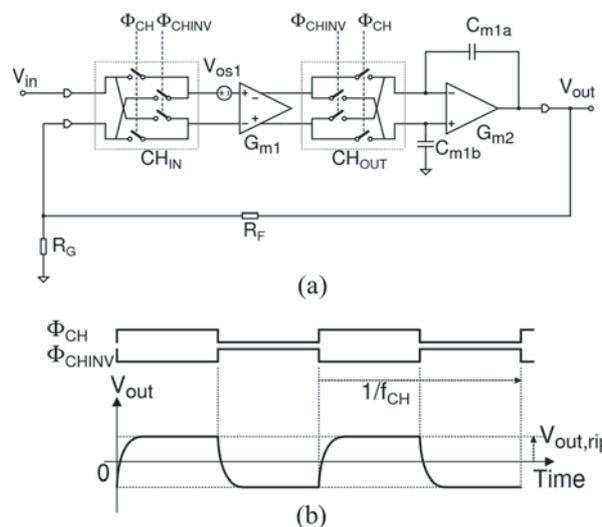


Fig. 1 Chopper op-amp in a closed-loop: (a) circuit diagram; (b) chopper clock and output ripple waveform.

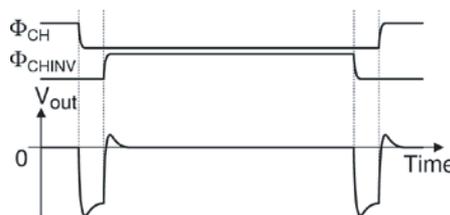


Fig. 2 Output glitch due to input charge injection.

Manuscript received November 12, 2019.

Manuscript publicized April 9, 2020.

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DOI: 10.1587/transele.2019CTI0001

Figure 3 shows the output noise power spectral density (PSD) of a chopper op-amp, taking both the ripple and the glitches into account. The PSD increases at the odd harmonics of the chopping frequency f_{CH} due to the up-modulated ripple, and at the even harmonics of f_{CH} due to the glitches. These noise spectra peaks usually need to be attenuated by a post low-pass filter, which increases cost and limits the usable signal bandwidth.

1.3 Input Bias Current and Residual Offset

Charge injection mismatch causes DC errors such as residual offset and input bias current [2], [3]. Close inspection shows that only the charge injection mismatch in the signal path between the two choppers is down-modulated, and thus contributes to the DC errors. As shown in Fig. 4 (a), CH_{IN} consists of four switches S_{1-4} , which inject charges q_{1-4} during every clock transition.

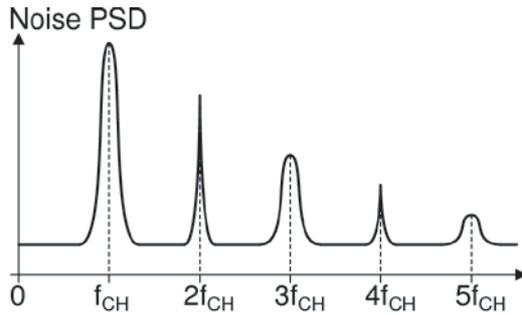


Fig. 3 Output noise PSD of a chopper op-amp.

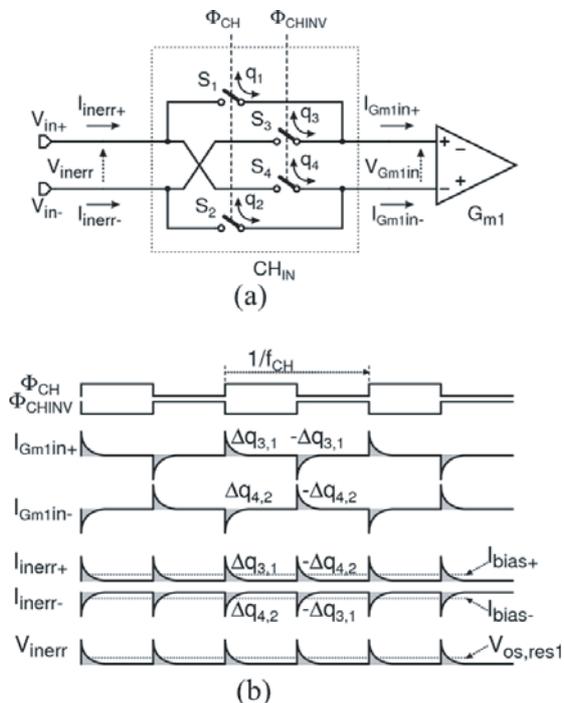


Fig. 4 Input bias current and residual offset due to input chopping: (a) circuit diagram; (b) transient waveform.

As shown in Fig. 4 (b), charge injection mismatches $\Delta q_{3,1} = q_3 - q_1$ and $\Delta q_{4,2} = q_4 - q_2$ are down-modulated so that the transient input currents I_{inerr+} and I_{inerr-} include the DC bias components I_{bias+} and I_{bias-} given by:

$$I_{bias+} = f_{CH}(\Delta q_{3,1} - \Delta q_{4,2}) \quad (3)$$

$$I_{bias-} = -f_{CH}(\Delta q_{3,1} - \Delta q_{4,2}). \quad (4)$$

Moreover, in conjunction with the on-resistance of each switch R_{on} and the source resistances driving the op-amp (R_{S+} and R_{S-}), these input bias currents cause a residual input offset voltage $V_{os,res}$ equal to:

$$V_{os,res} = f_{CH}(\Delta q_{3,1} - \Delta q_{4,2})(2R_{on} + R_{S+} + R_{S-}). \quad (5)$$

1.4 Summary of AC and DC Errors Due to Switching Artifacts

Many op-amp users prefer higher chopping frequency f_{CH} to locate the noise spectra peaks at higher frequencies and to extend the usable signal bandwidth. However, this increases the residual offset and input bias current. Those DC errors will also increase proportional to the amount of charge injection mismatch when wider input switches are used to reduce the on-resistances, hence the thermal noise. As discussed in later sections, researchers have invented various circuit techniques to reduce such AC and DC errors in chopper op-amps.

2. Ripple Reduction Techniques

2.1 Multi-Path Chopper Offset Stabilization

To attenuate the ripple amplitude, Witte proposed multi-path chopper offset stabilized op-amp employing active filter in 2006 [4].

As shown in the circuit diagram in Fig. 5, the proposed op-amp consists of a low frequency path (LFP) and a high frequency path (HFP) in parallel. The LFP further consists of the input transconductor G_{m1} and the subsequent three transconductors G_{m2-4} , whereas the HFP consists of the other input transconductor G_{m5} and shares G_{m4} with the LFP. The LFP dominates the low frequency performance of the overall op-amp, and G_{m1} is chopped to achieve low offset. The up-modulated input offset V_{os1} is filtered by two

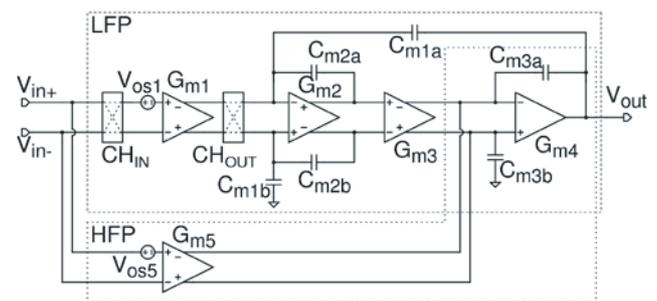


Fig. 5 Multi-path chopper offset stabilized op-amp.

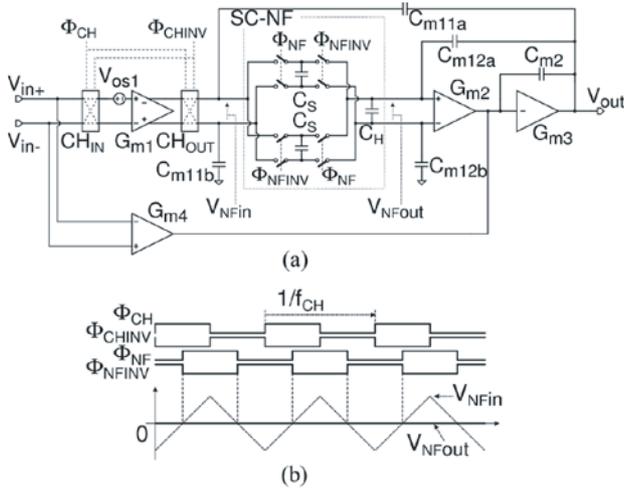


Fig. 6 Chopper op-amp employing a SC notch-filter: (a) circuit diagram; (b) timing diagram.

integrators built around G_{m2} and G_{m4} . The output ripple amplitude $V_{out,rip}$ is then given by:

$$V_{out,rip} = \frac{G_{m1}}{2f_{CH}C_{m2a,b}} \cdot \frac{G_{m3}}{G_{m5}} A_{CL} V_{os1}, \quad (6)$$

where A_{CL} is the closed-loop gain set by the external resistors. $V_{out,rip}$ can be reduced by adjusting parameters in the LFP such as G_{m1} , G_{m3} , and $C_{m2a,b}$. On the other hand, the unity gain bandwidth is set by the HFP and is equal to $G_{m5}/(2\pi C_{m3a,b})$. The offset of the HFP (V_{os5}) is offset stabilized by the LFP. However, in conjunction with the finite voltage gain of the LFP, it produces a residual offset $V_{os,res}$ given by:

$$V_{os,res} = \frac{A_{v5}}{A_{v1}A_{v2}A_{v3}} V_{os5}, \quad (7)$$

where $A_{v1,2,3,5}$ are the DC voltage gains of $G_{m1,2,3,5}$, respectively. One drawback is that this technique requires additional transconductors and capacitors to realize multiple integrators.

2.2 Switched Capacitor Notch Filter

Since the phase of the ripple is aligned with the chopping clocks, a switched capacitor notch filter (SC-NF) can be implemented with clocks synchronized with the chopping.

Figure 6 (a) shows a block diagram of the op-amp proposed by Burt in 2006 [5]. This again consists of a LFP and a HFP, where the LFP includes a SC-NF following the chopped input transconductor G_{m1} . Figure 6 (b) shows the timing diagram of the chopping (Φ_{CH} and Φ_{CHINV}) and the SC-NF (Φ_{NF} and Φ_{NFINV}), as well as the input and output voltages of the SC-NF (V_{NFIn} and V_{NFOut}). First, V_{NFIn} contains a triangular ripple due to the up-modulated output current of G_{m1} . However, since Φ_{NF} and Φ_{NFINV} operate at the same frequency as Φ_{CH} and Φ_{CHINV} but with a 90-degree phase difference, the SC-NF samples the triangular ripple

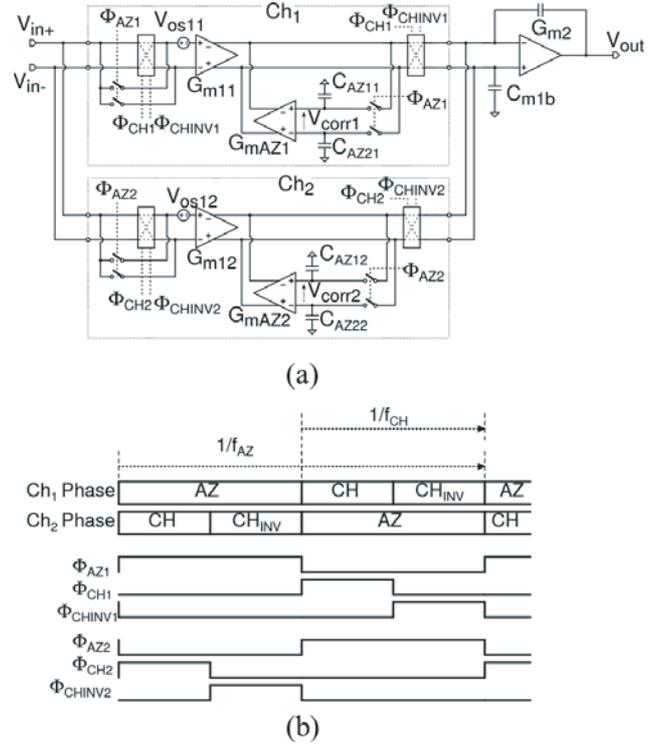


Fig. 7 A ping-pong auto-zero and chopper op-amp: (a) circuit diagram; (b) timing diagram.

whenever the amplitude becomes zero, and thus results in the ripple free output voltage V_{NFOut} . This SC-NF adds a 90-degree phase delay to the signal at the chopping frequency, so that the HFP is required to bypass this phase delay and to stabilize the overall op-amp.

This filter does not consume quiescent current, and thus is more power efficient than active filters so that the proposed op-amp only consumes $17\mu A$ of current. However, there are some drawbacks. First, clock skew and sampling capacitor mismatch result in residual ripple. Second, the sampled noise onto C_S can contribute to the overall in-band noise PSD. Third, G_{m1} must have a wide output range to tolerate the maximum ripple amplitude, since the ripple still exists there. This problem becomes more severe in low noise designs, because the ripple amplitude at V_{NFIn} is proportional to G_{m1}/C_S .

2.3 Combination with Auto-Zeroing

Instead of filtering, the ripple amplitude can be reduced by reducing the initial offset before being up-modulated. In 2002, Tang proposed combining auto-zeroing and chopping the block diagram of which is shown in Fig. 7 (a) [6].

To achieve continuous-time amplification, it ping-pongs two input channels Ch1 and Ch2, followed by an output stage G_{m2} . As shown in the timing diagram Fig. 7 (b), each channel is driven by three clocks $\Phi_{AZ1,2}$, $\Phi_{CH1,2}$, and $\Phi_{CHINV1,2}$, to define auto-zeroing (AZ), chopping (CH), and inverting-chop (CH_{INV}) phases. When one channel is in the

AZ phase, the other goes through CH and CH_{INV} phases. At the end of each AZ phase, the offset correction signals $V_{corr1,2}$ are sampled on capacitors $C_{AZ11,21,12,22}$ to cancel each initial offset $V_{os11,12}$. The resulting output ripple is reduced by a factor of the auto-zeroing loop, which can be usually higher than 80dB by utilizing cascode topology. The chopping frequency f_{CH} is set at twice the auto-zeroing frequency f_{AZ} .

Figure 8 (a), (b), and (c) show the expected noise PSDs of before auto-zeroing or chopping, after the auto-zeroing, and after the auto-zeroing and the chopping, respectively. The auto-zeroing almost eliminates $1/f$ noise, but introduces increased in-band noise PSD due to the broadband noise PSD folding [1]. This increased noise PSD lies in between DC and f_{AZ} . The chopping then up-modulates this high noise PSD up to f_{CH} , to obtain an in-band noise PSD that is only slightly higher than the initial thermal noise floor.

This op-amp achieves a $3\mu\text{V}$ offset and a $20\text{nV}/\sqrt{\text{Hz}}$ in-band noise PSD, while consuming $800\mu\text{A}$ of current. One drawback is the additional current consumption and die area for one extra input channel.

2.4 Auto-Correction Feedback

In 2010, Kusuda proposed auto-correction feedback (ACFB) to reduce the initial offset, hence the ripple, without requiring auto-zeroing [7], [8].

Figure 9 shows the circuit diagram of the proposed op-amp which consists of a low frequency path (LFP) by three transconductors G_{m1-3} , and a high frequency path (HFP) by transconductors G_{m4} and G_{m3} . The initial offset V_{os1} is up-modulated and results in ripples at the output V_{out} and an

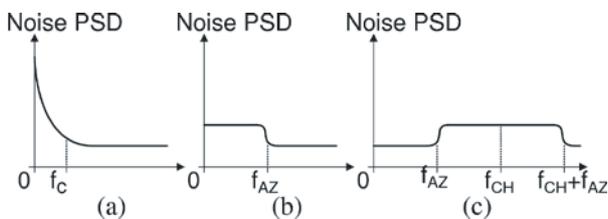


Fig. 8 Noise PSDs (a) without auto-zeroing or chopping, (b) after auto-zeroing, and (c) after auto-zeroing and chopping.

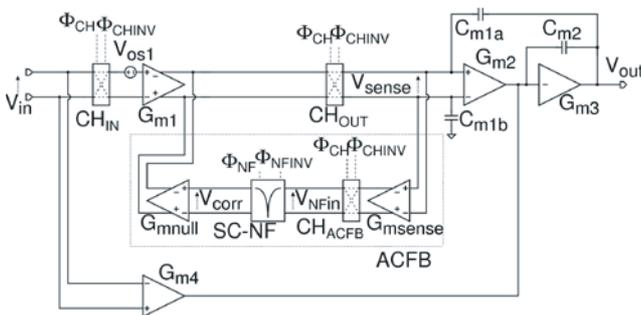


Fig. 9 Chopper op-amp employing auto-correction feedback.

internal node V_{sense} . The ACFB senses the ripple at V_{sense} , down-modulates it by CH_{ACFB}, and generates an offset correction signal V_{corr} . Based on V_{corr} and the feedback of the ACFB, an offset nulling transconductor G_{mnull} cancels V_{os1} to reduce the output ripple amplitude. A switched capacitor notch filter (SC-NF) is controlled by the same clock timings as the one in Fig. 6 (b) – Φ_{NF} and Φ_{NFINV} operate at the same frequency as the chopping clocks Φ_{CH} and Φ_{CHINV} but with a 90-degree phase difference. The desired input signal V_{in} results in a triangular ripple at $V_{NF,IN}$ after being modulated by CH_{IN}, CH_{OUT}, and CH_{ACFB}. This ripple is filtered by the SC-NF, such that the ACFB does not affect V_{in} .

The op-amp presented in [8] achieves $0.5\mu\text{V}$ maximum offset and $5.6\text{nV}/\sqrt{\text{Hz}}$ noise PSD while consuming 1.4mA of current. Compared to the implementation in [6], which uses a SC-NF in the main signal path, the ACFB requires two extra transconductors to sense the ripple and to cancel the initial offset, although they only consume 6% of the total current. On the other hand, when desired, the ACFB offers flexibility in choosing a relatively low chopping frequency, which reduces the input bias current. Moreover, the sampled noise in the SC-NF is up-modulated and thus does not contribute to the resulting in-band noise PSD.

3. Glitch Reduction Techniques

3.1 Adaptive Clock Boosting Technique

As explained in the Sects. 1.2 and 1.3, charge injections of input chopper switches cause transient output glitches, and the charge injection mismatch leads to a residual offset and input bias current. On the other hand, the switches must be made sufficiently wide to reduce the on-resistance and the thermal noise.

This requires a trade-off among the in-band noise PSD, the output glitches, and the residual offset in a chopper op-amp design. Moreover, the on-resistance of a conventional CMOS switch changes over the input common-mode voltage (V_{CM}) and the supply voltage (V_{SY}) due to the change of its overdrive voltage.

Figure 10 (a) and (b) shows the on-conductances of an

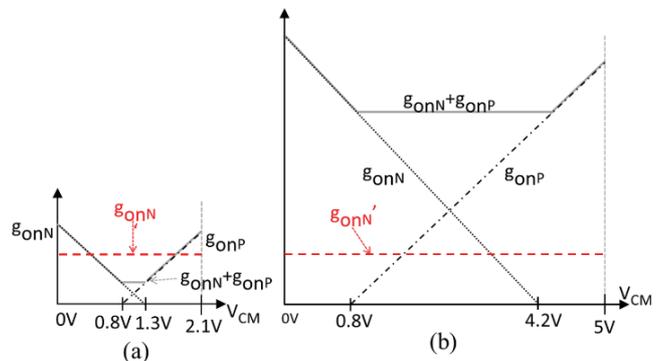


Fig. 10 On conductances of a conventional CMOS switch $g_{onN}+g_{onP}$ and a NMOS switch with a constant overdrive voltage $g_{onN'}$ (a) with $V_{SY} = 2.1\text{V}$ and (b) $V_{SY} = 5\text{V}$

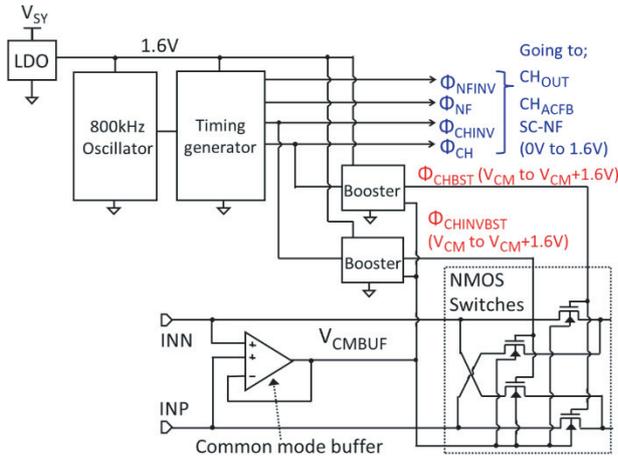


Fig. 11 Input chopping circuit and clock generator employing an adaptive clock boosting technique.

NMOS g_{onN} , a PMOS g_{onP} , and a CMOS switch $g_{onN} + g_{onP}$ over a rail-to-rail V_{CM} range with $V_{SY} = 2.1$ and 5.0 V, respectively. The PMOS is typically sized three times as wide as the NMOS to compensate for the lower mobility of holes compared to electrons. The on-conductance $g_{onN} + g_{onP}$ is lowest, when V_{SY} is the lowest and V_{CM} is in the middle of V_{SY} . Thus, the switches must be made sufficiently wide to achieve the targeted noise PSD for this voltage condition. Such wide switches are oversized for the other voltage conditions, and thus generate more charge injection. This increases transient glitches and residual offset, and degrades the CMRR and the PSRR. This problem can be solved by maintaining the overdrive voltage of an NMOS switch constant and independent of changes in V_{SY} and V_{CM} , so that its on-conductance g_{onN}' remains constant as shown in Fig. 10 (a) and (b).

Figure 11 presents the proposed NMOS input chopper CH_{IN} as well as the clock boosters to maintain the overdrive voltage constant. This circuit is used in the chopper op-amp shown in Fig. 9 [8]. The clock generator consists of an 800kHz oscillator and a timing generator based on D-latches, resulting in two sets of 200kHz complementary clocks with a 90-degree phase shift Φ_{CH} , Φ_{CHINV} and Φ_{NF} , Φ_{NFINV} . Supplied by a 1.6V LDO, those clocks have a fixed 1.6V amplitude to drive NMOS switches other than input switches, i.e. CH_{OUT} , CH_{ACFB} , and the SC-NF.

Based on Φ_{CH} and Φ_{CHINV} , two identical adaptive clock boosters generate the boosted output clocks Φ_{CHBST} and $\Phi_{CHINVBST}$ by utilizing the 1.6V LDO output and a buffered input common-mode voltage $V_{CM BUF}$ from a common-mode buffer. In each phase, one adaptive clock booster drives two NMOS switches to $V_{CM BUF} + 1.6V$ to turn on, while the other drives the other two NMOS switches to $V_{CM BUF}$ to turn off. The common-mode buffer also drives the backgates of the NMOS switches to avoid the body effect. With a fixed 0.8V NMOS threshold voltage, the overdrive voltage and the clock swing are kept constant at 0.8V and 1.6V, respectively, with the changes in the input

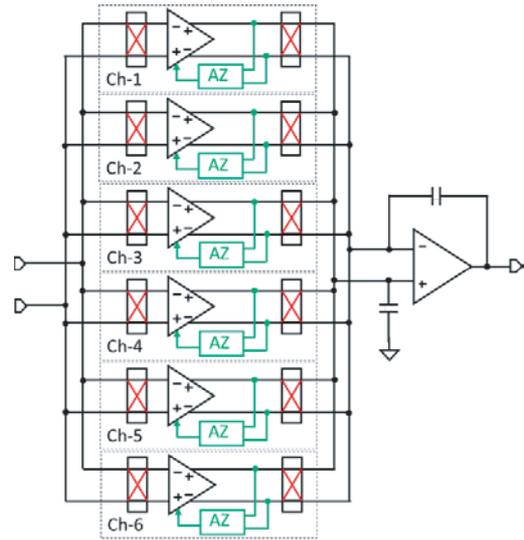


Fig. 12 Auto-zero and chopper op-amp with split six input channels

common-mode and supply voltages. This avoids the use of oversized switches, and improves the transient glitch, the residual offset, the CMRR, and the PSRR. The on-resistance of each switch is designed to be 200Ω , so that the noise PSD of the overall op-amp is still dominated by the thermal noise of G_{mI} . With the combination of $5.6nV/\sqrt{Hz}$ noise PSD, this op-amp achieves $0.5\mu V$ maximum offset and $400pA$ maximum input bias current which would be several times larger if conventional CMOS switches were used at the input.

3.2 A Multi-Channel Auto-Zero and Chopper Op-Amp with Interleaved Clocks

Another way to reduce the glitch amplitude is to spread out the energy of charge injection over time, by splitting input switches into multi-channels. In 2015, Kusuda proposed an auto-zero and chopper op-amp consisting of six input channels as shown in Fig. 12 [9]. Each channel consists of an input chopper, input transconductor, an output chopper, and an auto-zeroing loop to reduce the up-modulated ripple amplitude. As shown in the clock timing diagram in Fig. 13, each channel goes through auto-zeroing phase (AZ), chopping phase (CH), and inverting-chop phase (CH_{INV}). The phases of the six channels are interleaved, so that while two channels are in the AZ phase, the other four channels are either the CH or CH_{INV} phases at a time. By always having four channels in the signal path, the required size of the switch and the required amount of transconductance are reduced by a factor of four.

Figure 13 also shows the expected glitch waveforms from each channel and their total combined. Compared to a chopper op-amp with single channel design, the glitch amplitude from each channel is four times smaller, and two channels generate glitches at a time. Therefore, the total glitch amplitude is expected to be two times smaller. Moreover, compared to ping-pong auto-zero and chopper op-amp

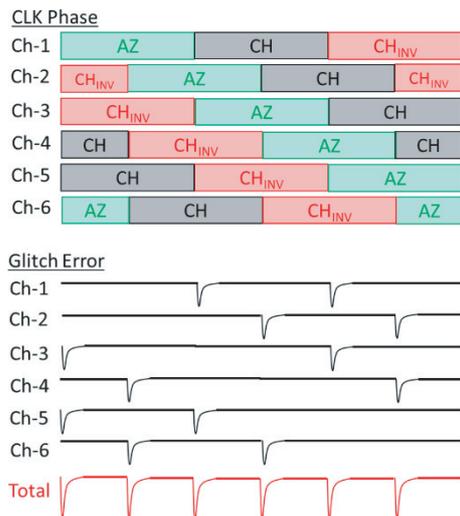


Fig. 13 The clock timing diagram and expected output glitch of Fig. 12

shown in Fig. 6, the proposed op-amp consumes less relative current for auto-zeroing, and is therefore more power efficient.

It is possible to further increase the number of channels to reduce the glitch amplitude. However, this decreases the time available for auto-zeroing phase, which may increase the current consumed in the auto-zeroing stage to meet the settling requirement. This also increases extra die area required for spacing between the adjacent channels. This op-amp achieved a $5\mu\text{V}$ maximum offset and a $5.8\text{nV}/\sqrt{\text{Hz}}$ noise PSD while consuming $840\mu\text{A}$ of current.

4. Input Bias Current and Residual Offset Reduction Techniques

4.1 Nested Chopping

In 2000, Bakker proposed nested chopping employing two different chopping frequencies as shown in Fig. 14 (a) [10]. An inner set of input and output choppers $\text{CH}_{\text{INinner}}$ and $\text{CH}_{\text{OUTinner}}$ are driven by a high chopping frequency f_{CHhigh} . While an outer set of input and output choppers $\text{CH}_{\text{INouter}}$ and $\text{CH}_{\text{OUTouter}}$ are driven by a low chopping frequency f_{CHlow} . Figure 14 (b) shows the expected transient waveforms along with the clock timings. In this example, f_{CHhigh} is set four times higher than f_{CHlow} , and only the glitches generated by the inner chopping are shown for simplicity. First charge injection mismatch in $\text{CH}_{\text{INinner}}$ causes voltage glitches V_{inA1} at the input of amplifier A_1 .

These glitches are down-modulated by $\text{CH}_{\text{OUTinner}}$ and thus produce DC error V_{outinner} . Then, the outer chopper $\text{CH}_{\text{OUTouter}}$ up-modulates V_{outinner} again, so that an output V_{out} contains no residual offset. Similarly, the input bias currents caused by $\text{CH}_{\text{INinner}}$ are up-modulated by $\text{CH}_{\text{INouter}}$, resulting in no DC input bias currents at the overall input pins. Through the operation of two output choppers, the offset and $1/f$ noise of A_1 are up-modulated to two frequencies $f_{\text{CHhigh}} \pm f_{\text{CHlow}}$. Therefore, f_{CHlow} can be set even

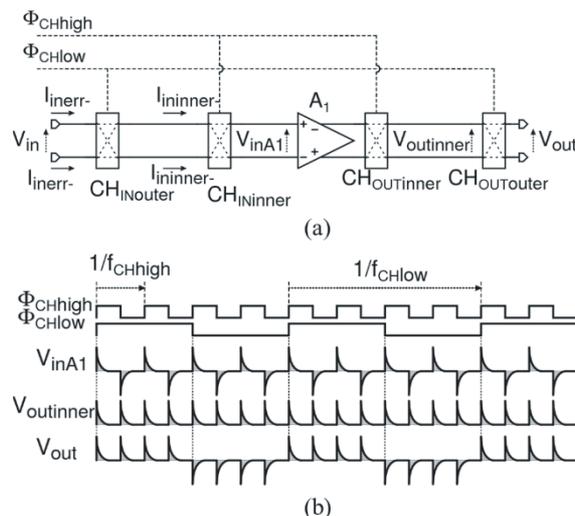


Fig. 14 Nested chopping: (a) circuit diagram; (b) transient waveforms.

below the $1/f$ noise corner frequency, while almost eliminating the $1/f$ noise from the baseband. Consequently, the residual offset caused by the outer chopper can be reduced to a very low level. In summary, the nested chopping technique utilizes two separate chopping frequencies, so that the $1/f$ noise can be mitigated by a high f_{CHhigh} while the residual offset can be determined by a low f_{CHlow} . With $f_{\text{CHlow}} = 2\text{kHz}$ and $f_{\text{CHhigh}} = 16\text{kHz}$, the proposed op-amp achieves a 100nV offset and a $27\text{nV}/\sqrt{\text{Hz}}$ noise PSD. One drawback is that the outer chopper creates spectral peaks at f_{CHlow} , which limits the usable signal bandwidth. Another drawback is that to achieve a targeted noise PSD, wider switches must be used, since two switches are connected in series.

4.2 Input Bias Current Trimming by Compensating Charge Injection Mismatches

In 2015, Kusuda proposed a charge mismatch compensation circuit as shown in Fig. 15 [9]. The four NMOS switches S_{1-4} are the input chopper switches and driven by positive and negative clock supplies CV_{DD} and CV_{SS} through inverters. Let us assume S_1 is associated with a coupling capacitor $C_P + \Delta C_P$, while each of the other three switches is associated with C_P . This capacitance mismatch ΔC_P causes a charge injection mismatch per clock period $1/f_{\text{CLK}}$, generating initial input bias currents $I_{\text{binit}+}$ and $I_{\text{binit}-}$ equal to:

$$I_{\text{binit}+} \equiv I_{\text{binit}} = f_{\text{CLK}} \cdot \Delta C_P \cdot (CV_{\text{DD}} - CV_{\text{SS}}), \quad (8)$$

$$I_{\text{binit}-} \equiv -I_{\text{binit}} = -f_{\text{CLK}} \cdot \Delta C_P \cdot (CV_{\text{DD}} - CV_{\text{SS}}). \quad (9)$$

To offset these error currents, the charge mismatch compensation circuit can inject charge mismatches with opposite polarity through four metal-metal coupling capacitors C_{C1-4} . An adjustable positive supply $CV_{\text{DD,DACP}}$ drives C_{C1} and C_{C3} , while another adjustable positive supply $CV_{\text{DD,DACN}}$ drives C_{C2} and C_{C4} . By adjusting these supply voltages, the resulting compensation input bias currents $I_{\text{bcomp}+}$ and

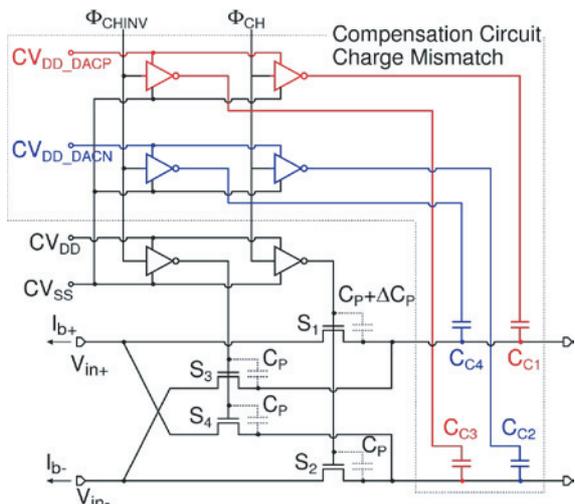


Fig. 15 The input chopping circuit and clock generator employing an adaptive clock boosting technique.

I_{bcomp-} can be controlled to allow:

$$\begin{aligned} I_{bcomp+} &\equiv I_{bcomp} \\ &= 2f_{CLK} \cdot C_{C1-4} \cdot (CV_{DD_DACP} - CV_{DD_DACN}), \end{aligned} \quad (10)$$

$$\begin{aligned} I_{bcomp-} &\equiv -I_{bcomp} \\ &= -2f_{CLK} \cdot C_{C1-4} \cdot (CV_{DD_DACP} - CV_{DD_DACN}). \end{aligned} \quad (11)$$

$C_{C1-4} = 2fF$ is only one-tenth of C_P , which will not significantly increase the absolute amount of charge injection nor, consequently, the magnitude of transient glitches. The resulting input bias currents I_{b+} and I_{b-} are given by:

$$I_{b+} = I_{binit} + I_{bcomp}, \quad (12)$$

$$I_{b-} = -(I_{binit} + I_{bcomp}). \quad (13)$$

Both I_{b+} and I_{b-} will be pushed toward zero by adjusting $I_{bcomp} = -I_{binit}$. Moreover, since the initial input currents and the compensation input bias currents are both proportional to the clock frequency, the cancellation remains stable with the change of the clock frequency over temperature.

The trimming is performed at a single temperature of 25°C – the initial input bias current is measured externally and then adjust CV_{DD_DACP} and CV_{DD_DACN} through an on-chip DAC. This reduced the maximum input bias current from 1.5nA to 150pA at 25°C. Changing the temperature to 85°C only increased the maximum input bias current up to 200pA without requiring additional trimming.

5. Comparison of the Techniques

Table 1 compares circuit techniques and the achieved specifications of chopper op-amps introduced in this paper, with the order of publication year (the oldest one is shown in the most left). Most chopper op-amp designs before 2011 addressed ripple reductions. Among three designs [4]–[6], the one in [6] employs feedback to reduce initial offset, and thus can expect the lowest output ripple amplitude. However, this

Table 1 Comparison of specifications and circuit techniques of chopper op-amps.

Author	Bakker [10]	Tang [6]	Witte [4]	Burt [5]	Kusuda [8]	Kusuda [9]
Year	2000	2002	2006	2006	2011	2015
Isy [μA]	100	800	700	17	1400	840
fCH [kHz]	16	15	32	125	200	1200
Vos,max [μV]	* 0.1	5.0	3.0	10.0	0.5	5.0
Ibias,max [pA]	**NS	100	**NS	200	400	150
GBW [MHz]	0.4	2.5	1.37	0.35	4.0	3.1
NSD [nV/√Hz]	19	20	15	55	5.6	5.8
NEF	7.3	21.8	15.3	8.7	8.1	6.5
GBW/Isy	4.0	3.1	2.0	20.6	2.9	3.7
Die area[mm ²]	1.5	0.67	3.6	0.7	1.26	1.58
Ripple reduction technique	-	Auto -zero	Active Filter	SC-NF	ACFB	6-channel Auto-zero
Glitch reduction technique	-	-	-	-	CLK booster	***CLK interleave
Residual offset reduction	Nested chopper	-	-	-	CLK booster	***Charge Trim

* Typical Vos, ** Data not shown, *** CLK booster is also used

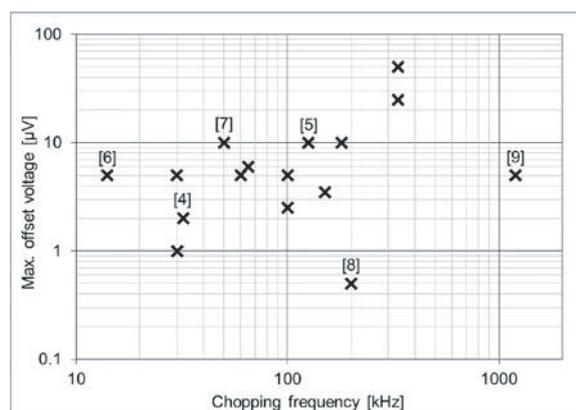


Fig. 16 Maximum offset versus chopping frequency of chopper op-amps.

design consumes extra current for auto-zeroing, and therefore shows the highest noise efficiency factor (NEF), which indicates the amount of noise PSD when every design is scaled to the same current consumption [11].

Later than 2011, the two designs in [8], [9] employ feedback to better reduce resulting ripple, but also in power efficient ways to achieve lower NEF than the design in [6]. Moreover, those two designs employ techniques to reduce residual offset, and consequently, achieved competitive maximum offset Vos,max and maximum input bias current Ibias,max with relatively high chopping frequencies fCH.

Figure 16 plots the chopping frequency versus the maximum offsets of 16 different op-amp designs. The offset tends to increase with the chopping frequency. The designs in [8] and [9] achieve relatively low offset of 0.5μV and 5μV with 200kHz and 1.2MHz of chopping frequency, respectively.

Figure 17 (a) shows the measured noise PSD of [8] and [9] to compare their glitch reduction techniques. Additionally, Fig. 17 (b) shows the corresponding integrated RMS noise over the frequencies. The op-amp in [9] shows smaller peak noise PSDs at its chopping and harmonic frequencies, thanks to the glitch and ripple reduction techniques.

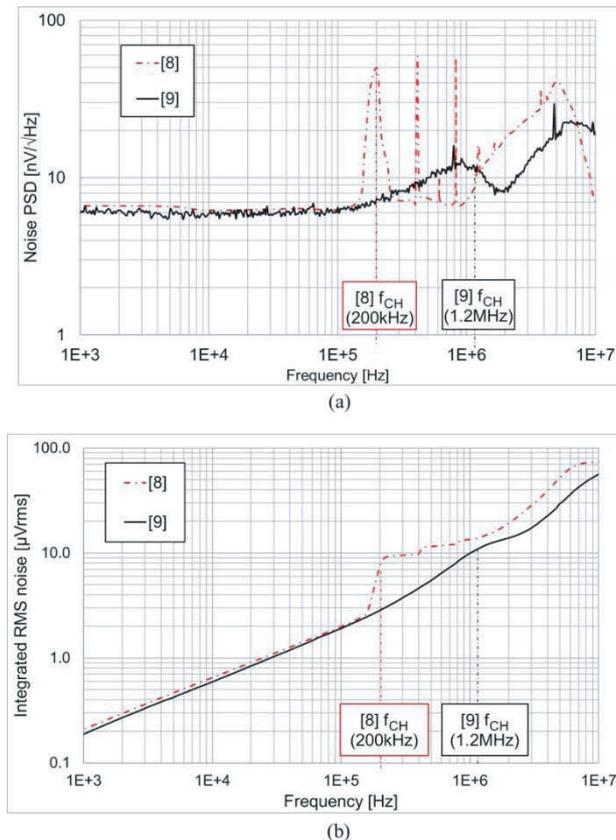


Fig. 17 (a) Noise PSD of [8] and [9]; (b) their integrated RMS noise

Consequently, for a 500kHz bandwidth, the integrated noise of the op-amps in [8] and [9] are $11.6\mu V_{rms}$ and $5.4\mu V_{rms}$, respectively. From another perspective, to target $10\mu V_{rms}$ integrated noise, the usable signal bandwidths of the op-amps in [8] and [9] are 400kHz and 1MHz, respectively.

6. Conclusion

This paper reviewed circuit techniques to reduce undesired switching artifacts – ripple, transient glitches, as well as residual offset and input bias current. As demonstrated by newer designs employing advanced circuit techniques [8], [9], noise spectra peaks due to switching artifacts can be reduced and pushed toward higher frequencies without significantly increasing DC errors. Such newer chopper op-amp designs can relax the requirements of post low-pass filters, and therefore serve a broader range of applications requiring wider usable signal bandwidth.

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