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Ultra-Low Quiescent Current LDO with FVF-Based Load Transient Enhanced Circuit

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SUMMARY This paper proposes an ultra-low quiescent current low-dropout regulator (LDO) with a flipped voltage follower (FVF)-based load transient enhanced circuit for wireless sensor network (WSN). Some characteristics of an FVF are low output impedance, low voltage operation, and simple circuit configuration [1]. In this paper, we focus on the characteristics of low output impedance and low quiescent current. A load transient enhanced circuit based on an FVF circuit configuration for an LDO was designed in this study. The proposed LDO, including the new circuit, was fabricated in a 0.6 μm CMOS process. The designed LDO achieved an undershoot of 75 mV under experimental conditions of a large load transient of 100 μA to 10 mA and a current slew rate (SR) of 1 μs. The quiescent current consumed by the LDO at no load operation was 204 nA.

key words: *low-dropout regulator, low quiescent current, fast transient response, FVF, WSN*

1. Introduction

The spread of internet of things (IoT) modules makes proposals for hardware changes in wireless sensor network (WSN) more dynamic than they were in the past. The market of battery-operated and energy harvest modules is expected to expand sharply because of the advantages of easier installation and lower maintenance cost. However, obtaining a battery with a long-life span poses complex issues. Using a bigger battery requires a larger module, effectively restricting the installation of the latter. Using a specific kind of battery with a long-life span increases the cost of the battery itself. Therefore, a general solution is to reduce the quiescent current of integrated circuits (IC). Currently, low power micro control units (MCU) with sub-μA sleep current are available [2]. Through these, the weight of the quiescent current of power management ICs in a module increases. This is why power management IC with low quiescent current are needed. The output voltage of a battery is not constant; hence, a low-dropout regulator (LDO) is generally used to stabilize the voltage for an MCU operation. An LDO can generate clean and high precision low voltage that is independent of the input voltage. Moreover, it has the advantage of occupying a smaller space than switching converters because it has fewer external components. A well-known fact is that there is a trade-off between having a low quiescent current and a transient response or power supply ripple reduction, which were the motivations of past studies. The transient response degradation causes MCU to malfunction [3], [4]; thus, it is recognized as a significant characteristic of power management IC. The fast current slew rate (SR) to the gate of the pass transistor realizes a fast settling time and small undershoot and overshoot. Some standard approaches have been adopted in the past to improve transient response. I. Amplifying the AC signal of the output voltage of the LDO using a high pass filter and an amplifier [5]–[10]; II. adding a buffer to the output stage of the error amplifier to extend the loop bandwidth [11], [12]; III. extending the bandwidth of the error amplifier by changing its configuration [13], [14]; IV. providing a lower impedance pass transistor stage to extend the loop bandwidth [15]–[17]. But the approach I usually needs extra current passes which increase quiescent current and large filter components. The approach II is not appropriate for ultra-low quiescent current LDO because of low bandwidth of the error amplifier. The approach III needs complicated configurations, and these increase quiescent current. Approach IV makes designing circuit to voltage range of input difficult. In this study, the proposed circuit employs the approach I under ultra-low quiescent current. This technique does not need complicated circuit configuration and suppresses increasing quiescent current under nA order operation. It can also significantly attenuate the undershoot occurring in large load transient, significantly reducing transient settling time compared to conventional LDOs.

2. Proposed LDO Structure and Circuit Implementation

In this section, we describe the characteristics of the FVF filter and the FVF-based load transient enhanced circuit (FBLC) which consists of an FVF filter. Furthermore, we explain simulation results of the LDO with FBLC.

2.1 FVF Filter

Figure 1 shows the structure and small signal equivalent circuit of a flipped voltage follower (FVF) filter. The FVF filter is designed based on an FVF with capacitor. Figure 2 shows the SPICE simulation results of the frequency characteristic when node A is the input and node C is the output in Fig. 1. Simulation conditions were V_{dd} = 2.2 V, C_{cap} = 1 pF, C_{load} = 5 pF, and *quiescent current* = 5 nA. The FVF fil-

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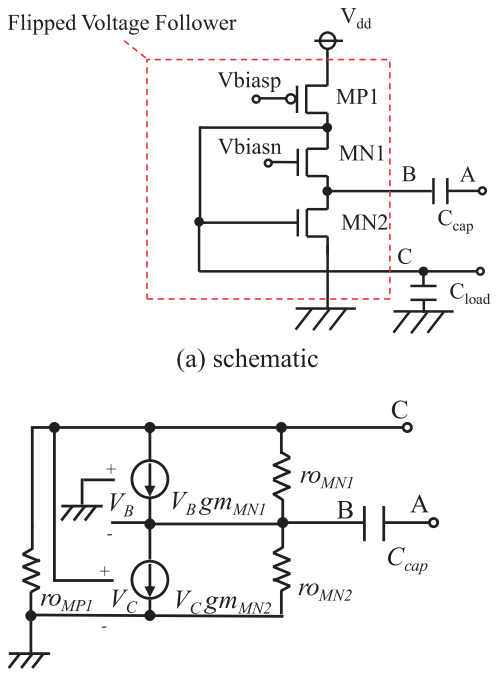


Fig. 1 FVF filter

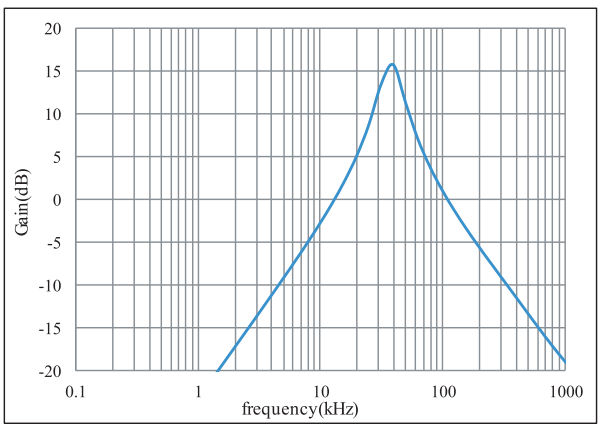


Fig. 2 Frequency characteristic of FVF filter

ter was confirmed to work as a frequency limited amplifier, as shown in Fig. 2.

The point is this circuit can respond to kHz order signal with *quiescent current* = 5 nA. This characteristic could amplify signal faster than other technics under nA order operation. The low impedance characteristic of node B realizes the unity gain frequency (f_u) in kHz order.

2.1.1 Peak Gain Frequency

The peak gain frequency f_g is calculated as

$$f_g = \frac{1}{2\pi Z_Y C_{cap}}, \tag{1}$$

where Z_Y is the impedance of node B. We found that Eq. (1) was the same as that of the high pass filter (HPF) cutoff frequency.

The peak gain frequency of the FVF filter was calculated using the cut-off frequency of the RC filter, which was configured by C_{cap} and Z_Y. Z_Y can be expressed as

$$Z_Y = \frac{1}{gm_{MN1}gm_{MN2}ro_{MN1}} \| \frac{1}{\omega C_{load}}, \tag{2}$$

where gm_{MN1} and gm_{MN2} are the transconductances of MN1 and MN2, respectively, and ro_{MN1} is the output resistance of MN1.

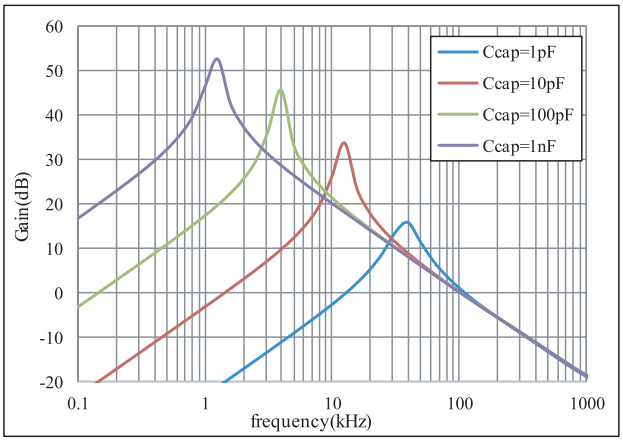


Fig. 3 Frequency characteristic of FVF filter changing C_{cap} value

2.1.2 Pole Frequency

When node B is the input and node C is the output in Fig. 1, the DC gain value G_{DC} may be calculated as:

$$G_{DC} = gm_{MN1}\left(ro_{MP1} \| gm_{MN1}ro_{MN1}\frac{1}{gm_{MN2}}\right), \tag{3}$$

where ro_{MP1} is the output resistances of MP1.

Z_O, which is the impedance of node C, can be expressed as:

$$Z_O = \frac{1}{ro_{MP1} \| gm_{MN1}ro_{MN1}\frac{1}{gm_{MN2}}}. \tag{4}$$

The pole frequency (f_p), related to Z_O, is expressed as

$$f_p = \frac{1}{2\pi Z_O C_{load}}. \tag{5}$$

The pole frequency f_p is the cut-off frequency of the DC gain value G_{DC}.

Figure 3 shows the frequency characteristic of an FVF filter as the C_{cap} value changes through a SPICE simulation. Simulation conditions were the same as Fig. 2. In addition, Eq. (1) and Fig. 3 show that we can select the required bandwidth that is amplified by changing the C_{cap} value.

2.2 FVF-Based Load Transient Enhanced Circuit

FVF-based load transient enhanced circuit (FBLC) consists

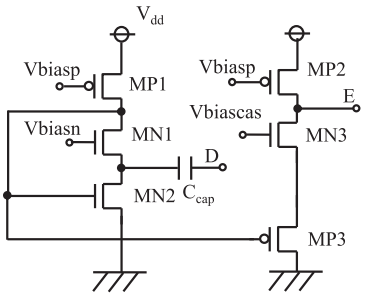


Fig. 4 Frequency characteristic of FVF filter

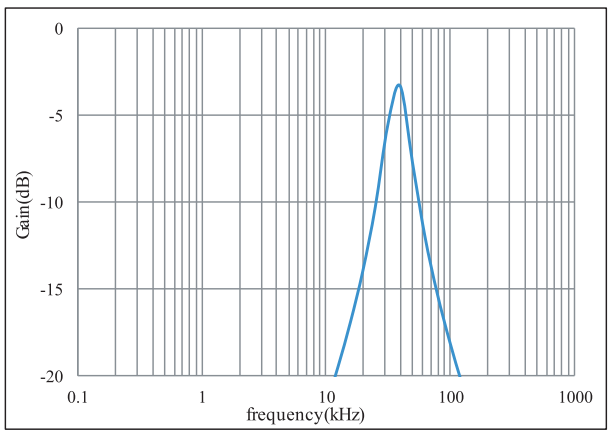


Fig. 5 Frequency characteristic of FVF based load transient enhanced circuit

of an FVF filter and a source follower amplifier. Figure 4 shows the configuration of the FBLC. Figure 5 shows the frequency characteristic when node D is the input and node E is the output in Fig. 4.

From Fig. 5, it was observed that the characteristics of FBLC was similar to that of the FVF filter. Simulation conditions were V_{dd} = 2.2 V, C_{cap} = 1 pF, and *quiescent current* = 20 nA. If the f_u of a source follower amplifier consisted of MP2, MP3, MN3 is higher than that of the FVF filter, f_g of FBLC may be calculated using Eq. (1). FBLC can be a frequency limited buffer. As shown by Fig. 5, the input noise was attenuated at a higher frequency than the peak gain frequency. This confirms the high robustness of the design of this structure.

2.3 LDO with FBLC

Figure 6 shows the LDO with FBLC. The proposed LDO is composed of a conventional LDO, FBLC, inverter, voltage-controlled switch, and constant current source. The constant current sources I_{tailB} and I_{tailA} are 28 μA and 60 nA, respectively. The conventional LDO was composed of a pass transistor Mpass, an amplifier AMP, and compensate devices C_c and R_c with divider resistances R_{f1} and R_{f2}, respectively. C_{out} and R_e refer to the output capacitor and were equivalent to its series resistance.

The input of the FBLC was connected to Vout of the

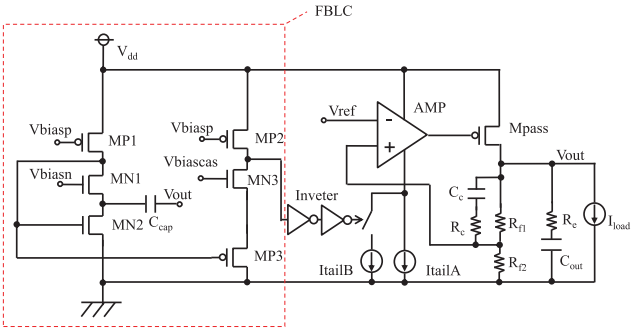


Fig. 6 LDO with FBLC

LDO through C_{cap}. When Iload changes suddenly, the voltage of node E in Fig. 4 changes promptly and is detected by an inverter. The detected voltage turns on the voltage-controlled switch. As a result, constant current source I_{tailB} is added as a quiescent current of the amplifier. Therefore, the f_u of the LDO can be extended by increasing the quiescent current of amplifier. This is a mechanism for improving the load transient response. Constant quiescent current of the proposed circuit remained in the nA order, because it increases only when output undershoot occurs.

3. Simulation Results

The proposed LDO was designed based on a 0.6 μm CMOS technology. Simulation conditions were V_{dd} = 2.2 V, V_{out} = 1.2 V, C_{cap} = 1 pF, I_{tailA} = 60 nA, I_{tailB} = 28 μA, C_{out} = 1 μF, and R_e = 15 mΩ. In addition, I_{load} = 10 mA for the AC simulation, I_{load} = 100 μA to 10 mA, and SR = 1 μs for the transient simulation. Quiescent current of the FBLC was 50 nA. Characteristics of the new and conventional LDOs are compared in the following section. Figure 7 shows the circuit structure of the conventional LDO and the tail current Itail. Table 1 shows the changed parameters of the amplifiers.

Figure 8 and Table 2 summarize the AC simulation results when load current is 10 mA. The f_u of LDO with FBLC was 2.6 kHz and the phase margin was 84°. Because FBLC does not work under DC operation, the f_u of the proposed LDO was the same as that of the conventional LDO A. An LDO with FBLC can respond to a voltage signal of approximately 50 kHz, as shown in Fig. 5 and Fig. 8, because of the increase of quiescent current as a function of FBLC.

Figure 9 and Fig. 10 show wave forms and performance comparison of the proposed and conventional LDOs in a transient simulation. Table 3 summarizes the simulation results. The conditions of the transient simulation were based on a current profile of an ultra-low quiescent current MCU [2]. The undershoot of the proposed LDO was 70 mV, under the load transient condition of I_{load} = 1 μA to 10 mA and SR = 1 μs. This shows an 89% improvement from the conventional LDO A, whose tail current was the same as that of the proposed LDO. Settling time, which is $V_{out} \pm 3\%$, was 25 μs, exhibiting a 94% improvement from the con-

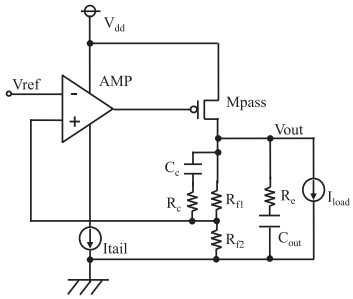


Fig. 7 Circuit structure of conventional LDO

Table 1 Specification of conventional LDOs

Parameter	*Itail*(nA)
LDO A	60
LDO B	600
LDO C	6000
LDO D	60000

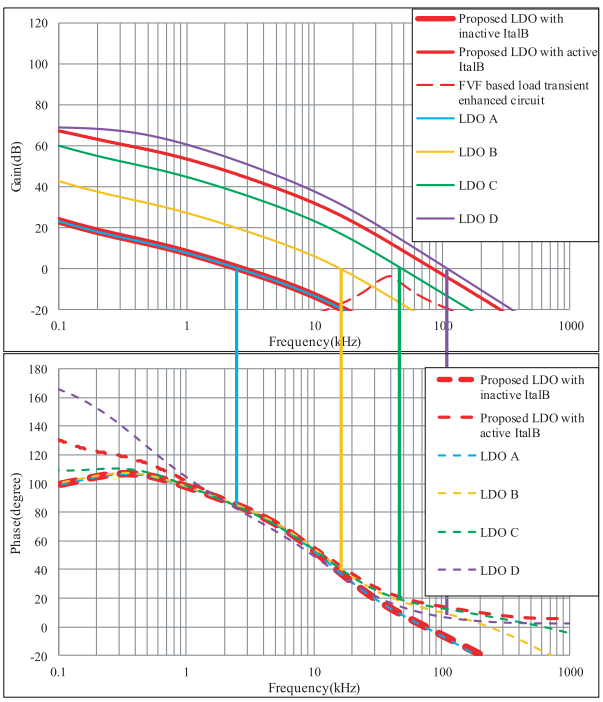


Fig. 8 Wave form of AC simulation result

Table 2 Summary of AC simulation results

Parameter	Unity gain frequency (kHz)	Phase margin (degree)
Proposed LDO with inactive ItaIB	2.6	84
Proposed LDO with active ItaIB	83	16
LDO A	2.6	84
LDO B	16	37
LDO C	49	19
LDO D	110	13

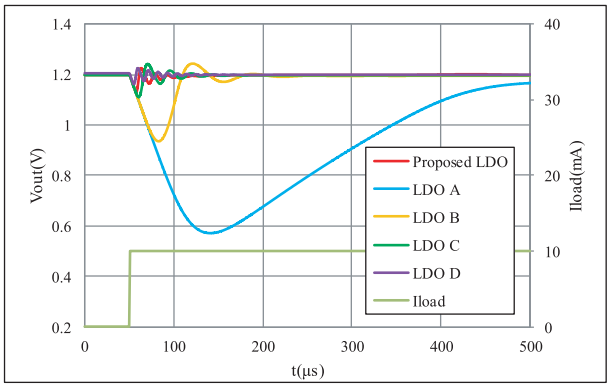


Fig. 9 Wave form of proposed LDO and conventional LDOs (I_{load} = 1 μA to 10 mA and SR = 1 μs)

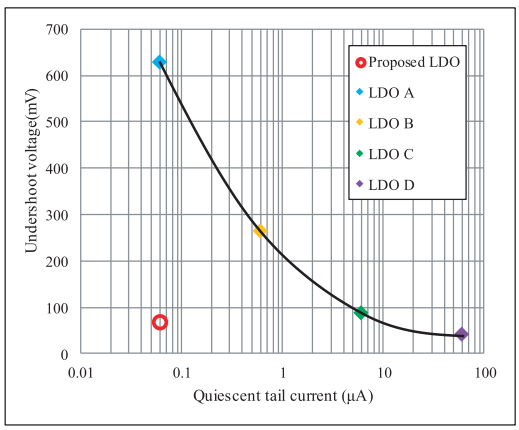


Fig. 10 Performance comparison of the proposed and conventional LDO in a transient simulation

Table 3 Summary of transient simulation results

Parameter	Under shoot (mV)	Settling time (μs)
Proposed LDO	70	25
LDO A	630	430
LDO B	260	80
LDO C	90	35
LDO D	45	5

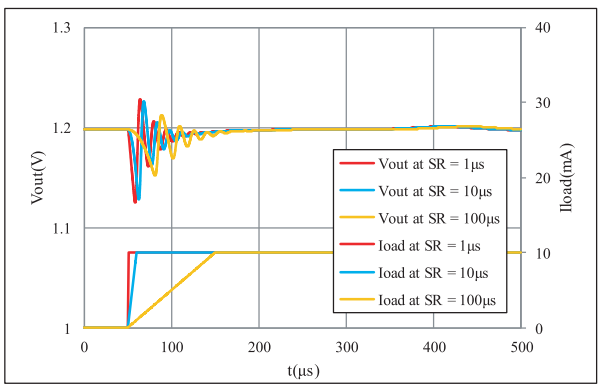


Fig. 11 Wave form of proposed LDO (I_{load} = 1 μA to 10 mA, SR = 1 μs, 10 μs and 100 μs)

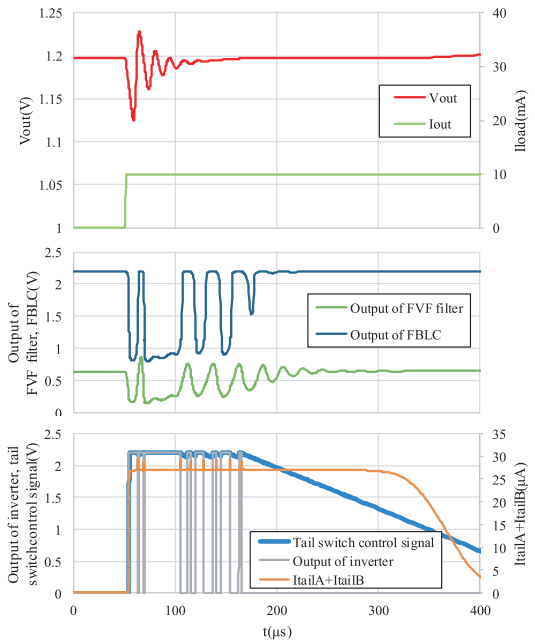


Fig. 12 Wave form of load transient simulation (I_{load} = 1 μA to 10 mA and SR = 1 μs)

ventional LDO A. In the system of WSN, stand by cycle is much longer than active cycle. Therefore, temporary increase of current does not make much influence on battery life. Figure 11 shows wave form of proposed LDO with different Iload SR. The proposed LDO has a good performance regardless of Iload SR. When ItailB is active, phase margin decreases from 84° to 16°, which is still enough value to keep stability. Table 2, Fig. 9 and Fig. 12 show the output voltage of proposed LOD is still stable during changing tail current.

4. Experimental Results and Discussion

In this paper, the proposed LDO was fabricated in a 0.6 μm CMOS process. Figure 13 shows the die of the designed LDO. The chip area was 0.72 mm × 0.81 mm, including the pads.

Experimental conditions were V_{dd} = 2.2 V, V_{out} = 1.2 V, C_{out} = 1 μF, I_{load} = 1 μA to 10 mA, and I_{load} = 100 μA to 10 mA. Figure 14 shows the transient experimental wave forms of the designed LDO.

Under the load transient conditions of SR = 1 μs and I_{load} = 1 μA to 10 mA, the designed LDO achieved an undershoot of 100 mV, which was fully recovered to 3% within 28 μs. Moreover, it achieved an undershoot of 75 mV, which was fully recovered to 3% within 26 μs under the load transient conditions of SR = 1 μs and I_{load} = 100 μA to 10 mA. The quiescent current was 204 nA with zero Iload under the DC operation. The difference between the simulation and experimental results were caused by the inaccurate parasitic capacitances that occur between the P-sub and the metal wire in the silicon chip. Especially, the capacitance from the node of FVF filer output to the ground affects load

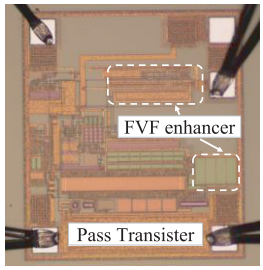
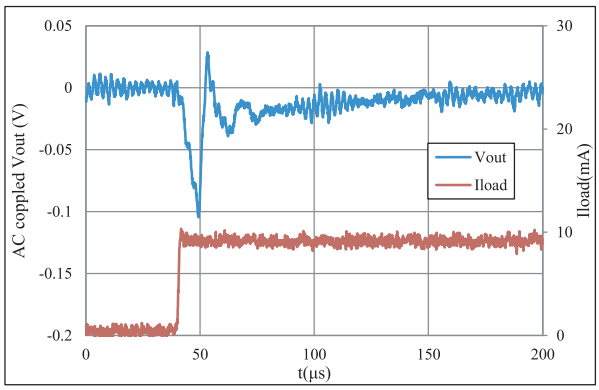
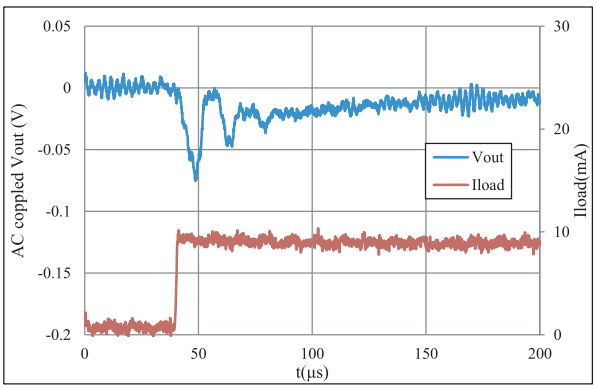


Fig. 13 Die of the proposed LDO



(a) I_{load} = 1 μA to 10 mA



(b) I_{load} = 100 μA to 10 mA

Fig. 14 Transient experimental wave forms of the proposed LDO

transient characteristics. In this case, increasing parasitic capacitance increases C_{load} in Fig. 1, which decreases the f_u of the FBLC. This degradation occurs because of parasitic capacitances, which can be improved with changes in the circuit layout. We can avoid from this degradation with using specific metal layers which is not near to the ground.

5. Conclusion

This paper proposes an ultra-low quiescent current LDO with an FVF-based load transient enhanced circuit for WSN. The proposed LDO was fabricated in a 0.6 μm CMOS process, simulated, and evaluated. The LDO with FBLC achieved an undershoot of 75 mV under experimental con-

ditions with a large load transient of 100 μA to 10 mA and current SR of 1 μs. Quiescent current was found to be 204 nA at no Iload. LDO with FBLC achieved better characteristics, with the tail current of the amplifier at 60 nA, compared to the conventional LDO. The results confirm that the proposed LDO could be a suitable solution for issues in WSNs.

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