PAPER

Post-Packaging Simulation Based on MOSFET Characteristics Variations Due to Resin-Molded Encapsulation

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SUMMARY A method for estimating circuit performance variation caused by packaging-induced mechanical stress is proposed. The developed method is based on the stress distribution chart for the target integrated circuit (IC) and the stress sensitivity characteristics of individual devices. This information is experimentally obtained using a specially designed test chip and a cantilever bending calibration system. A post-packaging analysis and simulation tool, called Stress Netlist Generator (SNG), is developed for conducting the proposed method. Based on the stress distribution chart and the stress sensitivity characteristics, SNG modifies the SPICE model parameters in the target netlist according to the impact of the packaging-induced stress. The netlist generated by SNG is used to estimate packaging-induced performance variation with high accuracy. The developed method is remarkably effective even for small-scale ICs with chip sizes of roughly 1 mm^2, such as power management ICs, which require higher precision.

key words: *stress, piezoelectric, package, simulation, SPICE*

1. Introduction

The Internet of Things (IoT), a system of connected computing devices, has been applied in smart homes, where consumer electronic appliances are connected through a network, and production lines for manufacturing. It is estimated that in the 2020s, more than 40 billion devices will be mutually connected and that the amount of network traffic will be more than 1,000 times larger than current traffic. It is a challenge to further increase the traffic volume for transmission requirements [1].

To create a variety of IoT services and realize diversified networks with an enormous number of IoT devices, it is necessary to facilitate installation and long-term operation with a simple power supply method for IoT devices.

To make installation easier, components can be made smaller and more lightweight. For IoT devices to operate stably over long periods, power consumption must be low and circuit performance must be accurate. For IoT equipment to spread, it is necessary to make integrated circuits (ICs) small and highly precise [2].

A schematic diagram of typical IoT equipment is shown in Fig. 1. For sensing devices, such as surveillance cameras and sensors that detect environmental conditions (e.g., temperature, pressure, and carbon dioxide levels),

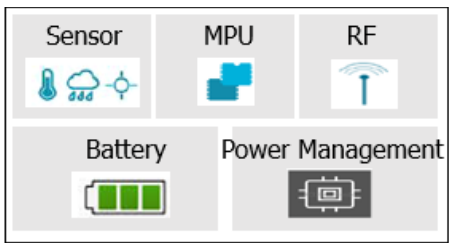

Fig. 1 Schematic diagram of typical IoT equipment.

complementary metal-oxide semiconductor (CMOS) image sensors must be small and highly accurate. These requirements also apply to microprocessing units (MPUs), which analyze the data obtained from the sensor device, and wireless communication devices, which transmit analysis results to a server. Miniaturization and high accuracy are also important for power management ICs, which supply electric power to individual electronic circuits [3].

IC miniaturization is driven by microfabrication technology in semiconductor manufacturing. State-of-the-art ICs are manufactured based on nanometer-scale nodes [4]. Processing precision has improved with progress in microfabrication technology. To improve the matching characteristic for analog circuits, measures such as increasing the circuit size have been applied to minimize the effects of the process variation of individual devices [5].

Performance variation introduced by the resin-molded packaging process is an inherent obstacle for high-precision ICs. Resin molding has a large thermal expansion coefficient, which causes volume shrinkage during its formation, which in turn generates compressive stress on the IC surface. Due to this residual stress, semiconductor devices in an electronic circuit cause variation due to the piezo effect, shifting circuit performance from the target value [6]. The packaging process thus affects circuit performance. Since current ICs are designed using SPICE model parameters extracted from the condition of the wafer, this performance variation is not taken into account. There have been few reports on the performance variation of small-scale ICs, such as power management ICs, despite their requirement of high precision.

This study proposes a method for estimating circuit performance variation caused by packaging-induced mechanical stress. The developed method is based on the stress distribution chart for the target IC and the stress sensitivity characteristics of individual devices. This information is

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experimentally obtained using a specially designed test chip and a cantilever bending calibration system. To realize the proposed method, a specific tool called Stress Netlist Generator (SNG) is developed. Based on the stress distribution chart and stress sensitivity characteristics, SNG modifies the specified model parameters of SPICE in the target netlist according to the impact of the packaging-induced stress.

This study shows that circuit performance variation caused by packaging-induced mechanical stress can be estimated with high accuracy. In addition, a method for visualizing the stress distribution chart for small-scale ICs is developed.

2. Methodology

Figure 2 shows an outline of the proposed method for estimating circuit performance variation caused by packaging-induced mechanical stress. In the conventional method, layout is conducted after circuit design using SPICE simulation. Based on the layout data, a Graphic Data System (GDS) file is generated to make photolithography masks for mass production. Then, parasitic data are extracted from the GDS file using a commercially available tool, such as Calibre-xRC.

The parasitic resistance and capacitance physically generated by the layout of the electronic circuit are considered. The extracted parasitic data are output as a file called a netlist (original netlist), with the type of device and its connection information included. Then, SPICE simulation is carried out again using the netlist to confirm that the target characteristics are realized.

This method is generally called post-layout simulation because it can take into account the influence of parasitic parameters generated by the layout. In addition, since the SPICE model parameters used in this conventional method are extracted from the condition of the wafer, stress-induced performance variations after packaging are not taken into consideration. To estimate stress-induced performance variations after packaging, a method for calculating the stress-induced variation of individual devices and reflecting it in the netlist is proposed here.

A specific tool (SNG) that can generate a netlist reflecting the stress-induced effects is also developed.

SNG has the following functions. It can extract coordinate information for individual devices from the GDS file. This information is used to specify the value of stress applied to each device. SNG can also extract the direction of each device from the GDS file. This information is used to calculate the amount of change in electrical characteristics caused by stress.

SNG requires two types of information. One is the stress distribution chart of the chip surface of the target IC (see Sect. 3.3 for details). SNG uses this information as input data to determine the magnitude of stress at the coordinate position of the device extracted in advance. The other is the stress sensitivity characteristics of the individual devices that constitute the target IC (see Sect. 3.4 for details).

SNG uses the stress sensitivity characteristics as input data to calculate the stress-induced variation of each device based on the stress applied to the device and the device direction (see Sect. 3.5 for details).

As described above, with the stress distribution chart and the stress sensitivity characteristics as input data, it is possible to calculate the amount of stress-induced performance variation for each device from the coordinates and the direction of the device. In this study, stress-induced variations are calculated for MOSFETs and resistors. In addition, a mobility value for a MOSFET and a resistance value for a resistor are selected as the characteristic parameters that reflect the influence of stress.

After the above procedure, SNG modifies the model parameters for each device in the netlist (original netlist) extracted using the conventional design method. Even for devices of the same type and the same dimensions, the model parameters are rewritten based on the coordinates and direction of the device. As a result, a new netlist that reflects the stress-induced effects is generated (see Sect. 3.6 for details).

SPICE simulation was performed using the SNG-generated netlist to simulate circuit performance after packaging.

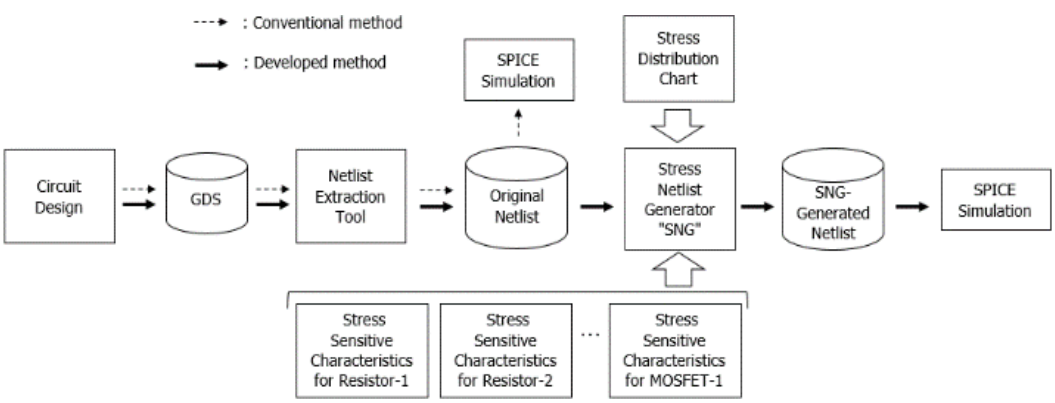

Fig. 2 Outline of methodology for estimation of stress-induced performance variation.

3. Proposed Scheme

3.1 Test Chip

To visualize the stress distribution chart for a small-scale IC, a specially designed test chip was developed. The test chip, shown in Fig. 3 [7], has the same outline as that of the target small-scale IC because the stress-induced variation of an actual small-scale IC can be accurately measured. A small-scale IC has a limited number of bonding pads, which means that only a single piezoelectric resistor can be mounted on a single test chip.

The following technique was used for evaluating the stress distribution chart for the entire surface of the chip. First, multiple test chips with different piezoelectric resistor positions were fabricated and their resistance values were measured before and after packaging. The measurement data for given test chips have die-to-die correspondence. The data from the different test chips are displayed simultaneously in the area of a single chip. This method allows the variation distribution on the chip surface of a small-scale IC to be obtained with only four pins (Fig. 4).

Second, to realize high accuracy for each measurement, a four-point Kelvin resistance measurement was performed to avoid other disturbance factors [8]. The sensor comprised p- and n-type implanted resistors embedded in the (100) crystallographic plane of a silicon chip, as shown in Fig. 5.

Third, since the size of a small IC is roughly 1.0 mm^2, the incorporated piezoelectric resistor should be sufficiently small compared to the entire chip. A piezoelectric resistor is approximately 0.03 mm in length and 0.002 mm in width (Fig. 6). The terminal numbers 1, 2, 3, and 4 in Fig. 6 correspond to the terminal numbers 1, 2, 3, and 4 in Fig. 5, respectively. The resistance value was measured under a 23.0 ± 0.5°C isothermal environment, as shown in Fig. 7.

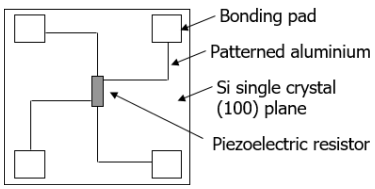

Fig. 3 Diagram of test chip.

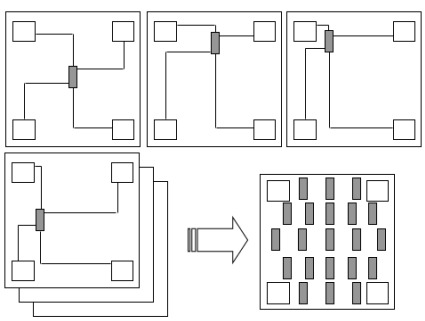

Fig. 4 Principle of multiple-point measurements.

3.2 Calibration

A Cantilever bending calibration system was applied to calibrate the response of the piezoelectric resistors (Fig. 8). The load stress was controlled via the intensity of the load cell. By pushing or pulling the silicon beam, it is possible to ap-

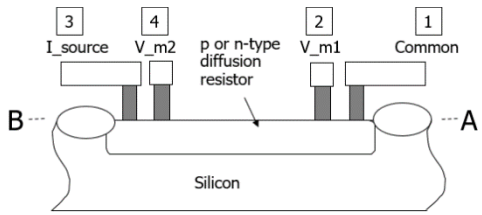

Fig. 5 Cross-section view of piezoelectric resistor.

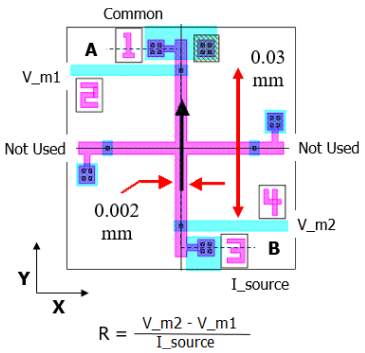

Fig. 6 Plan view of piezoelectric resistor.

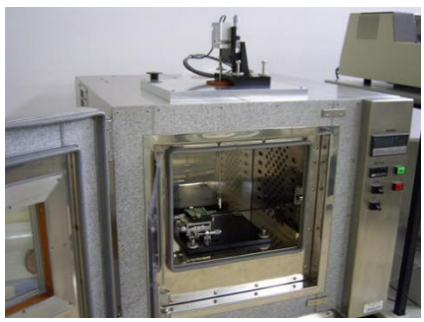

Fig. 7 Photograph of isothermal environment chamber.

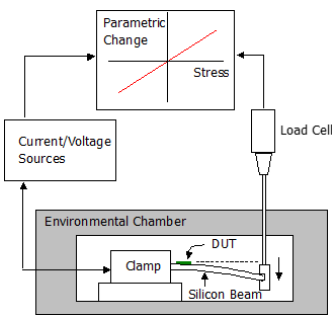

Fig. 8 Cantilever bending calibration system.

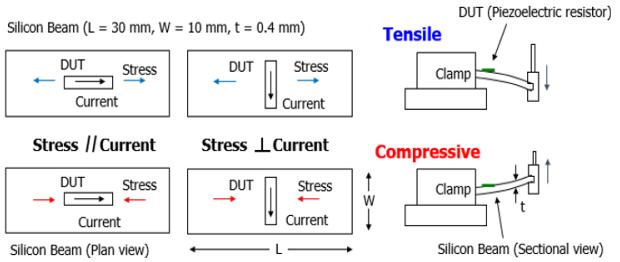

Fig. 9 Cantilever technique for extraction of piezoelectric resistance coefficient.

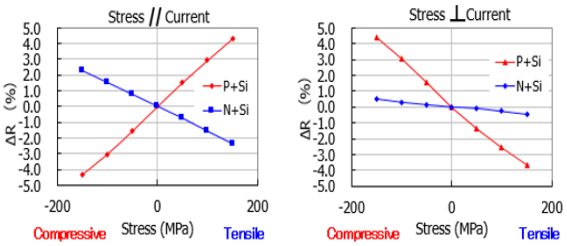

Fig. 10 Calibration results for p- and n-type piezoelectric resistors.

ply tensile or compressive stress to the target device under test (DUT), as shown in Fig. 9. There are two types of configuration for stress and current direction in a DUT, namely Stress // Current and Stress ⊥ Current.

Each piezoelectric resistance coefficient, π_{ij}, for the p- and n-type piezoelectric resistors was experimentally extracted through the controlled application of a uniaxial loading. The calibration results for the p- and n-type piezoelectric resistors are shown in Fig. 10.

R^N and R^P are the resistance values of the n- and p-type piezoelectric resistors, respectively. ΔR is the variation of the resistance value measured between in the wafer and package conditions. Then, the x- and y-direction stress components (S_x and S_y, respectively) can be calculated by algebraic manipulation using the following equations [9].

$$\frac{\Delta R^N}{R^N} = \left(\frac{{\pi_{11}}^N + {\pi_{12}}^N - {\pi_{44}}^N}{2}\right) S_x + \left(\frac{{\pi_{11}}^N + {\pi_{12}}^N + {\pi_{44}}^N}{2}\right) S_y \quad (1)$$

$$\frac{\Delta R^P}{R^P} = \left(\frac{{\pi_{11}}^P + {\pi_{12}}^P - {\pi_{44}}^P}{2}\right) S_x + \left(\frac{{\pi_{11}}^P + {\pi_{12}}^P + {\pi_{44}}^P}{2}\right) S_y \quad (2)$$

3.3 Stress Distribution Chart

Figure 11 shows an overview of a target small-scale IC with a chip size of 1.3 mm × 1.3 mm. The IC is a power management chip for white light-emitting diode (LED) applications for smartphones. It has 4-channnel LED driver circuits (LED-1, LED-2, LED-3, and LED-4), a 1-MHz oscillator circuit (OSC) for charge pumping control and logic control, a thermal shutdown circuit (TSHUT), and a reference current source circuit (IREF) in addition to the control logic circuits. To clarify the stress distribution for the target IC,

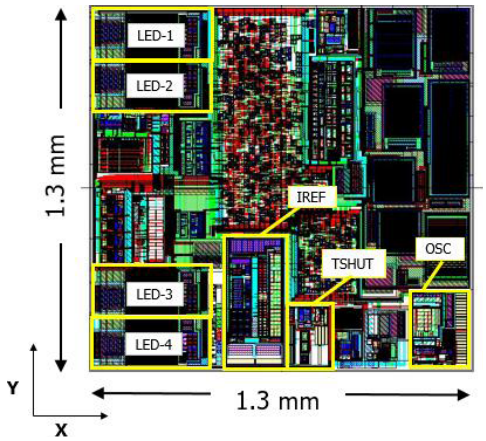

Fig. 11 Overview of the target small-scale IC.

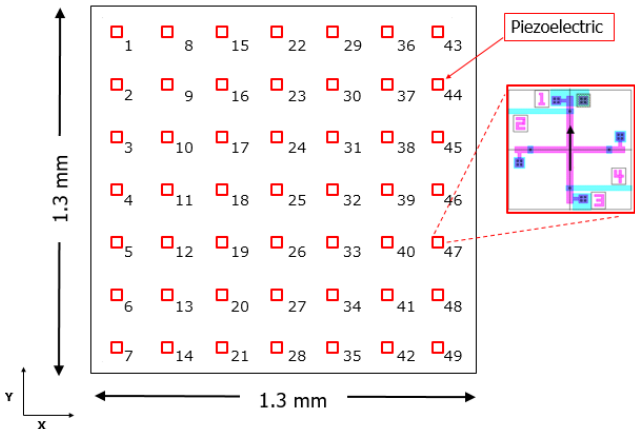

Fig. 12 Test chip with 49 piezoelectric resistors.

a test chip with 49 piezoelectric resistors arranged in a grid pattern was prepared, as shown in Fig. 12. The stress distribution chart for the entire chip surface can be visualized using the methodology shown in Fig. 4.

The stress distribution charts for the x- and y-direction stress components (S_x and S_y, respectively) for a 1.3 mm × 1.3 mm test chip are shown in Fig. 13. The compressive stresses are greatest at the center of the chip and gradually decrease toward the edges. The maximum stress value is approximately 100 MPa for both the x- and y-direction components.

3.4 Stress Sensitivity Characteristics of Each Device

To simulate the stress-induced performance variation for the target small-scale IC shown in Fig. 11, the stress sensitivity characteristics of each device in the IC were extracted using the cantilever technique shown in Fig. 9. The target IC has two types of MOSFET and three types of resistor. The stress sensitivity characteristics of MOSFETs and resistors are shown in Figs. 14 and 15, respectively. Transconductance G_m was measured instead of mobility, which is described in SPICE model parameters. Other types of de-

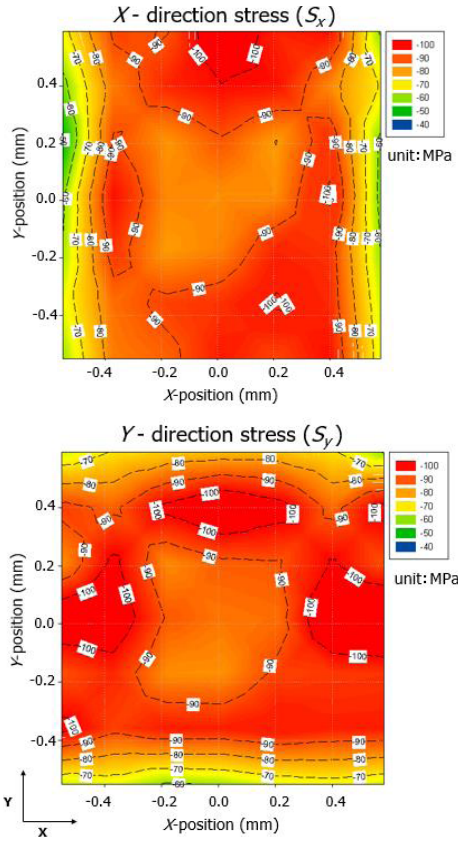

Fig. 13 Stress distribution charts of the x- and y-direction stress components.

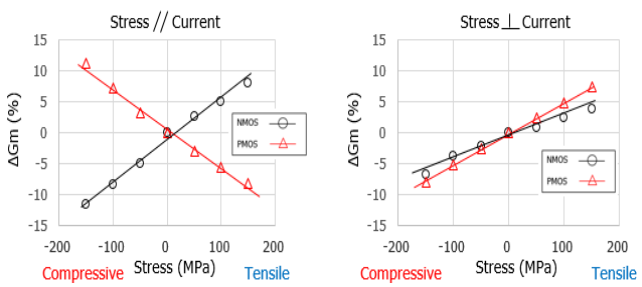

Fig. 14 Stress sensitivity characteristics of MOSFETs.

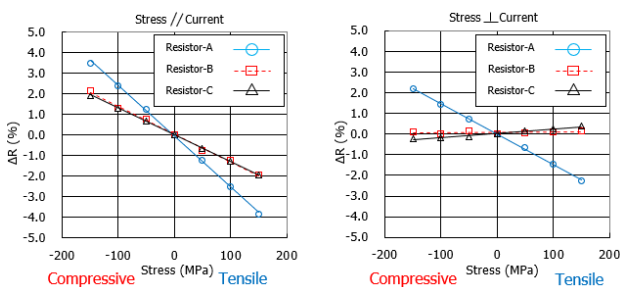

Fig. 15 Stress sensitivity characteristics of resistors.

vice, such as diodes and capacitors, and metal wiring are not considered in the stress-induced variation calculation.

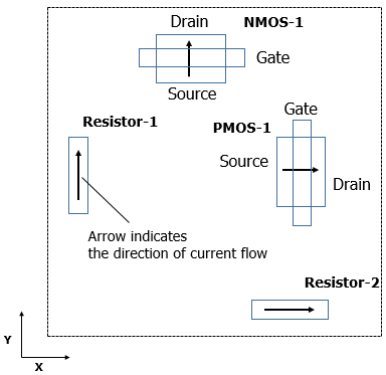

Fig. 16 Example of individual devices with different directions of current flow.

3.5 Estimation of Stress-Induced Variation

The stress-induced variation of each device in the IC was calculated using the stress distribution charts shown in Fig. 13 and the stress sensitivity characteristics shown in Figs. 14 and 15.

The formula is a linear combination of x- and y-direction stresses acting independently [10]. For MOSFETs in the IC, the transconductance G_m is modified as described below. NMOS-1, whose current is parallel to the y-axis, and PMOS-1, whose current is parallel to the x-axis, are used (Fig. 16). Attention must be paid to the current direction of the target device.

$$\begin{aligned}&\Delta G_{\mathrm{m}}(\text{NMOS-1})\\&= \text{gradient}\ \Delta G_{\mathrm{m}}(\text{Stress // Current}) \times Sy\\&\quad + \text{gradient\_}\Delta G_{\mathrm{m}}(\text{Stress} \perp \text{Current}) \times Sx\end{aligned} \tag{3}$$

$$\begin{aligned}&\Delta G_{\mathrm{m}}(\text{PMOS-1})\\&= \text{gradient}\ \Delta G_{\mathrm{m}}(\text{Stress // Current}) \times Sx\\&\quad + \text{gradient\_}\Delta G_{\mathrm{m}}(\text{Stress} \perp \text{Current}) \times Sy\end{aligned} \tag{4}$$

Here, ΔG_{m} (NMOS-1) is the change rate when stress is applied to NMOS-1. Gradients ΔG_{m} (Stress // Current) and ΔG_{m} (Stress $\perp$ Current) are the slopes of the stress sensitivity characteristics (Stress // Current) and (Stress $\perp$ Current), respectively, which are extracted from Fig. 14.

The resistance value of resistors is modified. The calculation method is shown below. Resistor-1, whose current is parallel to the y-axis, and Resistor-2, whose current is parallel to the x-axis, are used (Fig. 16).

$$\begin{aligned}\Delta\mathrm{R}(\text{Resistor-1}) = {}&\text{gradient}\ \Delta\mathrm{R}(\text{Stress // Current}) \times Sy\\&+\text{gradient\_}\Delta\mathrm{R}(\text{Stress} \perp \text{Current}) \times Sx\end{aligned} \tag{5}$$

$$\begin{aligned}\Delta\mathrm{R}(\text{Resistor-2}) = {}&\text{gradient\_}\Delta\mathrm{R}(\text{Stress // Current}) \times Sx\\&+\text{gradient\_}\Delta\mathrm{R}(\text{Stress} \perp \text{Current}) \times Sy\end{aligned} \tag{6}$$

Here, ΔR (Resistor-1) is the change rate when stress is applied to Resistor-1. Gradients ΔR (Stress // Current) and

ΔR (Stress $\perp$ Current) are the slopes of the stress sensitivity characteristics (Stress // Current) and (Stress $\perp$ Current), respectively, which are extracted from Fig. 15. The current direction of the device is considered.

The stress value applied to each device was calculated via interpolation using data for the four grids around each device (Fig. 17).

3.6 Modification of Netlist

The netlist is modified using the results of the stress-induced variation calculated using the above procedure. The modification of the netlist is as follows.

For MOSFETs, transconductance G_{m} is derived from the effective mobility (*Ueff*), which is expressed in the user manual for SPICE model BSIM3 as follows [11]:

$$Ueff = \frac{U0}{1 + Ua\left(\frac{Vgs + Vth}{Tox}\right)} \tag{7}$$

where *U0* is the mobility, *Ua* is the first-order coefficient of mobility degradation, *Vgs* is the applied voltage on the gate terminal, *Vth* is threshold voltage of the MOSFET, and *Tox* is the thickness of the gate oxide film. MULU0 is defined as a coefficient of variation with respect to the SPICE model parameter *U0*. That is, the change in mobility *U0* due to stress is treated as MULU0 in this study.

SNG executes a process that reflects ΔG_{m} as MULU0.

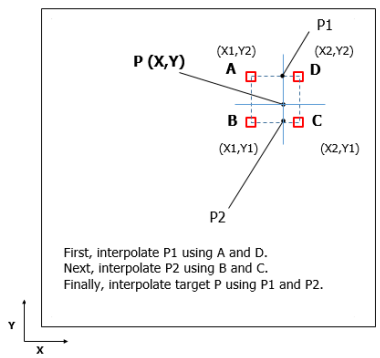

Fig. 17 Example of interpolation using data for four grids.

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M1 n1 n2 n3 n4 NM L=1e-06 W= 8e-06 AS= 8e-12 PD= 8.6e-06
 + MULU0=0.9724052
 +  $X=-61.8 $Y=-192.6 $DIRECTION=X

R1 r1 r2
 + 409.336
 + $X=247.3 $Y=205.2 $DIRECTION=Y
```

Upper is for a MOSFET, Lower for a resistor
The 1st line : General device description
The 2nd line : Calculated value of mobility or resistance after packaging
The 3rd line : Coordinates and direction for device

Fig. 18 Example of modified description in netlist.

That is, by using MULU0 as an additional value in the description of the MOSFETs in the netlist, the mobility of the MOSFETs is modified to a new value after variation due to stress. By performing such processing for all MOSFETs in the netlist, the stress-induced variation is obtained for each MOSFET.

SNG executes processing to modify the resistance value of the resistors. That is, in the netlist, the resistance value changed by stress is added as a new quantitative value. By performing such processing for all resistors in the netlist, the stress-induced variation is obtained for each resistor.

Figure 18 shows an example of a SNG-modified description in a netlist. Through the above operations, the information in the netlist is updated from post-layout to post-packaging.

4. Results

The evaluation was executed for four types of analog circuit in the target small-scale IC, namely LED driver circuits (LEDs), a 1-MHz oscillator circuit (OSC), a thermal shutdown circuit (TSHUT), and a reference current source circuit (IREF). In this study, the current value for each LED, the switching frequency value for OSC, the thermal protection voltage value for TSHUT, and the current value for IREF are evaluated.

Table 1 lists the comparison results for the target circuits. The results of simulation using SNG are shown in the column "Simulated", and those of the measurements of the manufactured IC are shown in the column "Measured".

The measurement data for given test chips have die-to-die correspondence. This means that perfect traceability between before and after packaging is achieved.

Figure 19 shows the variation rates for the target circuits. The simulation results are in good agreement with the measurement results for all types of analog circuit in the target IC.

All LEDs show a negative shift after packaging. LEDs have a wide channel width in their n-channel MOSFETs to distribute drive current. In addition, since the G_m of n-channel MOSFETs degrades under a compressive stress field, as shown in Fig. 14, the current value for each LED decreases after packaging. IREF shows the largest shift after packaging. This is likely due to IREF being located in the center area of the chip, where compressive stress is largest, as shown in Fig. 13. In contrast to IREF, OSC is located at

Table 1 Comparison of simulation and measurement results for the target circuits.

			Simulated			Measured		
Target circuit		Unit	Original	SNG-generated	Variation (%)	Wafer	Package	Variation (%)
LED	ch1	mA	23.21	22.80	-1.77%	24.02	23.63	-1.60%
	ch2	mA	23.21	22.73	-2.05%	24.05	23.66	-1.64%
	ch3	mA	23.21	22.78	-1.86%	24.05	23.64	-1.68%
	ch4	mA	23.21	22.75	-2.01%	24.05	23.68	-1.57%
OSC		MHz	1.000	0.988	-1.24%	1.08	1.07	-1.23%
TSHUT		mV	0.976	0.977	0.18%	0.96	0.97	0.53%
IREF		µA	2.010	1.967	-2.14%	2.13	2.08	-2.22%

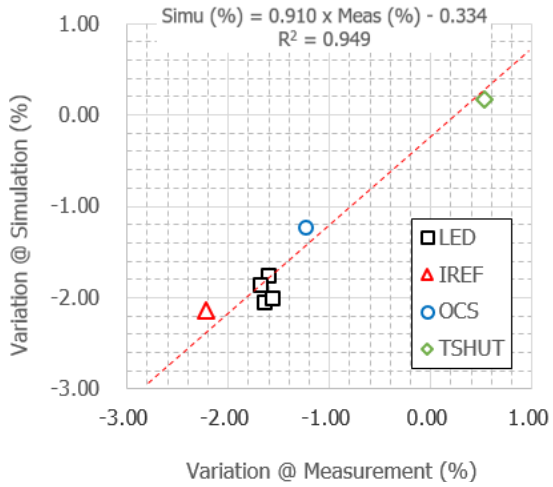

Fig. 19 Comparison between simulation and measurement results.

the corner of the chip, where the *x*- and *y*-direction stresses are small, and thus its performance variation is suppressed. TSHUT shows a smaller shift compared to those of the other three circuits.

5. Conclusions

A method for estimating circuit performance variation caused by packaging-induced mechanical stress was developed. The method is based on the stress distribution chart for the target IC and the stress sensitivity characteristics for individual devices. A tool called SNG was also developed. Based on the stress distribution chart and stress sensitivity characteristics, SNG modifies the SPICE model parameters in the target netlist according to the impact of stress intensity. By using the netlist generated by SNG, packaging-induced performance variation can be estimated with high accuracy. The simulation results are in good agreement with the measurement results for four types of analog circuit in the target IC. The developed method is remarkably effective even for small-scale ICs with chip sizes of roughly 1 mm^2, such as power management ICs, which require higher precision.

References

[1] S. Talwar, D. Choudhury, K. Dimou, E. Aryafar, B. Bangerter, and K. Stewart, "Enabling technologies and architectures for 5G wireless," IEEE MTT-S International Microwave Symposium, 2014.
[2] M.T. Lazarescu, "Design of a WSN Platform for Long-Term Environmental Monitoring for IoT Applications," IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol.3, no.1, pp.45–54, March 2013.
[3] M.O. Onibonoje, O.F. Ikpeze, and C.C. Ibenegbu, "Development of a wireless sensor network for monitoring an automated distributed water supply system," ABUAD Journal of Engineering Research and Development (AJERD), vol.1, no.1, pp.23–31, 2017.
[4] C. Auth, A. Aliyarukunju, and M. Asoro, "A 10nm high performance and low-power CMOS technology featuring 3rd generation FinFET transistors, Self-Aligned Quad Patterning, contact over active gate and cobalt local interconnects," IEEE International Electron Devices Meeting, pp.673–676, 2017.
[5] M.J.M. Pelgrom, A.C.J. Duinmaijer, and A.P.G. Welbers, "Matching Properties of MOS Transistors," IEEE J. Solid-State Circuits, vol.24, no.5, pp.1433–1440, Oct. 1989.
[6] H. Ali, "Stress-induced parametric shift in plastic packaged devices," IEEE Trans. Compon., Packag., Manuf. Technol. B, vol.20, no.4, pp.458–462, Nov. 1997.
[7] N. Ueda, E. Nishiyama, H. Aota, and H. Watanabe, "Evaluation of Packaging-induced Performance Change for Small-scale Analog IC," IEEE Trans. Semicond. Manuf., vol.22, no.1, pp.103–109, Feb. 2009.
[8] S.A. Gee, V.R. Akylas, and W.F. van den Bogert, "The Design and Calibration of a Semiconductor Strain Gauge Array," IEEE Proc. on Microelectronic Test Structures, vol.1, no.1, Feb. 1988.
[9] Y. Tanimoto, T. Toriyama, and S. Sugiyama, "Characteristics of Polycrystalline Si Nano Wire Piezoresistors," IEEJ Transactions on Sensors and Micromachines, vol.121, no.4, pp.209–214, 2001.
[10] Y. Han, M. Koganemaru, T. Ikeda, N. Miyazaki, K. Yamakuchi, W. Choi, and H. Tomokage, "Effects of uni-axial mechanical stress on the scattering parameters of metal oxide semiconductor field effect transistors," ICEP Proc., 2009.
[11] http://semicon.jeita.or.jp/book/docs/design_for_manufacturabilit.pdf

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