FOREWORD

Special Section on Low-Power and High-Speed Chips

Low-power and high-speed chips (Cool Chips) encompass a broad range of architectures, applications, methodologies, and usage models. These technologies are present not only in multimedia, digital consumer electronics, mobile, graphics, encryption, robotics, networking, and biometrics, but also in the peta-scale computers. They are based on multiprocessing, reconfigurable computing, dependable computing, and memory architectures. Cool software, which includes parallel schedulers and compilers, is also emerging.

These technologies all aim to reduce power consumption and enhance chip performance. Regardless of their goals, all of industry has been challenged with developing optimal solutions - both hardware and software - for power optimization according to the required performance. In general, in an attempt to migrate decades worth of legacy approaches to low-power technology, industry approaches these optimal solutions from the perspective of starting from scratch.

With this in mind, we've been organizing annual Cool Chips conferences since 1998. And in April 2017, we celebrated Cool Chips' 20th anniversary as "COOL Chips 20". COOL Chips, a sister conference of Hot Chips, focuses on all aspects of cool technologies. Approximately 120 individuals attended to COOL Chips 23 virtually held in April 2020, despite the severe situation by COVID-19. In addition to regular paper presentations, COOL Chips 23 included keynote and invited talks, special topic sessions, and poster discussions. To attract submissions from engineers working in industry, the program committee bases acceptance on a short abstract. The conference proceedings include only the short abstract with the final presentation rather than a set of long papers.

It is our great honor to announce the publication of this special section on Low-Power and High-Speed Chips. The section is devoted to variety of techniques for COOL Chips. It contains 5 papers, among 6 submissions, which covers, a firmware update in flash memory, non-volatile Flip Flops, an area-efficient RNN core, power constrained HPC systems, and a distributed DNN training.

On behalf of the editorial committee, we would like to express our sincere appreciation to all the authors for their contributions and to all the reviewers for their critical reviewing papers. Lastly, We would like to thank the editorial committee for their work on this special section, especially, secretaries: Prof. Wada and Prof. Egawa.

Fumio Arakawa and Makoto Ikeda, Guest Editors

Fumio Arakawa *(Senior Member)* is a designated professor of Graduate School of Informatics at Nagoya University, and a designated researcher of Engineering School at the University of Tokyo. His research interests include architecture and micro-architecture of low-power and high-performance microprocessors. Arakawa has a PhD in electrical engineering from the University of Tokyo. He is a program committee co-chair of the Cool Chips conference series, and the chairman of Microprocessor Technical Committee of JEITA. He served as a Guest Editor for IEEE Micro for six times, and TPC members of conferences including ISSCC, VLSI Circuits Symposium, A-SSCC, and MCSoC.

Makoto Ikeda *(Senior Member)* is a professor in Systems Design Lab., Engineering School, at the University of Tokyo. His research interests include high-performance, low-power, and reliable digital circuit and smart image sensor design. He is a program committee co-chair of the Cool Chips conference series, and a program committee vice chair of the International Solid-State Circuits Conference (ISSCC 2020), Symposium chair (2019) and Program chair (2017) of VLSI Circuits Symposium, Program chair (2015) of Asian Solid-State Circuits Conference, and several others. Ikeda has a PhD in electrical engineering from the University of Tokyo.