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Design and Integration of Beyond-10MHz High Switching Frequency DC-DC Converter

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SUMMARY There are continuous and strong demands for the DC-DC converter to reduce the size of passive components and increase the system power density. Advances in CMOS processes and GaN FETs enabled the switching frequency of DC-DC converters to be beyond 10MHz. The advancements of 3-D integrated magnetics will further reduce the footprint. In this paper, the overview of beyond-10MHz DC-DC converters will be provided first, and our recent achievements are introduced focusing on 3D-integration of Fe-based metal composite magnetic core inductor, and GaN FET control designs.

key words: *DC-DC converter, high switching frequency, 3-D integration, integrated inductor, GaN FET*

1. Introduction

Many modern electronic systems require multiple power domains to reduce power consumption and improve load response for each load chip. A small power delivery circuit system for these power domains located right next to the load is called point-of-load (PoL) converter. As the power domain number and the current consumption continue to increase, the number of PoL in recent electronic systems also increases and power delivery occupies significant portion, sometimes up to 30%, of the total system area and cost. Therefore, there are always quite strong demands to reduce the area or footprint of the power delivery circuits. The area of power delivery circuit is often dominated by passive components such as power inductors. Since the required inductance of the power circuit is basically inversely proportional to switching frequency f_{sw}, the size of power inductor can be greatly reduced by increasing f_{sw}, as it is a basic trend for the entire power electronics. On the other hand, higher f_{sw} results in higher loss as many loss components are the parameter of f_{sw}. Considering the tradeoff between loss and power density, f_{sw} of typical commercial low voltage (< 50V), low-power (< 100W) DC-DC inductor based buck converters are around 100kHz to 4MHz. However, DC-DC converters with f_{sw} higher than 10MHz are rapidly developing as integration technologies and circuit techniques are aggressively advancing to push power density even higher [1]–[62].

In this paper, high f_{sw} inductor-based DC-DC buck converters whose f_{sw} is beyond 10MHz are focused and their overview is provided with recent achievements from our group. Note that high f_{sw} resonant converters are not handled in this paper. In Sect. 2, after brief fundamentals are given to understand the challenges in the high f_{sw} buck converter, benchmarks of high f_{sw} buck converter are provided as an attempt to analyze the current status of this research area. It is found that three types of high f_{sw} buck converter exist; they are CMOS buck converters, integrated voltage regulators (IVRs), and high voltage buck converters that mainly use GaN FET. Their characteristics and requirements are also briefly explained. In Sects. 3 and 4, detailed overview for these three types of high f_{sw} buck converters are given and some recent results from our group are shared. Finally, Sect. 5 concludes this paper.

2. Overview of High f_{sw} DC-DC Converters

2.1 Brief Fundamentals of DC-DC Converters

An inductor-based DC-DC buck converter is one of the simplest yet efficient power topologies for step-down voltage conversion. Simple topology is also preferable for high f_{sw} operation. Figure 1 shows the schematic of this DC-DC buck converter. It also allows flexible output voltage V_{OUT} control and regulation. At continuous-conduction mode, following equations hold from KVL at steady state,

$$\Delta I_L = \frac{V_{IN}(1-D)D}{Lf_{sw}} = \frac{V_{OUT}(1-D)}{Lf_{sw}} \quad (1)$$

$$V_{OUT} = DV_{IN} \quad (2)$$

where ΔI_L, V_{IN}, D, and L are inductor peak-to-peak ripple current swing, input voltage, duty ratio of the switching node pulse, and inductance of the power inductor, respectively. In a typical design, ΔI_L is set to 0.1~0.3 of maximum load current I_{LOAD}, considering V_{OUT} ripple, AC loss of the power inductor, load response speed, and inductor size [63]. Figure 2 shows the surface mount device (SMD) inductors

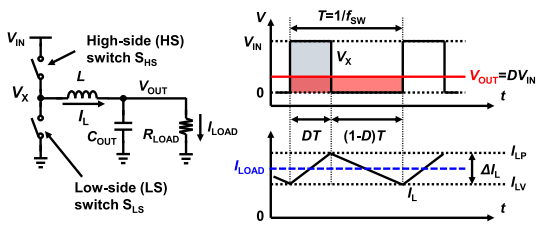

Fig. 1 Schematic and operation of inductor-based DC-DC buck converter.

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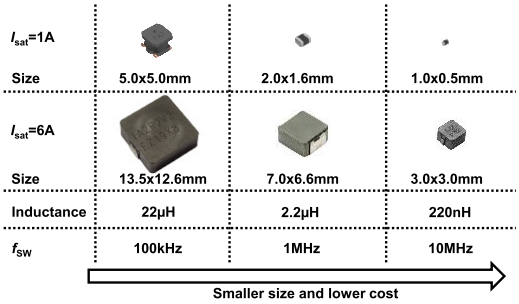

Fig. 2 Inductor size and f_{sw}.

Table 1 Loss factors in a buck converter.

Loss Components	Equation	Remarks
FET conduction loss	$P_{COND} = R_{ON\_HS}\left(I_{LOAD}{}^2 + \frac{\Delta I_L{}^2}{12}\right)D + R_{ON\_LS}\left(I_{LOAD}{}^2 + \frac{\Delta I_L{}^2}{12}\right)(1-D)$	R_{ON_HS}: High-side (HS) switch on-resistance R_{ON_LS}: Low-side (LS) switch on-resistance
Gate charge loss (Driver loss)	$P_G = (C_{ISSHS} + C_{ISSLS})V_{DD}{}^2 f_{sw}$	C_{ISSHS}: HS gate input (gate) capacitance C_{ISSLS}: LS gate input (gate) capacitance V_{DD}: Driver supply voltage V_{IN}=V_{DD} in low-voltage converter, V_{IN}>V_{DD} in high-voltage converter
Drain (output) charge loss	$P_{OSS} = (C_{OSSHS} + C_{OSSLS})V_{IN}{}^2 f_{sw}$	C_{OSSHS}: HS drain (output) capacitance C_{OSSLS}: LS drain (output) capacitance
Dead time loss	$P_{DT} = 2t_{dead}V_F I_{LOAD} f_{sw}$	t_{dead}: Dead time V_F: Forward voltage drop of body diode
Reverse recovery loss	$P_{RR} = \frac{1}{6}\sim\frac{1}{2}V_{IN}I_{RR}t_{RR}f_{sw} = V_{IN}Q_{RR}f_{sw}$	I_{RR}: Reverse recovery current t_{RR}: Reverse recovery time Q_{RR}: Reverse recovery charge
Switching transition loss	$P_{ST} = \frac{1}{2}V_{IN}I_L t_{TR} f_{sw}$	t_{TR}: Switching transition time
Inductor loss	$P_{IND} = P_{windDC} + P_{windAC} + P_{coreAC}$	P_{windDC}: Conduction loss by winding DCR P_{windAC}: AC winding loss (skin effect, proximity effect) P_{coreAC}: AC core loss (hysteresis, eddy current)

corresponding to different f_{sw} and their size. Obviously, L and inductor size can be greatly reduced as f_{sw} increases from Eq. (1) and Fig. 2 at same ΔI_L. Since buck converters with f_{sw} higher than 10MHz are focused on this paper, the required inductance is basically much lower than 1μH.

The limitation for increasing the f_{sw} is the excessive power loss. As briefly summarized in Table 1, most of the loss components in a buck converter increase by f_{sw}. For low voltage buck converter, gate charge loss P_G, drain charge loss P_{OSS}, and inductor loss P_{IND} become dominant loss factors at high f_{sw} rather than conduction loss P_{COND}. In high voltage applications such as V_{IN} = 48V converters, P_{OSS}, switching transition loss P_{ST}, and P_{IND} are dominant. Besides, for a silicon device, reverse recovery loss P_{RR} is also considerable as body diode exists while dead time loss P_{DT} is serious in a GaN FET device as it does not [64]. It should be also noted that AC loss of inductor grows faster than the other loss components as f_{sw} increases, since it contains loss components that has dependency of $f_{sw}{}^2$ or larger like proximity effect loss and eddy current loss [65]. Therefore, in some early reports, inductor loss becomes one of the largest loss components, typically in very high f_{sw} near or above 100MHz [1]–[6], [20]–[27].

2.2 Benchmarks of High f_{sw} Buck Converters

In this section, benchmarks for the high f_{sw} buck converters [1]–[60] are shown and discussed. Figure 3 shows the inductance used in the converter per phase as a function of f_{sw} plotted by inductor core type. As explained previously, the required inductance, hence basically the inductor size, clearly decreases as f_{sw} increases. Also, magnetic cores are mostly not available beyond 100MHz, and it is still not common above 30MHz. Although it is preferable to use magnetic core as the inductor size becomes much smaller than the air core, the fact indicates that the inductor core loss becomes very high at this frequency range and there are limited material candidates for magnetic core.

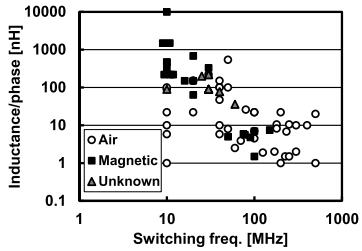

Fig. 3 Inductance per phase as a function of f_{sw}.

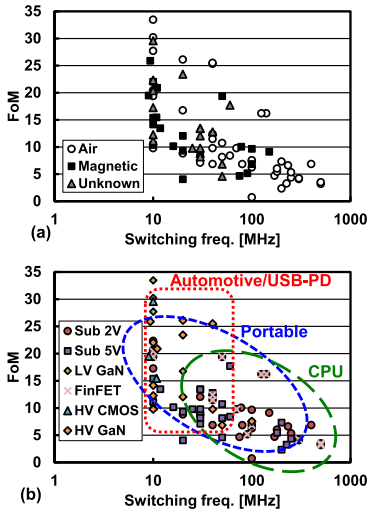

Fig. 4 FoM as a function of f_{sw}. (a) Plotted by inductor core type, (b) plotted by technology.

Figures 4 (a) and 4 (b) show figure-of-merit (FoM) as a function of f_{sw} plotted by inductor core type and technology, respectively. The FoM is defined as,

$$\text{FoM} = \frac{V_{IN}}{V_{OUT}}\frac{P_{OUT}}{P_{LOSS}} = \frac{1}{\text{VCR}}\frac{\eta}{1-\eta} \tag{3}$$

where P_{OUT} is output power ($V_{OUT}I_{LOAD}$), P_{LOSS} is loss, VCR is voltage conversion ratio (V_{OUT}/V_{IN}), and η is power conversion efficiency ($P_{OUT}/(P_{OUT} + P_{LOSS})$). Fundamentally, in a buck converter, it is difficult to achieve high efficiency at low VCR, or approximately equivalent to low duty D, as P_{OUT} becomes low while P_{LOSS} does not change much (only P_{COND} changes). To compensate for this effect, this FoM is introduced rather than using efficiency η only as a performance factor. From Fig. 4 (a), FoM tends

to decrease as f_{sw} increases indicating that it is very challenging to achieve size reduction and high efficiency at the same time by only increasing f_{sw}. On the other hand, as will be discussed in Sect. 3, some recent works with integrated magnetic core inductor are improving FoM [15], [16], [35], [39], [40], [43], [45], [50]. In Fig. 4 (b), Fig. 4 (a) is replotted by the technologies used in the converters. From this figure, high f_{sw} buck converters can be classified into 3 types. The first one utilizes sub-5V process, such as CMOS legacy process ranging from 0.35μm to 130nm CMOS process for portable applications with f_{sw} up to 50MHz while some early works adopt very high f_{sw} above 100MHz [1]–[17]. The second type is targeted for high performance CPU power delivery whose f_{sw} is mainly above 50MHz using advanced CMOS process including FinFET [18]–[50]. These two types often integrates inductor on-chip or in-package for footprint reduction, higher power density, and better load transient response. The details of these two types are discussed in Sect. 3. The third type use high-voltage technologies with f_{sw} from 10-to-50MHz where their input voltage are ranging from 8V to 48V, mainly targeting for automotive and USB power delivery (USB-PD) applications [51]–[62]. It can be also found that GaN FETs are effective to enhance FoM as their $R_{ON}Q_G$ value is much better than silicon HV FETs. This topic will be covered in Sect. 4.

3. High f_{sw} CMOS Buck Converters and Integrated Voltage Regulators

3.1 Motivations and Overview

In this section, high f_{sw} CMOS buck converter and IVR for portable and CPU power delivery applications are focused. First, the features and motivations of the high f_{sw} CMOS buck converter are explained. In portable devices like smart phones, the system footprint and size are directly related to cost. A power management IC (PMIC) in a recent smart phone uses many inductors as many DC voltage and power domains are required, so the size of the inductors should be small as possible by increasing f_{sw}. Legacy CMOS processes are mostly used from the viewpoint of cost for PMIC. Thick gate oxide devices, typically 2.5/3.3/5V I/O devices, are often used for power FET to support battery and USB voltage ranging from 2.6V to 5V. Besides increasing f_{sw}, some works integrate inductor into the PMIC package for further footprint reduction.

The second type of the high f_{sw} converter is mainly used in high-performance CPU power delivery. The load current of high-performance CPU is huge, and it is more than 10A per one power domain. Since there are many power domains in a CPU die, the total peak load current can easily exceed 100A. Furthermore, each power domain frequently change their voltage by dynamic voltage frequency scaling (DVFS) and the load transient is very fast whose slew rate is beyond A/ns. Therefore, this type of buck converter should be located close as possible to the load power domain of CPU die. This requirement is achieved by integrating a buck converter power FET and control circuit itself on the CPU die, and an inductor on the CPU die or in the package. Thus, this buck converter is called (fully) integrated voltage regulator (F)IVR. Since the inductance available in these technologies is small as 1-to-3nH, the operation frequency is very high, which is around 100MHz. This is also preferable in terms of fast load transient response and output voltage change. Thanks to the advanced process, this very high f_{sw} is possible. V_{IN} ranges between 1V and 2V, and V_{OUT} is sub-1V, thus, VCR is not so low in IVR as it is difficult to achieve even moderate efficiency by extremely high f_{sw}.

3.2 Design Strategy and Basic Circuit Techniques

As discussed in Sect. 2.1, P_G, P_{OSS}, and P_{IND} are significant loss factors in addition to P_{COND} in CMOS buck converters and IVRs. Therefore, following design strategies are adopted in these converters:

- Use low $R_{ON}Q_G$ power FET configuration
- Optimize conduction loss and charge loss tradeoff for each load point with adaptive control
- Use voltage mode PWM or non-linear control (hysteresis, constant-on-time control)
- Use efficient integrated magnetic inductor (explained in Sect. 3.3)

The first point actually applies to entire power electronics. Lower $R_{ON}Q_G$ device allows reduced charge loss (P_G and P_{OSS}) for a given power FET on-resistance, which improves efficiency [66]. Basically, thin oxide FET in advanced technology nodes offers lower $R_{ON}Q_G$ device as the FET is scaled if one can afford the process cost. Higher timing resolution also allows reduced dead-time and switching transition time of the switching node, which can reduce P_{DT} and P_{ST}, respectively. On the other hand, the voltage ratings of the thin oxide FET in the advanced technology node is typically around 1V, thus, V_{IN} beyond this voltage requires FET-stack power stage [13], [14], [25], [30], [31], [34], [35], [37], [38], [41]–[46], [48]–[50], [67] as shown in Fig. 5. By this technique, the voltage tolerance is multiplied by the number of cascode stage as long as V_{IN} does not exceed the voltage tolerance of the isolation well. In the case of Fig. 5, the voltage tolerance is doubled. Interestingly, stacked configuration often allows better total $R_{ON}Q_G$ than a single thick

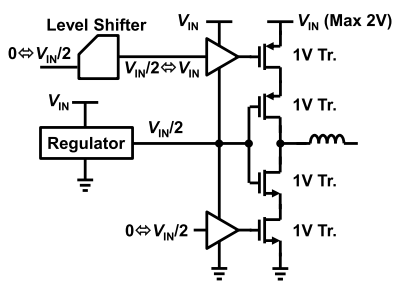

Fig. 5 FET-stack power stage for higher voltage tolerance.

oxide FET as smaller gate length and low voltage gate drive are available [48]. However, the driving circuit becomes complex because floating gate drivers and level shifters are required, which means that additional intermediate power rails and their regulators are also required. The power loss of these circuits should be considered for the detailed design. Furthermore, start-up circuits to protect the thin oxide devices are also mandatory. It should be worth noting that a new technology platform like low voltage GaN-on-silicon process targeting below 5V operation, is emerging [48]. Traditionally, GaN FETs shows significantly better $R_{ON}Q_G$ than silicon FETs only at higher voltage (> 12V) region. This is because the total on-resistance is affected by the channel and contact/diffusion resistance in low voltage devices while that is dominated by the drift layer resistance in high voltage devices, which directly reflects the GaN and silicon material properties. However, low voltage GaN process can offer much better $R_{ON}Q_G$ and thus FoM (see Fig. 4 (b)) than advanced CMOS processes. Therefore, it has a strong potential for high f_{sw} buck converters.

The second strategy is realized by circuit techniques. Fundamentally, there is a tradeoff between P_{COND} and charge loss (P_G and P_{OSS}) in a buck converter. At light load, charge loss is dominant while P_{COND} dominates at heavy load. Therefore, efficiency peaks where P_{COND} and charge loss balances at the certain I_{LOAD} for a given power FET size. If the power FET gate width is increased to reduce power FET on-resistance, hence P_{COND}, now P_G and P_{OSS} are increased as gate and drain capacitance increase. To mitigate this tradeoff, adaptive size [22], [28], [29], [42] and adaptive phase control are commonly used as shown in Fig. 6. In these schemes, power FET or bridge units are parallelly connected and the number of activated units can be varied. A current sensor detects I_{LOAD} and optimum gate width configuration (Fig. 6 (a)) or phase count

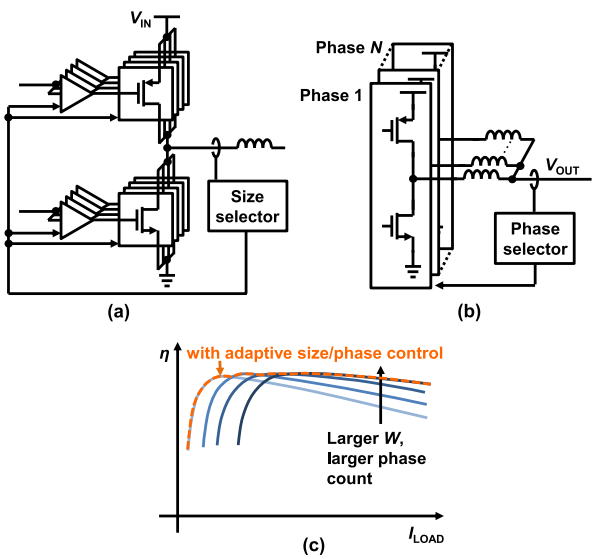

Fig. 6 Control schemes to optimize loss tradeoff, (a) adaptive size control, (b) adaptive phase control, (c) efficiency curve.

(Fig. 6 (b)) are selected by a selector block to maximize the efficiency. As I_{LOAD} increases, larger gate width or larger phase count are selected (Fig. 6 (c)). An adaptive phase control is mostly used together with a multiple phase control [2], [7], [9], [11], [12], [15], [18]–[21], [23], [25]–[27], [29], [30], [32], [33], [43]–[45], [49]–[51], [55], [60], where each phase is shifted by $360/N$ degree (N is the total number of phases). This scheme can basically reduce the ripple current by the factor of N, or it can even perfectly cancel out the ripple current at certain duty. Although multiple inductors are required, this allows higher output current, smaller inductance, and output capacitance. Furthermore, it also improves load transient response by the factor of N because the parallel inductors reduce the effective inductance by $1/N$. On the other hand, adaptive/multiple phase control requires additional DLL or PLL for phase control. It also requires a current balancing control including current sensors so that all the phases equally share the load current to avoid overcurrent in a specific phase.

The third strategy relates to regulation control. In a low f_{sw} converter below 4MHz, peak current mode PWM control are frequently used since it achieves fast load transient response with good stability [68]–[70]. In this control, high-side power FET replica current sensor is generally used for the peak current sensor. However, at high f_{sw}, the required bandwidth of the peak current sensor exceeds 100MHz to reproduce pulse-shaped high-side FET current, which is difficult to achieve in a legacy CMOS process. Therefore, unless one can afford to use an advanced process, voltage mode PWM or non-linear mode control, such as hysteretic or constant-on-time control are preferable. Hysteretic control can response very fast to load transient while maintaining stability [2], [18], [26], [27], [71]. However, f_{sw} is not fixed and it changes by I_{LOAD} and V_{IN} variations in a basic hysteretic control. This may require a wideband electromagnetic interference (EMI) filter that increases system cost and complexity. From this reason, advanced controls like adaptive hysteresis window and adaptive on-time control to fix f_{sw} has been proposed [16], [17], [72]–[77].

3.3 Technologies for Integrated Inductors

Since a demand to reduce the footprint of the inductor is very strong in a high f_{sw} low voltage buck converter, the integration of inductor on the die or in the package has been studied and developed from early 2000s. Here, high f_{sw} converters with integrated inductors whose application is not limited to CPU power delivery are defined as IVR here in a broad sense. IVRs are extracted from Fig. 4 (a) and replotted to Fig. 7. Some commercial low f_{sw} IVRs are also added [78]–[83]. As shown in Fig. 7, two major groups can be found in IVRs. Group 1 aiming for CPU power delivery as introduced before, and Group 2 that has been newly added. 2.5-D integration with an SMD inductor is used in Group 1. Since f_{sw} is very low, high FoM (efficiency) is achieved with low cost, while the size of inductor is quite large. The settling time of the load transient response is also

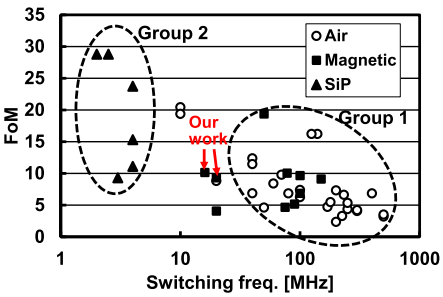

Fig. 7 Benchmarks of buck converters with integrated inductor.

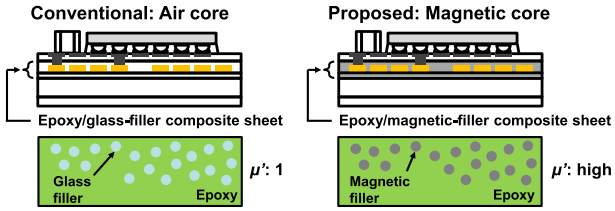

Fig. 8 Conventional and proposed package embedded inductor.

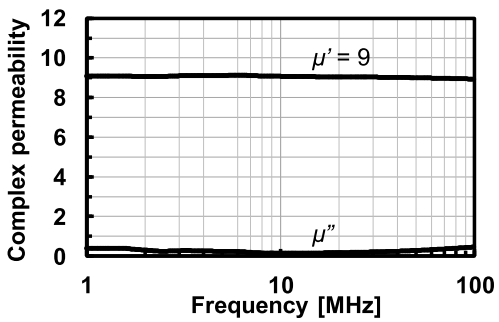

Fig. 9 Complex permeability of proposed epoxy/magnetic filler composite lamination sheet.

limited to tens of μs by the large inductance.

In Group 2, relatively early works tried to use on-chip interconnects or wire bonding for a power inductor wiring, and legacy CMOS process for a power FET. However, since only air coil was available, the wire resistance is high and the Q-factor in those works are below 5. Furthermore, small inductance resulted in very high f_{sw}, which severely damaged the efficiency. Around 2013, Intel group commercialized IVR with 22nm process CPU die and air core inductors formed by copper traces embedded in their package substrate [30]. They achieved 16-phase 140MHz operation with 16A output and 90% efficiency at V_{IN} = 1.7V and V_{OUT} = 1.05V, which is very high performance (FoM = 16.2) for an IVR.

On the other hand, magnetic core inductors for IVR are also rapidly developing in these 10 years. There are two types of candidates for the core material. One is the thin magnetic film like permalloy ($Fe_{45}Fe_{55}$) and CZT (CoTaZr) [27], [33], [35], [37], [39], [40], the other is epoxy/magnetic-filler composite [16], [43], [45], [50], [84], [85]. Some thin film processes are compatible with CMOS, so the magnetic core inductor can be integrated on-chip. However, it requires high vacuum process to deposit core and often through-silicon-via (TSV) process to form solenoid coil on-chip, which are expensive. The permeability of thin film materials are basically high, but the core loss is very high in the early works. The epoxy/magnetic-filler composites use ferromagnetic metal grain powder mixed in epoxy resin to form arbitrary shape core. Generally, permeability is relatively low ranging from 5 to 100, but the core loss is small especially when the metal grain size is very small, which is suitable for high f_{sw} operation. In the next section, 3-D IVR with a magnetic core inductor embedded in a package substrate (interposer) fabricated by epoxy/magnetic-filler composite build-up sheet from the author group is introduced.

3.4 3-D IVR with Embedded Magnetic Core Inductor

In this section, 3-D IVR with a magnetic core inductor from our group is introduced [16]. The proposed IVR targets portable applications, thus advanced process and thin film inductors are not used from the viewpoint of cost. The maximum f_{sw} of 20MHz is chosen to keep moderate efficiency. The required inductance for the converter derived from f_{sw} is 100~150nH, which is much larger than that of embedded inductors reported. From these requirements, magnetic core inductor using epoxy/magnetic-filler composite sheet is proposed. The proposed inductor is compatible with the conventional package embedded air core inductor process, where the inductor is embedded in the build-up package substrate as shown in Fig. 8. In the build-up package substrate process, epoxy/glass-filler composite sheet (i.e. Ajinomoto build-up film: ABF) is used for build-up layer by a lamination process. In this work, magnetic filler is replaced from the conventional glass filler to realize closed magnetic circuit inductor. Thanks to higher permeability of the magnetic filler, large inductance can be obtained at small size. Furthermore, high-cost vacuum thin-film and TSV processes are not required, so the process cost can be kept low in this scheme. The magnetic-filler is made of Fe-amorphous powder with the average grain diameter of 2.6μm and the relative permeability of the magnetic composite sheet is around 9 with small imaginary part up to high frequency as shown in Fig. 9. Each grain forms high resistance layer coating at its surface, which suppresses the eddy current flowing in the core. The saturation magnetic flux density B_S is 0.8T. A 6-turn embedded inductor is fabricated and the diameter is 3.6mm as shown in Fig. 10. Figures 11 (a) and 11 (b) show measured inductance and Q-factor as a function of frequency of the individual inductor, respectively. The measured inductance and Q-factor are around 150nH and 38, respectively at 20MHz. The actual inductance value and Q-factor of the inductor embedded in the package substrate pattern is lower than these values because the leakage flux penetrates into the package surface interconnect copper pattern and induces eddy current. According to FEM simulation, the estimated inductance and Q-factor are 130nH and

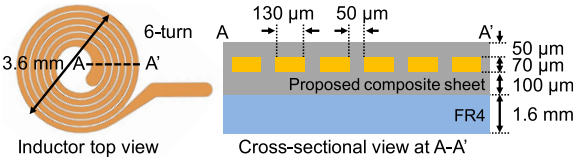

Fig. 10 Top and cross sectional view of the proposed embedded magnetic core inductor. © [2019] IEEE. Reprinted, with permission, from T. Fukuoka et al., 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, pp.1561–1566, 2019.

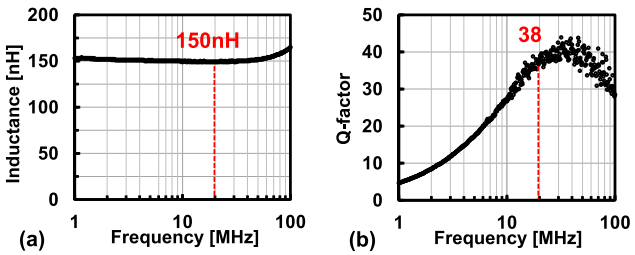

Fig. 11 Measured embedded magnetic core inductor without surface interconnect pattern. (a) Inductance, (b) Q-factor. © [2019] IEEE. Reprinted, with permission, from T. Fukuoka et al., 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, pp.1561–1566, 2019.

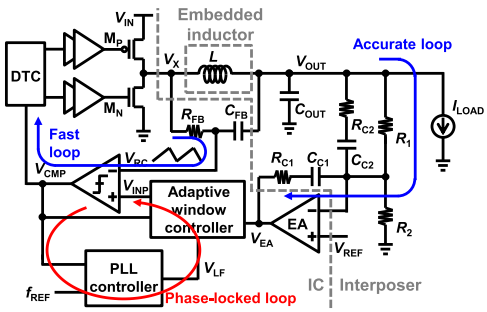

Fig. 12 Proposed IVR buck converter circuit schematic. © [2019] IEEE. Reprinted, with permission, from T. Fukuoka et al., 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, pp.1561–1566, 2019.

16~20, respectively, at 20MHz [85]. However, the Q-factor is still larger than most of the integrated inductors reported.

The buck converter circuit that is integrated with the proposed embedded inductor is shown in Fig. 12. A legacy 0.35μm standard CMOS legacy process is chosen and 5V I/O thick gate oxide transistors are used. A modified adaptive window control quasi-V^2 hysteresis PWM control is proposed and adopted in this work. By adaptively changing the hysteresis window of the hysteresis converter according to the I_{LOAD} and V_{IN}, the converter itself forms a phase-locked loop and f_{sw} is fixed to the reference frequency f_{REF}. The quasi-V^2 regulation control consists of fast loop and accurate loop simultaneously allows fast transient response and good load regulation. The adaptive window controller is shown in Fig. 13. The hysteresis window V_{HYS} is created by the variable resistor using PFET in the voltage divider, while the input common-mode voltage of the

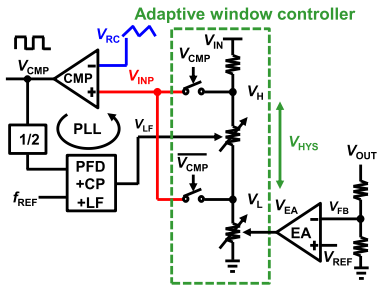

Fig. 13 Schematic of adaptive window controller. © [2019] IEEE. Reprinted, with permission, from T. Fukuoka et al., 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, pp.1561–1566, 2019.

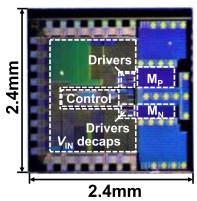

Fig. 14 Proposed IVR chip photograph. © [2019] IEEE. Reprinted, with permission, from T. Fukuoka et al., 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, pp.1561–1566, 2019.

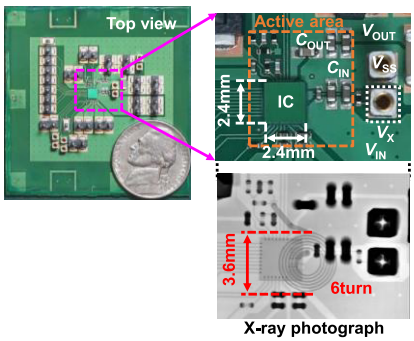

Fig. 15 Photographs including x-ray photograph of the proposed IVR. © [2019] IEEE. Reprinted, with permission, from T. Fukuoka et al., 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, pp.1561–1566, 2019.

hysteresis comparator is generated by the bottom variable resistor controlled by the error amplifier (EA) for accurate load regulation. The proposed buck converter chip photograph is shown in Fig. 14.

The measured efficiency and load regulation are shown in Figs. 16 (a) and 16 (b), respectively. From Fig. 16 (a), the maximum efficiency of 87.0% and 86.0% are obtained at f_{sw} 16MHz and 20MHz, respectively for V_{IN} = 5.0V and V_{OUT} = 3.3V. The FoM of the proposed IVR can be found in Fig. 7. From Fig. 16 (b), the percentage load regulation (PLOR) at V_{OUT} = 3.3V is 0.18%/A and 0.12%/A at 16MHz and 20MHz, respectively. Also, the variation of f_{SW} is less than 0.01%/A for full load range, thanks to the adaptive window control. As for the load transient response, 59mV V_{OUT} undershoot, 44mV V_{OUT} overshoot, and settling time below

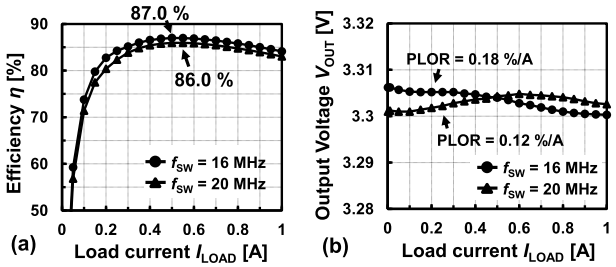

Fig. 16 (a) Measured efficiency, (b) measured PLOR of the proposed IVR. © [2019] IEEE. Reprinted, with permission, from T. Fukuoka et al., 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, pp.1561–1566, 2019.

2.6μs are observed at the load current step between 80mA and 460mA.

3.5 Prospective Views

In this section, prospective views for the high f_{sw} CMOS buck converter and IVR are provided. In terms of circuit techniques, power stage topologies that can reduce charge loss will be important. Simple hybrid topologies that combine switched capacitor and inductor based buck converter like 3-level topology [13], [14], [25], [34], [38], and double step-down (DSD) topology [86], [87] can reduce the switching node swing by half, thus P_{OSS} can be reduced by quarter. Furthermore, lower switching node voltage swing can reduce the required inductance for the same ripple performance, However, these topologies require additional flying capacitor that consumes area and decreases power density. Therefore, the integration of the flying capacitor will be the key challenge. If the requirements for the load transient response, V_{IN} transient, and V_{OUT} change for DVFS are not severe, resonant topologies including resonant gate drive circuits [88], [89] are good choices to reduce charge loss.

For the integrated inductors, new magnetic filler materials that have smaller core loss to improve efficiency or higher permeability to increase inductance density are rapidly developing. For instance, carbonyl iron (CIP)/epoxy composite sheet shows very low eddy current loss even at 100MHz thanks to the very small grain diameter of 1.1μm [43], [45], [50], [84]. This is suitable for high-end CPU IVR and has been adopted to magnetic inductor array (MIA) [43] or coaxial metal inductor loop (Coax MIL) [45], [50] for 10th generation Intel Core microprocessors and beyond.

4. High f_{sw} High Voltage Buck Converters

4.1 Motivations and Challenges

As introduced in Sect. 2.1, the third type of high f_{sw} buck converter is a high voltage buck converter that mainly use GaN FET aiming for automobile and USB-PD applications. Since electronic control units (ECUs) and processing units will be integrated on a vehicle more than ever, the demand

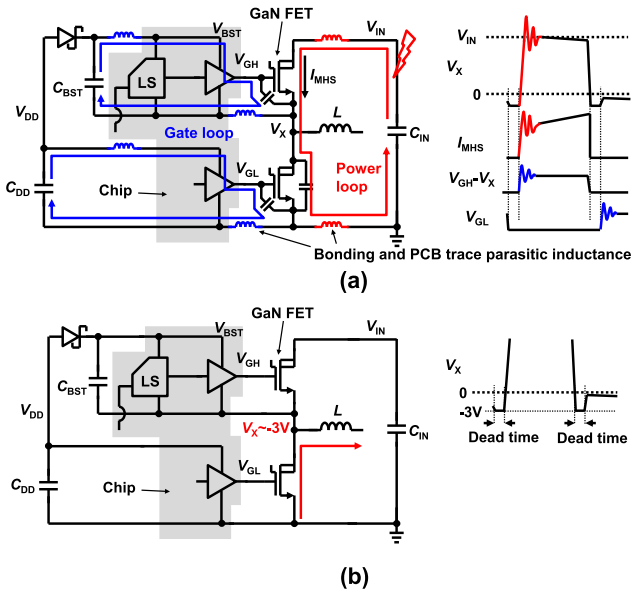

Fig. 17 Challenges in high f_{sw} GaN FET buck converter, (a) power and gate loop ringing due to high dV/dt and dI/dt, (b) GaN FET reverse conduction during dead time.

for high power density PoL converters is getting stronger in automobile applications. On the other hand, the power bus of the automobile applications has been recently increased from 12V to 48V to be compatible with a new battery standard and to reduce the bus current. Thus, the power loss in the bus resistance can be reduced by the factor of 16, but the input voltage of the PoL converters becomes 4-times higher, which will result in lower VCR and lower efficiency. The requirements for the higher input voltage and higher power density are also the same in USB-PD applications. The supported voltage rails are traditionally 5V, 9V, 15V, and 20V, and now 28V, 36V, and 48V are newly added to handle higher power. Small power connectors are also strongly demanded.

As GaN FET became available these days, the buck converter efficiency is expected to be improved from the conventional silicon FET converters by using GaN FET. It also allows higher f_{sw} operation and contributes to higher power density by the inductor size scaling. On the other hand, since V_{IN} is high, it is still very challenging to achieve good efficiency beyond 10MHz in this field even using GaN FET. Besides, a GaN FET and gate driver are mostly integrated separately so new issues related to high f_{sw} gate driving becomes apparent.

The design challenges of the high f_{sw} GaN FET driving are shown in Fig. 17. In order to achieve high f_{sw} beyond 10MHz, the slew rate dV/dt of switching node needs to be higher than few tens of V/ns. This result in high dI/dt in the parasitic power and gate loop inductance in Fig. 17 (a), inducing undesirable switching node and gate node overshoot, undershoot, and ringing by the resonance with the power FET capacitances. These phenomena degrades transistor reliability and may induce false turn-on of the power FETs.

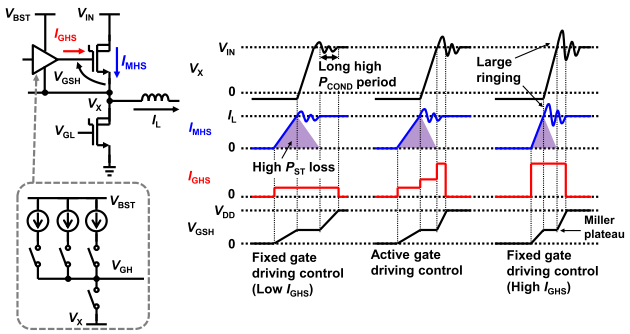

Fig. 18 The concept of active gate driving.

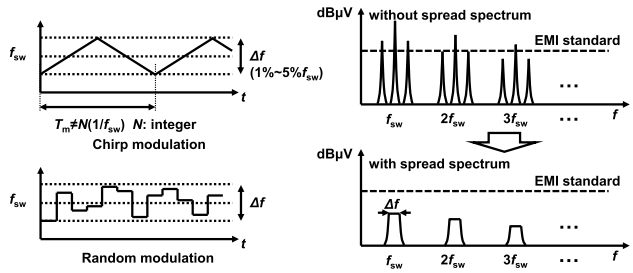

Fig. 19 f_{sw} spread spectrum modulation for EMI peak reduction.

It also induces large electromagnetic emissions that can exceed electromagnetic interference (EMI) standards. Generally, gate resistance is inserted between the gate driver output and power FET gate terminal to reduce dV/dt, dI/dt and eventually the undesirable ringing. However, if the slew rate are reduced too much, now the switching transition becomes slow and switching transition loss P_{ST} increases. The other challenges in a high f_{sw} GaN FET drive originates from the feature that GaN FET does not have a body diode. At heavy load in a silicon FET buck converter, the body diode of the low-side FET clamps the switching node to $-V_F$, where V_F is the forward voltage drop of the body diode during dead time. However, in a GaN FET converter, since there is no body diode, low-side GaN FET operates in reverse conduction mode during dead time where the switching node becomes source terminal and its voltage goes to $-V_{GS}$, which can reach -3V at heavy load as shown in Fig. 17 (b). This voltage drop is much larger than the silicon FET converter, thus huge dead time loss P_{DT} may occur even if the dead time is moderate.

4.2 High f_{sw} GaN FET Driving Techniques

In this section, techniques to mitigate the challenges explained in Sect. 4.1 are introduced. The key techniques are:

- Active gate driving
- Spread spectrum driving
- Adaptive dead time control
- Monolithic GaN FET and driver integration

Active gate driving is used to mitigate the tradeoff between voltage/current ringing and P_{ST} [56], [61], [62]. Conventionally, fixed gate resistance or fixed gate driving current is used, so the tradeoff cannot be solved. In active gate driving, as shown in Fig. 18, the gate driving current, equivalently the gate resistance, is dynamically changed during the gate rise/fall transition time. The driving current is basically controlled by changing the gate driver buffer size dynamically. The basic idea is to reduce the gate driving current during the current transition to reduce dI/dt noise and increase it after the current transition to reduce switching transition time and on-resistance. Active gate driving technique itself is commonly used in high voltage (> 100V) and high-power FET driver where dV/dt and dI/dt are also high [90], [91]. There are many driving patterns and circuit implementations reported. This is because in high voltage/-power drivers, the transistor size is large and f_{sw} is low, thus the transition time is more than 10ns, which allows to implement complex driving pattern. Conversely, in high f_{sw} beyond 10MHz, there are not so many reports as the timing control is severe and difficult. Further development is expected for this technique.

The spread spectrum driving technique introduced as the second technique is to reduce EMI [56], [92]. This scheme modulates f_{sw} and the EMI peak spectrum is reduced by the principle of spread spectrum modulation as shown in Fig. 19. The EMI spectrum is averaged at the bandwidth of the modulation frequency Δf, which is typically 1-to-5% of f_{sw}. Δf should be also above 20kHz to avoid audible noise. There are several ways to modulate f_{sw}. In this example, switching frequency is chirped but if f_{sw} can be changed randomly, larger EMI peak reduction can be achieved. However, random f_{sw} modulation may degrade V_{OUT} regulation when f_{sw} suddenly jumps to very different frequency.

To reduce P_{DT}, dead time in GaN FET buck converter should be small as possible. However, shoot-through current must be avoided in the main bridge. The simplest way to control dead time is to use fixed bit trimming that adjust the delay of the delay line for dead time generation, or to changethe external resistor that generates bias current to determine dead time. However, these methods are vulnerable to process variations as the required dead time is nearly zero. Another technique is to detect negative V_X voltage at dead time and turn on FET as fast as possible [62]. However, this requires very fast comparator and driver. Therefore, adaptive dead time control that minimizes dead time using feedback control is an effective solution [52], [57]. Many adaptive dead time controls are proposed including low f_{sw} reports, but it can be classified in to two types. The first type aligns the high-side FET gate rise and fall edge with the low-side FET gate fall and rise edge, respectively, using well known synchronizing techniques like delay-locked loop (DLL) as shown in Fig. 20 (a) [57]. In GaN FET converter, dummy level-up and -down shifters are intentionally inserted in low-side drive path to avoid delay mismatch between high-side and low-side drive path. The other type is shown in Fig. 20 (b) [52]. This scheme samples switching node voltage at falling and rising edge of the low-side FET gate signal and compares with 0V. If the sampled voltage is

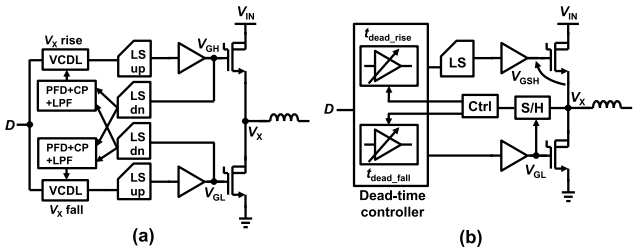

Fig. 20 Active dead time control for dead time minimizing, (a) DLL type, (b) V_X sampling and compare type.

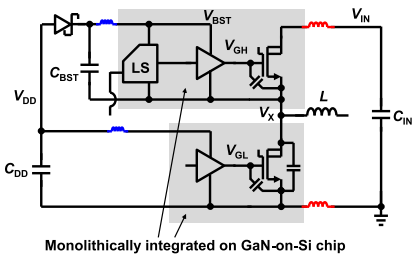

Fig. 21 Monolithic integration of GaN FET and driver on GaN-on-Si chip.

negative, it means that the dead-time is too long, so the control circuit prolongs the dead-time by changing the delay of the variable delay line in the dead-time circuit, and vice versa. These kinds of feedback control can remarkably reduce the dead-time down to sub-0.5ns for various operation and process conditions, but they are sensitive to noise.

The final techniques introduced here is to integrate GaN FET and gate driver monolithically using advanced GaN-on-Si process [61], [62], shown in Fig. 21. The number of system components can be reduced a lot and thus cost is reduced. Furthermore, since the power FET locates very close to the gate driver, parasitic inductance is significantly decreased. Especially, for the gate loop, it is reduced by an order of magnitude. As a result, extremely high slew rate and f_{sw} of 50MHz with 48V input are demonstrated in the recent works. The challenges of GaN-on-Si process relate to the process maturity. Since a p-type GaN FET is not available, all the circuit blocks should be implemented using a n-type GaN FET. The process variation is much larger than silicon process and threshold voltage shift due to aging is currently large too. Process monitoring and compensation circuit and system techniques are be the current and future topics along with the process improvement.

4.3 Integration of GaN FET Driver and Controller

In this section, a recent work from the author's group are introduced [60]. There are not so many reports that integrate both regulation control and GaN FET gate driver in a single die, as conventionally driver and digital controllers are separately provided in this area for the system design freedom. However, as high f_{sw} operation requires very small loop delay in reality, regulation controllers should be integrated with the gate driver. Here, a 10MHz constant frequency adaptive on/off-time (CF-AOOT) control with GaN FET

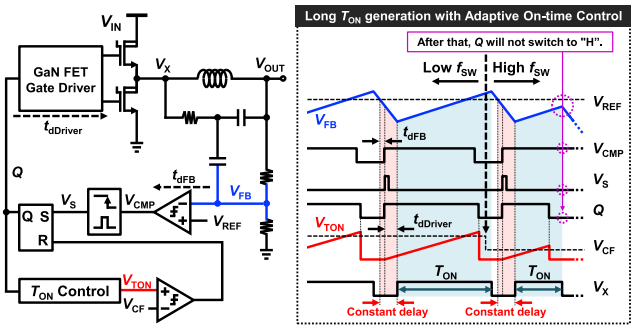

Fig. 22 Issue of high f_{sw} AOnT control at long T_{ON}.

driver is proposed to achieve GaN DC-DC buck converter with wide range VCR at high f_{sw}. Although some high f_{sw} GaN FET converters have integrated controllers [51], [55], they focused on low VCR. However, in some cases, like 24V input USB-PD power delivery, wide V_{OUT} range of 5-to-20V is required. This corresponds to VCR of 0.21 to 0.83 at high f_{sw}. In order to achieve wide VCR, this work utilizes CF-AOOT control that is fully integrated with GaN FET drivers on 250nm HV BCD process chip.

The proposed control is based on ripple injection type adaptive on-time (AOnT) control buck converter for its simple yet fast load transient response features. When f_{sw} becomes high or on-time T_{ON} is very long due to extreme VCR, the delay of GaN FET driver and comparator cannot be ignored in the switching cycle. At the worst case, the converter fails to operate normally as shown in Fig. 22. The proposed CF-AOOT control switches AOnT and adaptive off-time (AOffT) control at VCR around 0.5 to realize a wide range of V_{OUT} as shown in Fig. 23 (a). This can be simply achieved by introducing DINV signal and XOR to reverse the polarity of the control as shown in Fig. 23 (b). The details of T_{ON} control and CF regulator can be found in [77].

Figures 24 (a) and 24 (b) show the photograph of the designed chip and board, respectively. A 3030 metric SMD 220nH inductor is mounted on the backside of the board. Figure 25 (a) shows the measured shows the measured power conversion efficiency, with various V_{OUT}. The peak efficiency of 84.4%, 88.6%, 91.3%, 92.1%, and 95.4% are achieved at V_{OUT} of 5V, 9V, 12V, 15V, and 20V, respectively. Figure 25 (b) shows load regulation for each V_{OUT}. PLOR ranges from 0.47% to 1.2% for full load range up to 1.5A with fsw ranging from 9.3MHz to 13MHz, successfully showing that high efficiency and wide VCR operation at high f_{sw}.

4.4 Prospective Views

Prospective views for the high f_{sw} GaN FET buck converter are discussed here. Since high V_{IN} and high f_{sw} generates very large P_{OSS} and P_{ST} loss, very low VCR hybrid topologies are strongly expected. However, these converters show very high efficiency, they still operates at below 4MHz, as complicate high-side switching drives are re-

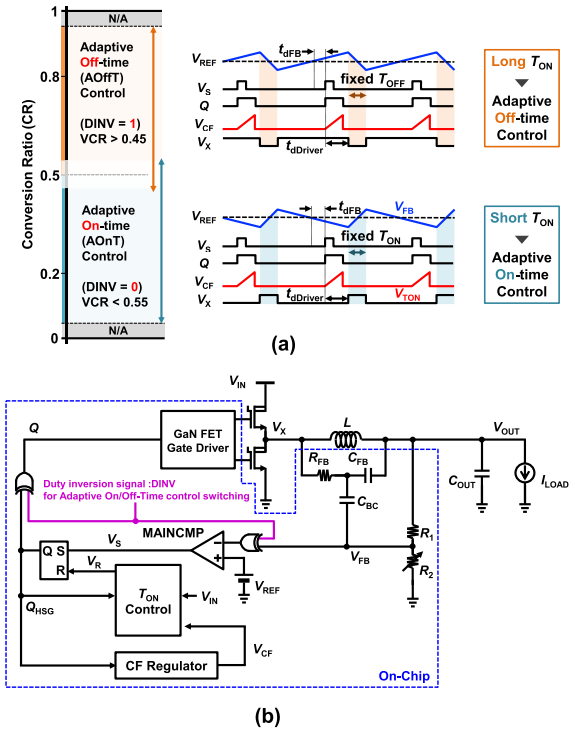

Fig. 23 Proposed CF-AOOT control, (a) control policy, (b) circuit implementation.

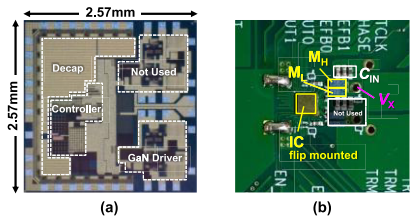

Fig. 24 Proposed CF-AOOT (a) chip photograph, (b) board photograph.

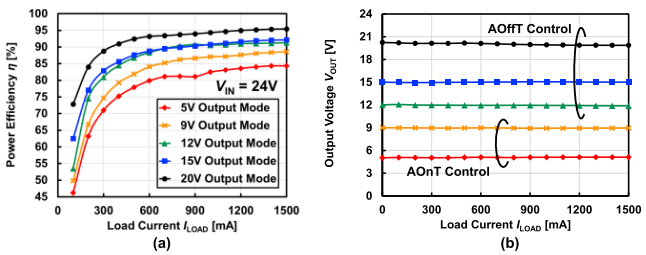

Fig. 25 Measurement results, (a) efficiency, (b) load regulation.

quired [93], [94]. Therefore, fast and accurate control is required for hybrid topologies. Other promising circuit techniques are zero-voltage switching (ZVS) circuits. Using auxiliary branch which is consisted of LC resonant tank or small inductor power path, switching node can be fully charged or discharged before high-side or low-side FET turn on, respectively. This can remove P_{OSS} and P_{ST}, or even P_{DT}, which contributes to significant efficiency improvement. On the other hand, an additional low loss inductor is required. Additional loss by the auxiliary branch should be much smaller than the efficiency improvement achieved by ZVS too. Furthermore, ZVS should be achieved in wide V_{IN} and V_{OUT} range for practical usage [58], [95]. These techniques are also not well established at f_{sw} above 10MHz. In the near future, these controls are expected to be integrated into GaN FET driver as well as main regulation controls in a single die. As discussed in Sect. 4.2, new circuit techniques and process improvements in monolithic GaN process are also strongly demanded.

5. Conclusions

The overviews for the design and integration of the high f_{sw} inductor-based DC-DC buck converters whose f_{sw} is beyond 10MHz are provided in this paper. Three types of high fsw buck converters are introduced using benchmarks, and their applications, motivations, challenges, integration technologies, circuit techniques, and future prospective views are explained in each section. Furthermore, IVR with embedded magnetic inductor and integration of GaN FET driver and regulation control from the author's group are introduced.

Acknowledgments

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